Closed-loop control of a high-voltage induction machine using a high-voltage multi-level converter

by
José Miguel Sánchez Lobato

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Author...
José Miguel Sánchez Lobato

Certified by...
David Díaz Reigosa
Associate Professor
Thesis Advisor

Certified by...
Fernando Briz del Blanco
Full Professor
Thesis Coadvisor

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Abstract

In this thesis, a complete set of hardware and software has been designed and implemented to interface a Neutral Point Clamped three level converter in order to perform a closed-loop control of a high voltage induction machine.

The hardware design is related to the selection of the proper components for the correct communication with the PC, linkage to the NPC through fibre optic link, design of the filter stages, reading of the encoder signals and finally design and building of the PCB.

The software carries out the development of the algorithms to implement the closed-loop control of a high voltage induction machine by reading the encoder attached to its shaft and controlling the currents flowing to the machine.

The equipment used has been a 4kV, 36A high-voltage high-power supply unit to feed up the NPC converter capable to manage 4kV, 40A to control a high-voltage induction machine with rating $690V_{ph\text{-}ph}$, 45kW, 2pole, 50Hz, 2970rpm.

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Chapter 1

Introduction

1.1 Motivation and Objectives

The concept of multilevel converters has been known since 1975. The multilevel terminology started with the three level converters. This topology promoted the development of new topologies with more than three levels.

The advantages that the multilevel converters introduce can be summarized in the next points:

- They are able to generate the output with lower harmonic distortion than the PWM traditional ones. Also, the harmonic content of the input current is lower than the PWM traditional converters.
- In addition, they reduce the *dv/dt* stresses induced in the switches since they have to support lower voltage than the two level PWM converters.
- Closely related to the work developed (as it is used to control an induction machine), the common mode voltage that the multilevel converters produce is lower than the PWM converters. This behaviour causes in the bearings of the motor to have smaller mechanical stress. Furthermore, such common voltage can be reduced by using modified modulation strategies.
- Multilevel converters (depending on the switches used) can operate at both fundamental switching and high frequency switching as PWM converters do. The lower the switching frequency, lower the switching losses and therefore, higher the efficiency.

However, some drawbacks of the multilevel converters make them unsuitable for all the situations. One of the main disadvantages is related to the number of switches used. As the number of levels is increased, the number of switches increases also. Subsequently, all of them will require a gate circuitry to manage its switching state which causes the system to be more expensive and complex.

Many multilevel converter topologies, control and modulation strategies have been proposed, but, three different major structures have been reported in the literature: cascaded H-bridges converter (with isolated DC links), neutral point clamped (using diodes) and flying capacitor (or capacitor clamped). In the case of the modulation, many strategies have been studied also: sinusoidal pulse width modulation (SPWM), space vector modulation (SVM) and others.

Applications for multilevel converters are mainly industrial medium voltage motor drives (the application related to this work), renewable energy systems, flexible AC transmission systems (FACTS) and traction drives.

The aim of the work developed is, in the end, to perform a closed-loop control of a high voltage induction machine. Starting from a commercial DC source, a custom NPC multilevel inverter, and a commercial induction machine, the PCB board to interface the PC to the inverter has been developed. Also, the work carried out includes the software needed to implement a speed control using the readings from an encoder attached to the shaft of the machine.

1.2 Neutral point diode clamped multilevel converter (NPC)

1.2.1 Background

This kind of topology was first proposed by Nabae, Takahashi and Akagi in 1981. It was basically a three-level diode-clamped inverter [1]. A three-phase three-level diode-clamped inverter is shown in Fig. 1. The NPC inverter can be found in literature as three, four or five-level inverter, but only the three-level inverter was used wider than the other topologies.

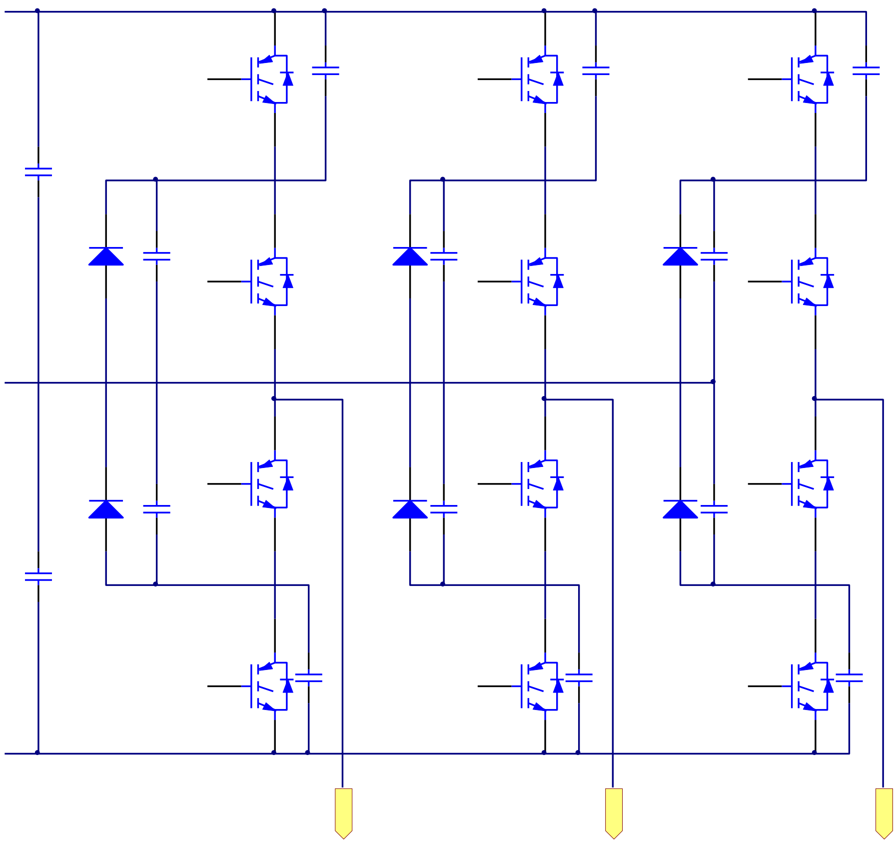


Fig. 1 3ph 3-level NPC inverter

Each of the three phases is connected to a DC bus which has been divided in three levels by using two capacitors. As it can be seen, the two levels are connected each other by means of a clamping diodes forming the neutral point which sets the division in the DC bus. Connecting the semiconductors this way allows the power devices to block half of the total input voltage.

In order to control the converter, only two signals are needed per phase which are complementary to avoid the short circuit of the DC bus. The gate signals are binary signals since a zero stands for the OFF state of the switch and a one represents its ON state.

Table1represents the different switching states of the converter with its corresponding voltage outputs. Fig. 2shows graphically the states gathered in the table below as well as the current flow achieved in each state.

	S1	SS	S'1	S'2	Vout
I	1	1	0	0	VDC
II	0	1	1	0	0
III	0	0	1	1	–VDC

Table1 NPC inverter switching pattern

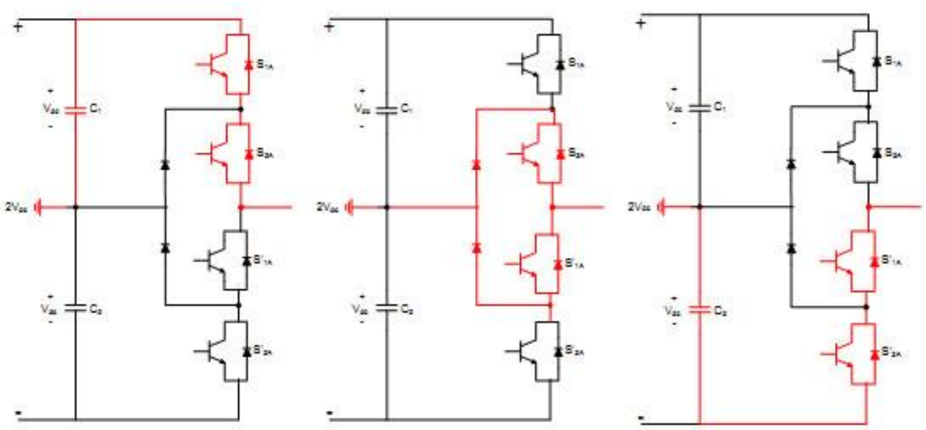


Fig. 2 Output voltage generation

Each active switching transistor is required to block a voltage level of VDC and the number of diodes is six. As the number of levels is increased, the number of transistors and diodes increase, and, when the number of levels is high enough, the number of required diodes makes the converter to be almost impossible to implement.

Furthermore, as the control strategy will be based on PWM, the diode reverse recovery of the clamping diodes causes a great challenge when applied to high power applications [2].

1.2.2 Advantages and drawbacks of NPC inverters

Many features offered by the NPC inverter made it one of the first candidates for energy conversion applications. One of them is that the semiconductors have to withstand VDC/2 during its OFF state.

The line to line voltage is composed by three levels (+VDC, 0 and –VDC) leading to lower total harmonic distortion. Also, the stress induced because of *dv/dt* is lower than the classical two-level PWM inverters.

However, NPC have disadvantages derived from the clamping diodes needed, more or less complicated PWM switching strategy depending on the control and possible unbalance in the DC bus capacitors because of its inherent differences introduced by their manufacturing.

In this condition, if the DC neutral point has too much deviation and an undesired voltage distribution takes place, may lead to a premature failures of the transistors increasing the THD of the output voltage [3].

Chapter 2

Hardware design

In this chapter, the description of the hardware design is done. First, the emulation PCB board needed to communicate the microprocessor to the PC in order to program it and to run the application. In second term, a description of the interface board is detailed. Such PCB board have several modules ready to use: errors connection, PWM control signal optical link, SCI and SPI interface, A/D conversion, filters, etc.

2.1 Emulation board

The DSP used for the project has been a TMS320F28335, floating point Delfino® Microcontroller from Texas Instruments. In order to connect the DSP to the PC, an emulator board in needed. The designed board is based in the XDS100 [4] emulator from Texas Instruments.

However, a different digital isolator has been used in order to separate (for protection purposes) the USB part of the PC from the rest of the circuit. This way, in case of an electric fault in the interface board, it is not passed to the PC protecting it from electrical shocks.

Fig. 3 shows the emulation board. Its main component is the FT-2232D from FTDI, used to translate the DSP UART protocol to the USB protocol. It has the whole USB protocol embedded, so there is no need for an additional firmware and serves as a bridge between the DSP and the PC. It is USB 2.0 full speed compliant (12Mbaud).

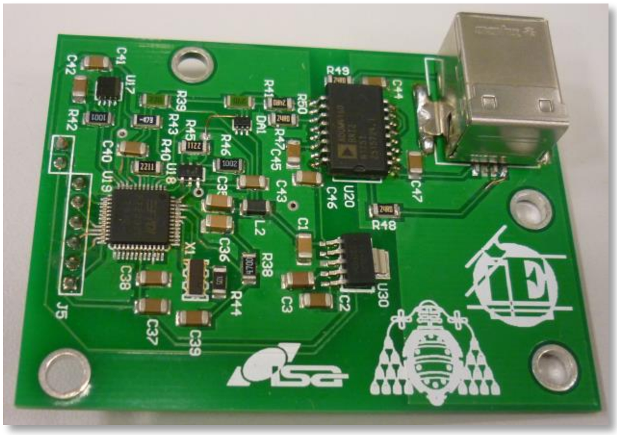


Fig. 3 Emulation Board

The emulation board also implements the JTAG protocol developed by Texas Instruments. Such a protocol provides the user the ability to emulate the microcontroller for debugging purposes.

The emulation PCB board also has a 4kBit EEPROM memory (93LC66BT from Microchip) which stores the serial number of the emulator. Finally, the digital isolator used belongs to ST semiconductors, ADUM4160BRIZ. The digital isolator is connected directly to the USB and interfaces the FTDI. As soon as the interface board is powered up, the emulation PCB is also powered and the emulator is detected by the host and automatically connected.

2.2 Interface board

The interface board includes several modules useful for the control of the NPC inverter and many other features. Since the DSP is able to generate up to twelve PWM control signals the interface board can also manage all of these twelve signals. Hence, only one NPC inverter can be controlled or two classical PWM inverters as they only need six PWM signals each one. Fig. 4 shows a general overview of the interface board as well as its main modules.

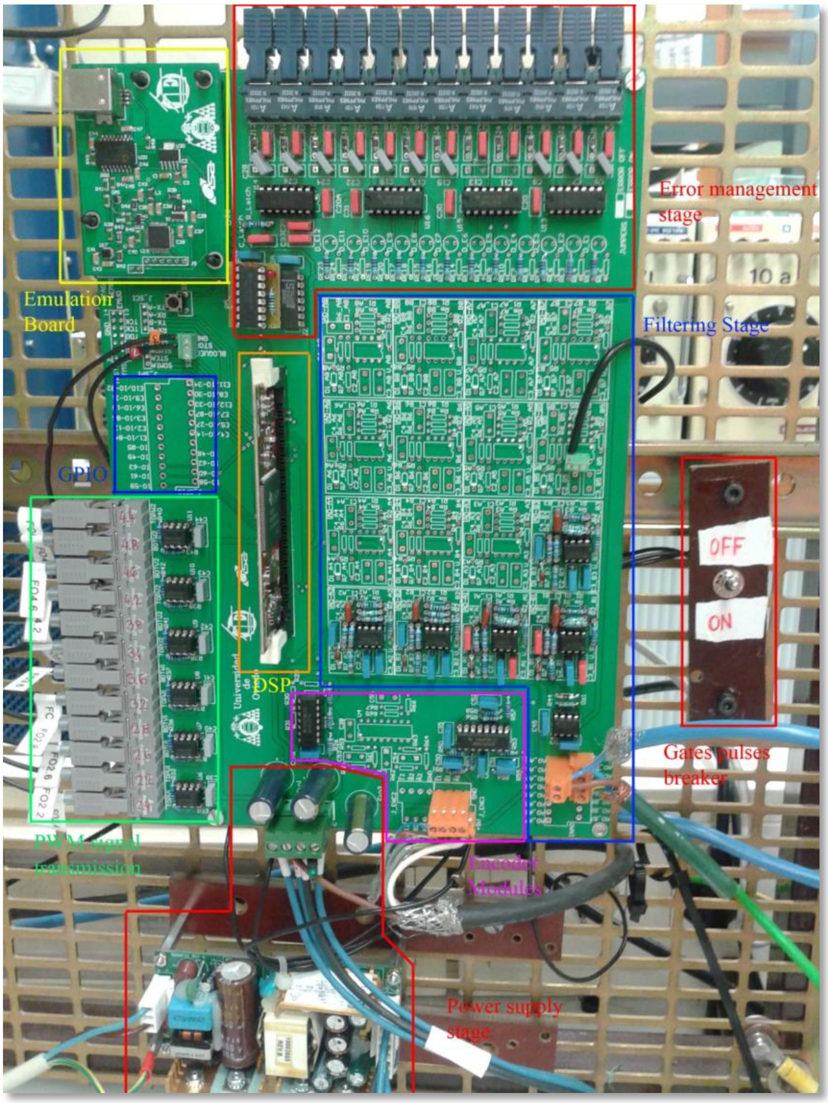


Fig. 4 Interface board general overview

Each of the modules that compose the interface board can be studied independently as the interact each other but their design is not fixed by the other existent modules. The modules that compose the interface board are listed below:

- Error management: The errors reported by the IGBT drivers, are collected altogether resulting in only one error signal which is sent both to the DSP in order to acknowledge its triggering and to a flip flop IC which blocks the sending of the gate pulses to the optical link.
- Gate signals: The PWM signals to be sent to the drivers have to be conditioned to the levels of the line drivers which perform the electrical to optical signal transducing.
- Filtering stage: Needed for the A/D acquisition, the implemented filters can be totally customized in order to achieve the desired cut-off frequency. However its architecture cannot be modified. Each of them is composed by two stages.
- GPIO: Several general purposes input-output ports have been connected to a terminal in order to be used as desired.
- Encoder modules: Two different encoder modules have been implemented. Both of them use differential reception in order to eliminate noise when reading the speed of the machine.
- SCI and SPI connections: The DSP allows the user to communicate with other peripherals by means of the SCI and SPI modules.
- Power stage: As the DSP is 3.3V signal tolerant, all the IC used in the board work at 5V level, and all the operational amplifiers have to be polarized to +15V and –15V, a multiple power stage have to be implemented.

2.3 Error Management

In order to avoid the operation of the inverter in a faulty situation, the gate signals have to be stopped when any of the drivers reports an error. The error management part of the board implements the reception, voltage shifting, pulse blocking and visual advising.

All the twelve drivers that manage the switching of the transistors have the ability to feedback errors to the interface board because of three main reasons:

- Overvoltage during turn off
- Overcurrent in all short circuit conditions

The board does not establish difference between any of the three types of error since the useful information of the error is only the notification itself to stop the gates pulses to avoid damages on the switches or even risk situations.

This part implements also a R-S latch IC (MC14044 from ST Semiconductors), which stores in its output a voltage level blocking the PWM gates signals sent to the transmitters. The latch also serves as a powering-up protection since the prior signal is the Reset. In the powering-up of the board, both the inputs adopt a logical zero, so as the latch gives priority to the R, the output of this final stage of error management sets a logical zero.

The output of the latch is connected to a final AND gate (SN74LS08N from Texas Instruments) which collects its signal and a signal coming from an external breaker. Such a breaker has the purpose of block the pulses externally by hardware. Operating this way, in case of a fault in the board or in the software (or even in case of an uncontrolled or wrong operation) the pulses can be turned off just by deactivating the breaker. Hence, an extra security measure is provided to the user.

As the A/D acquisition starts with the run button in the software, there may be some inconsistencies if the run button is pressed and the pulses are not turned on (speed of the machine, current regulators, control actions, etc.), leading to erroneous situations which may be potentially hazardous. So, in order to run the program, the external breaker has to be activated before starting the program to allow the control to operate correctly.

The effect on the PWM gates signals is its blocking and no PWM signal is sent to the transmitters. Also, the purpose of introduce a latch in the circuitry is to avoid undesired triggering events caused by noises in the system.

Fig. 5shows the schematic implemented for this part. The process of receiving, notify and blocking the gates pulses is explained in the next steps:

- When an error is reported, the correspondent fibre optic transmitter turns off the light for a while.
- The receiver which gets the error turns its electrical output to a logical one.
- The output of the logical NOR gates notifies the error by setting its output to a logical zero.
- As the DSP voltage level (3.3V) and the gates voltage level (5V) are different, a voltage shifter is needed. The selected IC was 74LS07N which has an open collector output stage capable to deliver up to 1A. By means of a pull-up resistor, the output of the gate is now at 3.3V level.
- The output of the logical gates is sent both to a GPIO of the DSP in order to be detected via software and to the latch which manages the blocking of the PWM transmitters.
- As the system is working correctly at this stage (pulses breaker turned on), the final AND gate output follows the event triggered by the latch. So the output of the AND gate is going to be a logical zero from now.
- The transmitters implement a built-in AND gate. One of the inputs comes from the PWM signal of the DSP and the other signal from the latch. When the error is notified to the latch, it blocks the gates pulses just by setting its output to a logical zero.
- The gates pulses remain blocked until the reset button in the board is pressed in order to clear the error and restart the control of the inverter.

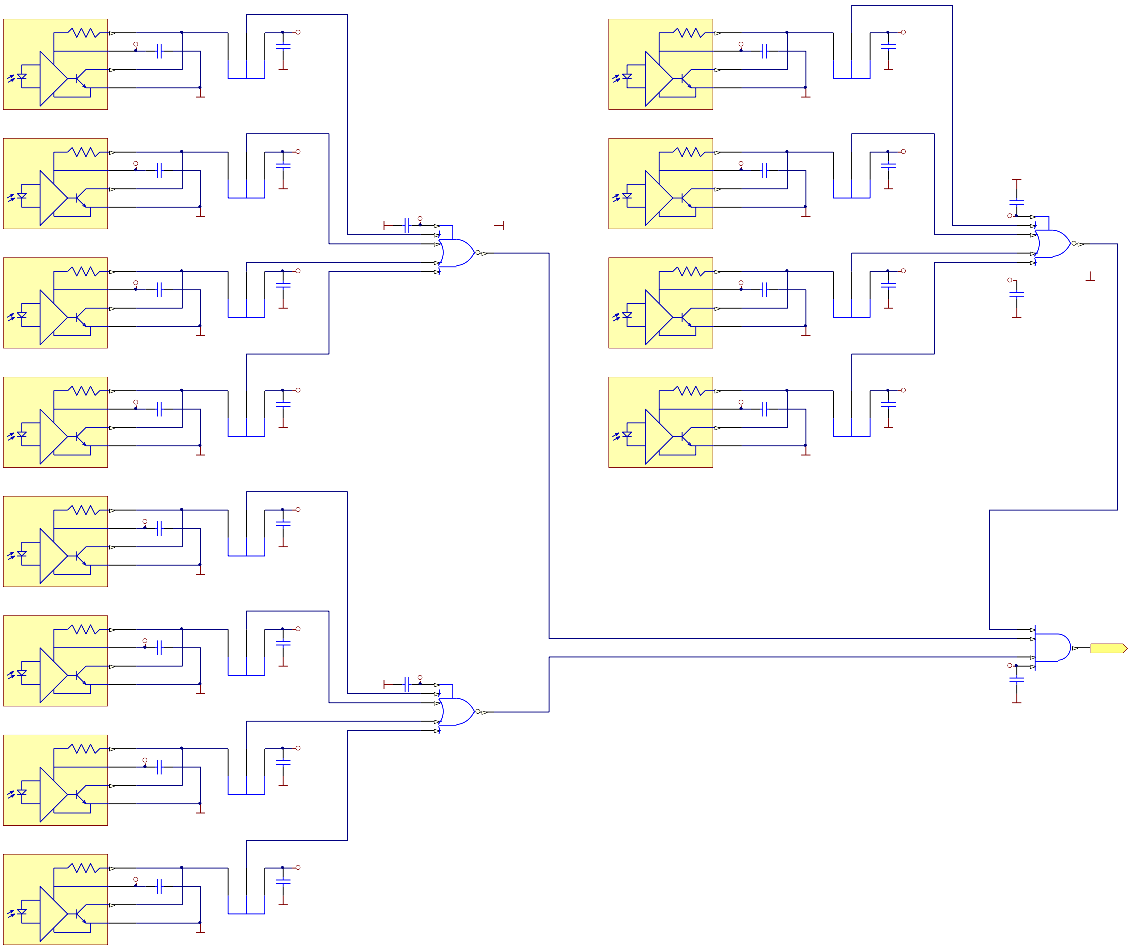


Fig. 5 Error management logic gates

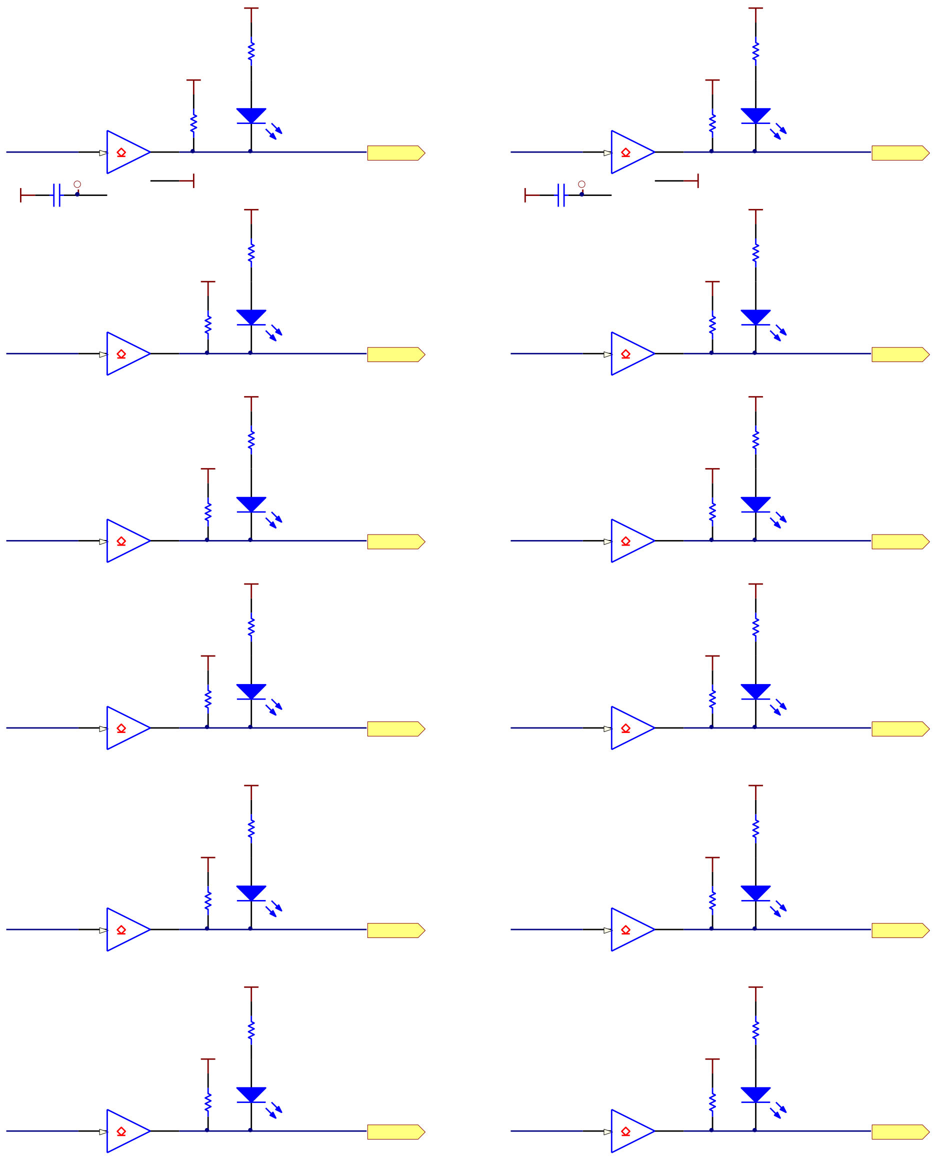


Fig. 6 Error Voltage shifting

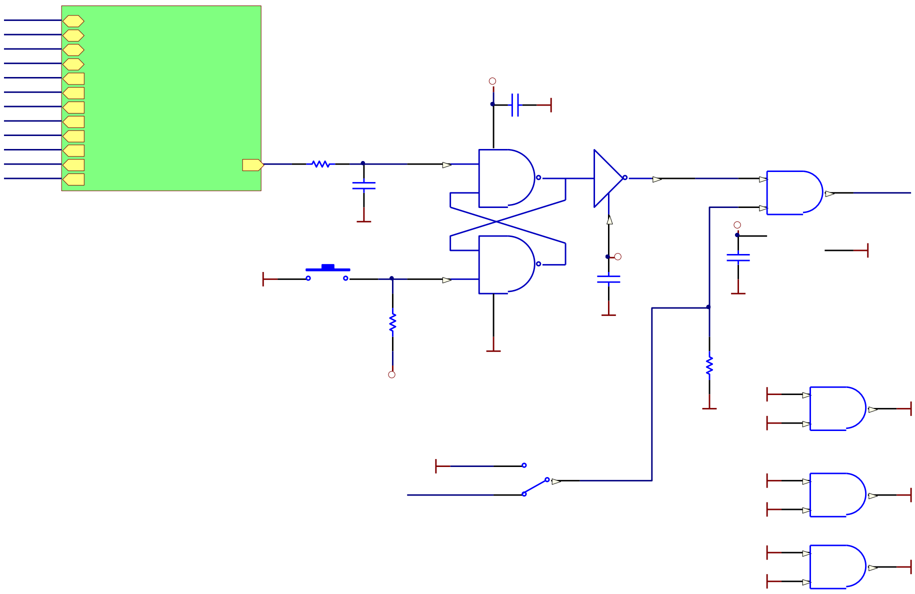


Fig. 7 Latch and final AND gate

Additionally, a LED attached directly to the second output of the latch notifies the error occurred visually. It follows the behaviour of the gate blocking stage and remains turned on until the reset button is pressed.

2.4 PWM gate signal generation

The PWM gate signals are generated by the PWM modules of the DSP. The outputs of the DSP are 3.3V level. However, the fibre optic transmitters (HFBR-1522 from Avago Technologies) need up to 80mA of current to correctly polarize the LED which sends the optical signal. Also, their levels are 0 to 5V which are not compatible with the DSP voltage levels.

These issues caused in the circuitry to implement an intermediate power stage capable to manage all the current demanded by the transmitters. Also, the transmitters have to be controlled by the error management stage. These operating conditions are perfect for the line driver suggested by the manufacturer of the transmitters.

The line driver suggested by the manufacturer was the SN75451BP from Texas Instruments. Such a line driver has two NAND built-in gates, the capability to manage up to two transmitters (which reduces the number of line drivers needed) and an open collector output power stage capable to deliver 50mA.

The output of the line driver is connected directly to the input of the fibre optic transmitter. As the output of the SN75451BP is an open collector, a pull-up resistor has to be connected to set up the output voltage to the +5V rail.

As said, the input stage of the line drivers is a NAND gate. Its logical levels are fully compatible with the output voltage levels of the DSP so there is no need to implement an intermediate buffering stage. Hence, one of the inputs of the NAND input gates is connected directly to the PWM output of the DSP.

A special situation takes place when the software used to debug, programs the memory of the DSP. In this process its PWM outputs are set in high impedance state while the outputs can be modified without control by any part of the rest of the circuitry. This condition may lead the inverter to a risk situation where the switches may be turned on without control.

In order to avoid such situation, a pull down resistors have to be connected to the inputs of the line drivers. This way, the resistors fix the voltage to a logic zero (IGBT in OFF state) when the DSP is being programmed avoiding that risk situation.

The other input is managed by the error output. Unless the latch releases the blocking signal, the line drivers cannot sent signals to the gate drivers. As both the error output and the line drivers (SN75451BP) have TTL technology they are totally compatible. Also the final AND gate has enough power to manage all the six line drivers needed to control the NPC inverter.

2.5 Fibre optic links

The fibre optic links selected for the sending and receiving of the signals were a standard performance 10m long. They are composed by a simplex cable with a latching function that ensures the correct locking of the fibre optic into the receivers or transmitters.

The fibre optic (HFBR_RLS010z) is also manufactured by Avago Technologies, made from optical plastic (which implies a low cost). It has 0.22dB/m attenuation, 1mm diameter. The signal wavelength is 660nm.

In order to establish a difference between the receiving end and the sending end, both of them have different colour connectors. Hence, the colour of the end attached to the receiver is blue while the sending end has a grey colour.

Fig. 8 shows the fibre optic used for the link as well as the entire family of transmitters and receivers used in the project.

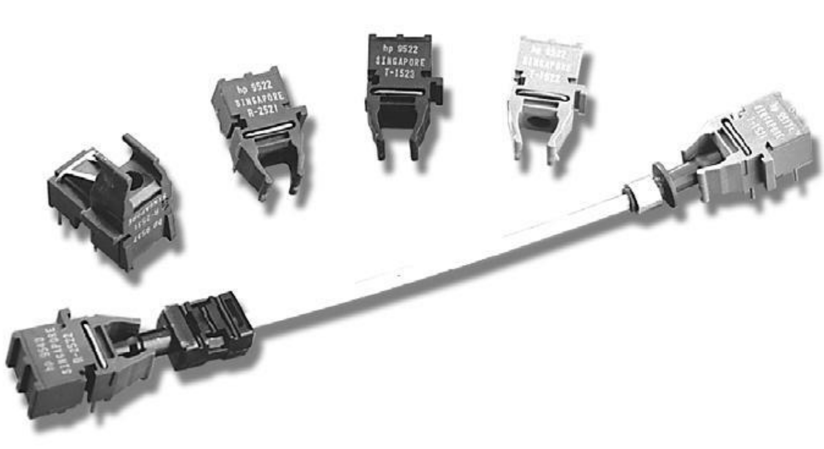


Fig. 8 Fibre optic link, transmitters and receivers

2.6 Error Reception

The transducers used to transform the optical signal into an electrical one have been the HFBR-2521Z from Avago Technologies. Such transducers belong to the Versatile Link family.

As Fig. 9 shows, the transducer has a built-in circuitry capable to deliver up to 25mA. Their outputs are connected directly to a high impedance input stage gates, hence this is not a problem since their current capability is high enough. They have an open collector output stage with a built-in pull up resistor. Their supply voltage has to be 5V.

This circuitry causes the output of the receiver to have a negative behaviour: when the transmitter is sending a logic one (light turned on), the receiver puts in its output a logic zero. On contrary, when the transmitter is sending a logic zero (light turned off), the receiver is getting a logic one in its output. This has to be considered when designing the rest of the circuit.

The maximum data transfer rate that they can manage is up to 1MBd. Such parameter is far away from the frequency used for the switching pattern of the IGBT, 2kHz.

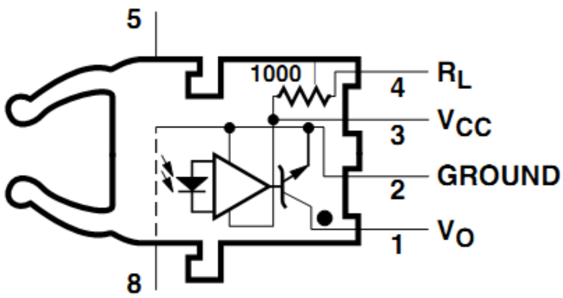


Fig. 9 Receiver built-in circuitry

2.7 PWM transmission

In order to send the PWM signals, a HFBR-1522z transducer has been used. Such a transducer belongs to the same Versatile Link family from Avago Technologies as in the case of the receivers.

The transmitter has a built-in diode with a 660nm wavelength which is used to send the information through the fibre optic. However, as the signal cannot be viewed directly, the transmitter includes a general purpose LED which acknowledges whether the transmitter is sending information or not.

As said before, the transmitters are managed by a line driver capable of manage two transmitters each one. As the line drivers have an open collector output stage, a pull-up resistor has to be connected to the +5V rail in order to set the operating current. In this condition, and taking the values of the datasheet, the resistor is calculated for a forward current of 25mA causing in the diode to have a voltage drop of 1V approximately.

Fig. 10 shows the selected schematic for the correct polarization of the transmitter diode.

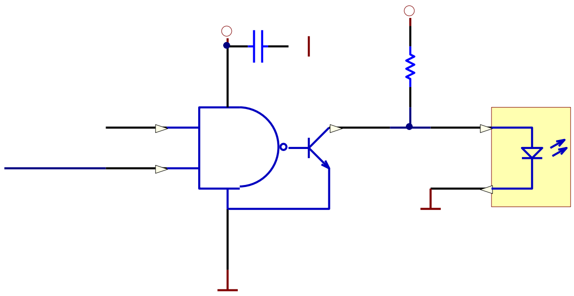


Fig. 10 Transmitter schematic

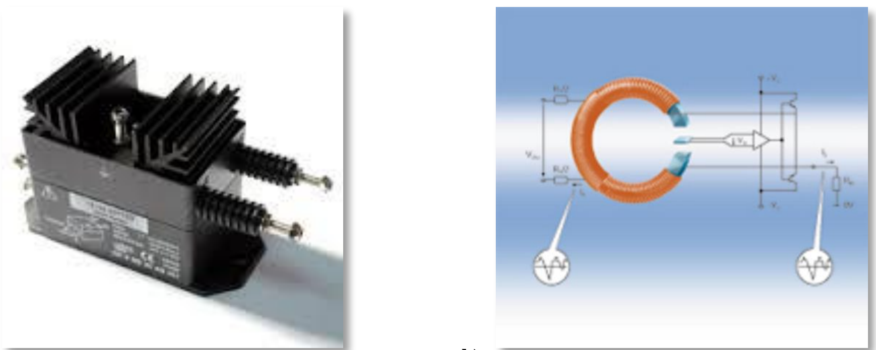
2.8 Filtering stage – A/D acquisition

2.8.1 Sensors used

The control of the machine performed has two different loops: an inner current loop and an outer speed loop. As its control is not going to be sensorless, it is necessary to include some current and voltage sensors and an encoder to feedback to the control the actual measures. Also, the measures reported by the sensors (both current and voltage), serve to the user as a software protection in case of a wrong controlled operation.

2.8.1.1 Voltage sensors

The voltage sensors used were the LV100-3000/SP3 from LEM which are closed loop Hall Effect voltage transducer (Fig. 11, a). The operating principle of the voltage transducer is based on the Hall Effect (Fig. 11, b). A very small current limited by a series resistor is taken from the voltage to be measured and is driven through the primary coil. The magnetic flux created by the primary current IP is balanced by a complementary flux produced by driving a current through the secondary windings. A hall device and associated electronic circuit are used to compensate the secondary current that is an exact representation of the primary voltage.



a) b)

Fig. 11 a) LEM LV100-3000/SP3 voltage transducer; b) Hall effect principle

The primary nominal voltage is 3000V. Hence, when the voltage applied to the primary is 3000V, its output current is 50mA. They achieve a very good linearity between the applied voltage to the primary and the current output on the secondary. The linear relationship can be observed in Fig. 12.

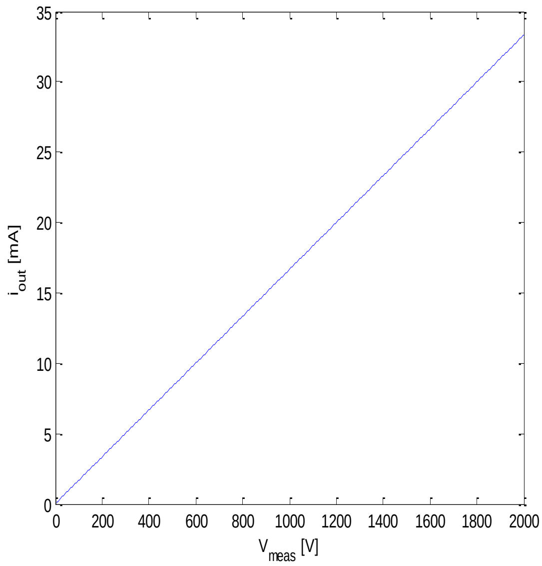
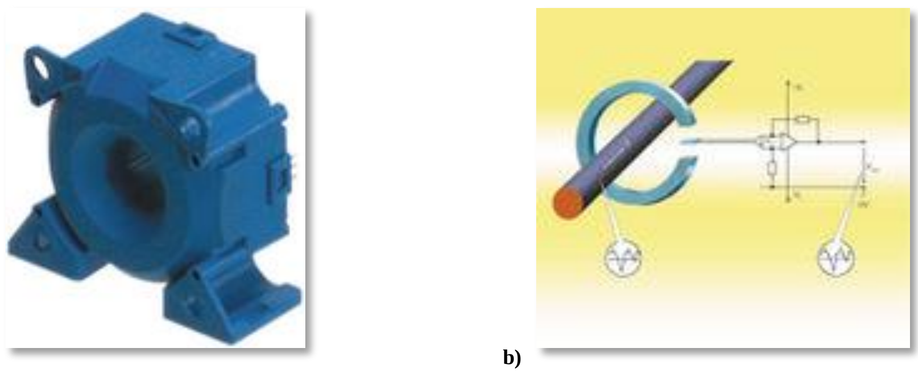


Fig. 12 Voltage sensor V to I transducing curve

2.8.1.2 Current sensors

On the other hand, the current transducers used are the LF305-S from LEM (Fig. 13, a). As in the case of the voltage transducer, they are also a closed loop Hall Effect current transducer (Fig. 13, b). Its operation is the same as the voltage transducer but, instead of apply the voltage to the primary of the transducer, the current flows through its hole inducing a magnetic flux that is compensated by the secondary winding.



a) **b)**

Fig. 13 a) LEM LF305-S current transducer; b) Hall effect principle

In this case, the maximum current that the transducer is capable to measure is 300A. When this current is flowing through the sensor, its output delivers 150mA. Similar to the voltage transducer, a line that relates the sensed current to the output current can be drawn (Fig. 14).

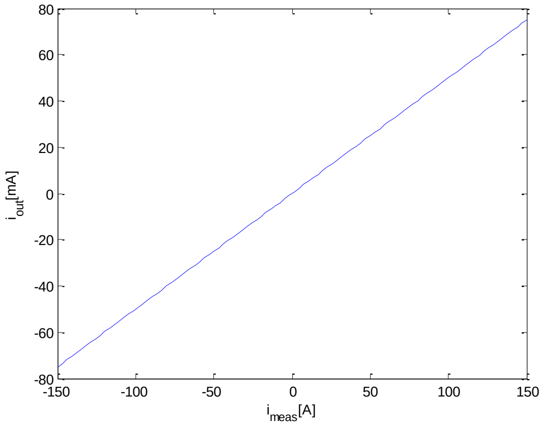


Fig. 14 Current sensor I to I transducing curve

2.8.1.3 Encoder

An encoder is a device that converts the relative movement of the shaft of a machine into electrical pulses. The shaft encoder generates a signal every incremental change in its position. Also, they can be used to measure linear movement.

Inside the device, a line-coded disc made of metal or plastic, attached to the shaft of the encoder interrupts an IR light generated by a transmitter LED which is send to an IR receiver. The higher number of lines the encoder has, the higher its resolution (the encoder used has 1024 lines per revolution, it implies that every step read from the encoder, the shaft has rotated 360/1024=0.35º).

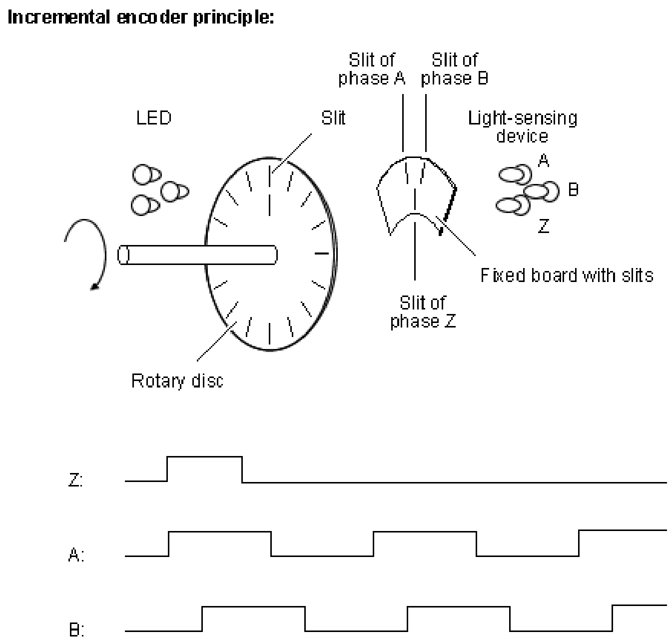


Fig. 15 Incremental encoder operating principle

Every interruption of the IR light made by the lines of the disc means a pulse read by the IR receiver. By means of the built-in circuitry of the encoder, its outputs show a rectangular signal which depends on the frequency of the mechanical rotation of the shaft of the machine (Fig. 15).

2.8.2 Voltage shifting stage

As said, both the voltage and current transducers have a current output. This fact implies that the signals reported by the sensors cannot be read directly by the DSP. In order to surpass this issue, a voltage shifter stage has to be implemented.

Such stage performs two different functions: translate the current output of the sensors into a voltage (just by introducing a measuring series resistor) and shift the previous voltage to the levels suitable for the DSP.

The A/D modules of the DSP are 0 to 3V tolerant. That means the signals generated by the sensors have to be shifted to such range. Also, their measures have to be filtered in order to get the useful information. Filtering stage is studying in the next paragraph.

Fig. 16 shows the voltage shifting stage. The sensors output current is delivered to a series resistor with a value depending on the sensor used.

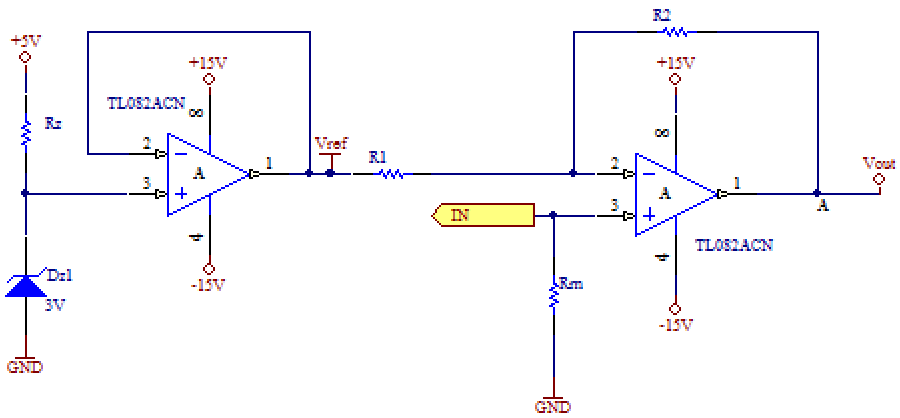


Fig. 16 Voltage shifting stage

The equation of the voltage shifting stage is:

$$V_{out} = \left(1 + \frac{R_2}{R_1}\right) \cdot i_{IN} \cdot R_m - \frac{R_2}{R_1} \cdot V_{ref}$$

The voltage sensors will always measure from 0 to V_{DC} as the sensors are connected in parallel to the bus capacitors. So, as the maximum reading of the voltage sensor is going to be 2000V, the maximum output current is going to be 33.3mA. When the voltage is 0, the current is 0. This makes the output current to be proportional to the voltage measured.

This voltage shifting stage does not inverse the signal, it only introduces a gain and offsets its input signal. The filtering stage connected to the output of this stage does inverse the signal, so the output of the filter results a signal filtered and reversed. To undo the inversion introduced by the filters, the current acquired is inversed by software.

In order to set an output voltage range for the shifting stage from 0 to –3V, its input has to be in the range –1V to 1V, taking into account that the voltage sensor is delivering from 0 to 33.3mA. So, in order to get a V_{IN} equal to 1V when the maximum voltage is read (2000V which equals to 33.3mA), R_m has to be equal to:

$$R_m = \frac{1V}{0.0333A} = 30\Omega$$

For the current sensors, the maximum current they are going to measure will be –150A to +150A. Adopting the same thoughts as in the case of the voltage sensors, the output of the voltage shifting stage has to be in the range of –1V to 1V.

When the sensor is reading its nominal current (–150A and +150A), the current that is delivering on its output the current transducer is -75mA and +75mA. Performing the same operation as for the case of the voltage transducer, the series measuring resistor is:

$$R_m = \frac{1V}{0.075A} = 13.3\Omega$$

2.8.3 Filtering stage

However, the sensors do not give clean signals since they are located in an electrical noisy environment. Their signals are contaminated by the switching of the transistors, ground loops, EMI radiation, etc. In order to get cleaner signals and to adequate their levels to the ones tolerated by the A/D modules of the DSP, both filter and voltage shifting stages are needed to perform such signal conditioning.

In order to ensure the correct acquisition of the A/D, not only a voltage shifting stage is needed but also a filtering stage. In the next paragraphs, the filter stage, its dimensioning and implementation are explained in detail.

2.8.3.1 Active Filter topologies

Although many topologies are widely used to filter signals, this work will only focus on the most common topologies. They are: Butterworth, Chebyshev and Bessel (Multiple Feedback).

For the application that this work is thought, the filter which is going to be used is a low pass filter. The reason is that the main noise the filter has to avoid is the one coming from the switching of the transistors. The useful information for the A/D conversion is related to the main frequency of the currents (50Hz) and so, any component above that value should be removed.

2.8.3.1.1. Butterworth topology

The Butterworth is probably the best-known filter topology. This topology exhibits a nearly flat passband with almost no ripple. Its rolloff is smooth and monotonic. It has a low-pass rolloff rate of 20dB/decade for every pole. In the case of the filter finally used, only one pole.

The general equation for a Butterworth filter's is:

$$H(\omega) = \frac{1}{1 + \left(\frac{\omega}{\omega_0}\right)^{2n}}$$

where n is the order of the filter, can be any positive whole number (1, 2, 3...).

Fig. 17 shows the amplitude response curves for Butterworth low-pass filters of various orders.

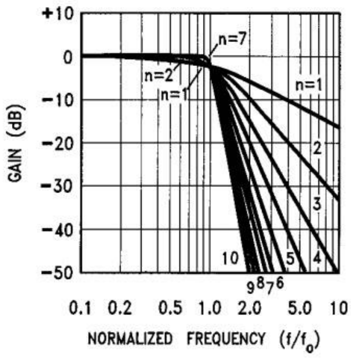


Fig. 17 Amplitude response curves. Butterworth topology

However, the main disadvantage of the Butterworth topology is that it has a wide transition region (choosing n=1) when switching from the pass band to the stop band.

2.8.3.1.2. Chebyshev topology

The Chebyshev topology achieves ripple in the pass band amplitude response. When defining the Chebyshev filter, such amount of allowed ripple is one of the parameters to be taken into account.

This topology has a steeper rolloff than the Butterworth near the cutoff frequency. However its monotonicity lower than the Butterworth achieves and furthermore it has a poorer transient response.

Fig. 18 (a) shows a step response (the higher the order, the higher the overshoot). Fig. 18 (b) shows the amplitude response versus the normalized frequency.

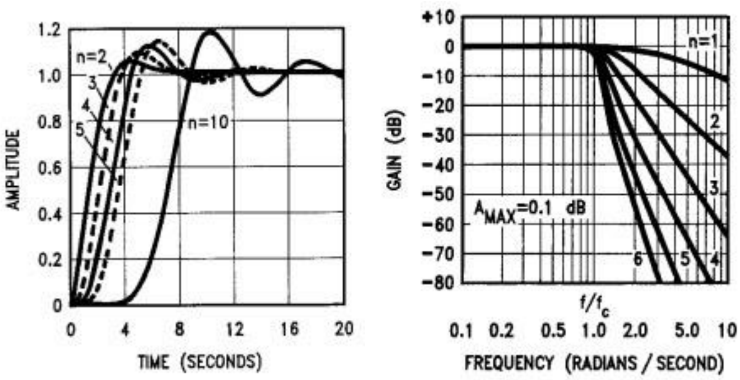


Fig. 18 (a) Chebyshev filter step responses; (b) Amplitude response. Chebyshev filter

2.8.3.1.3. Multiple Feedback Bessel (MFB)

The main advantage of the Bessel (or Thompson) filter is that the phase shift is approximately linear with frequency. This results in the action of the filter to be as a low pass filter with a delay. The higher the filter order, the more linear the phase response.

Also, the characteristics of the Bessel filter are that the overshoot and the ripple when a step is introduced in the filter is lower than the experimented by the Chebyshev topology. The amplitude response of the MFB is monotonic and smooth (Fig. 19), but its rolloff is lower compared to Butterworth or Chebyshev (n=1).

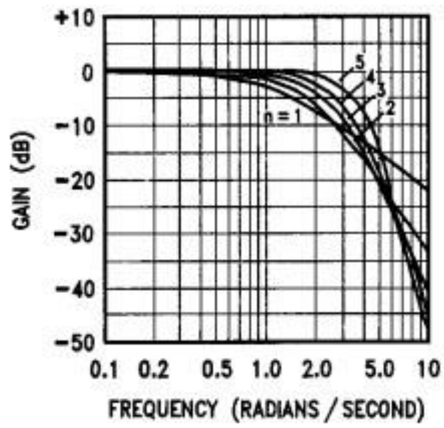


Fig. 19 MFB amplitude response

The MFB filter is widely used in high dynamic range ADC input stages. This topology of filters offers very good stop band rejection over the former filter topologies described [5].

The topology selected for the filters is shown in Fig. 20. The design is an inverting signal path, second order MFB low pass filter. Also, to set an additional protection measure, a zener diode (V_z=3V) is placed. In case the output of the filter exceeds a voltage of 3V, it will conduct current setting the output of the filter equal to 3V.

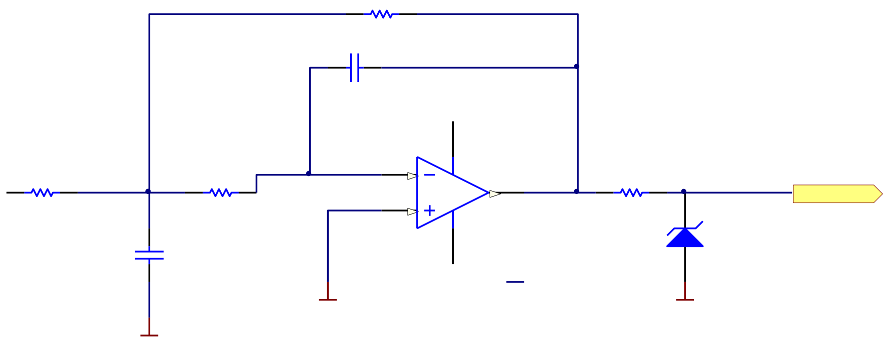


Fig. 20 MFB used filter

The cutoff frequency of the filter is given by the relationship:

$$f_c = \frac{1}{2 \cdot \pi \cdot \sqrt{R_6 R_5 C_1 C_2}}$$

With the values shown in Fig. 13, the cutoff frequency results 1kHz.

The gain of the filter is [6]:

$$AvDC = -\frac{R_6}{R_4} = -1$$

To separate the digital ground plane from the analog ground plane both planes are attached each one by only specific locations (Fig. 21). The path is only a trace that acts as impedance to high frequency noise coming from the digital part of the circuit disturbing the A/D acquisition.

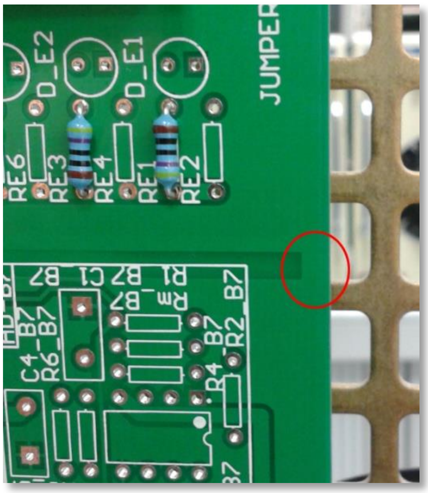


Fig. 21 Analog and Digital Grounds union

2.9 Encoder signal reception

In order to avoid EMI noises induced in the wiring coming from the encoder, the encoder used (Heidenhain ERN430), gives the possibility to use differential wiring. The differential wiring implies to use two wires for each signal sending the signal and their opposite (Fig. 22).

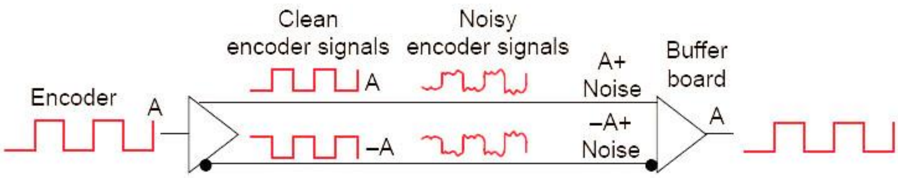


Fig. 22 Encoder differential signaling

When the noise is induced in the wiring (they are twisted-pair cables), the same noise in induced in both the signals (A and Ā). When the receiving end gets the signals, the differential signaling allows removing the noisy component reading the clean signal sent by the encoder.

The differential receiving stage is shown in Fig. 23. The architecture is termed as AC Termination. It receives such a name because the termination resistor (R_t) allows the current to flow from the high-state to the low-state. The fact of include a capacitor, eliminates the DC current path from one differential signal to the other.

However, this included RC impedance introduces in the circuitry a delay depending on the time constant which may reduce the transmission speed. But, as the motor is not going to run at a very high speed, the data rate capability of the receiving stage is far away from the encoder data rate.

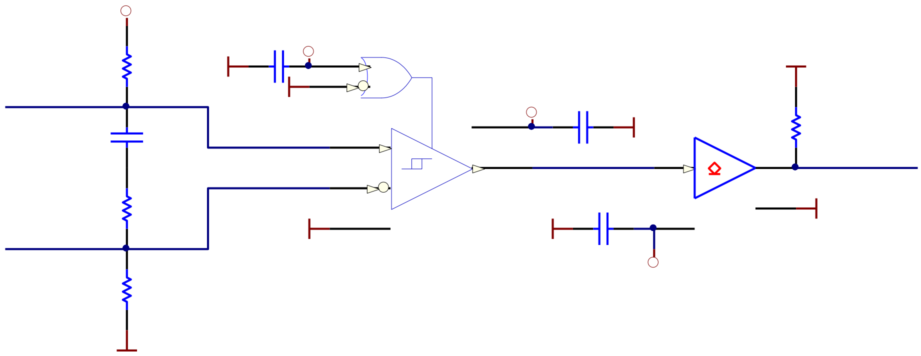


Fig. 23 Differential AC termination

The selected differential receiver IC is the 26LS32AMS from Texas Instruments. It has a +5V voltage supply. The encoder has to be fed with +15V but as its output stage is a TTL, the output voltage signals are set by the differential amplifier.

The differential amplifier sets an output changing from 0V to +5V which is not a value tolerated by the DSP (3.3V) so a voltage shifting buffer stage is needed. As in the previous cases, the selected voltage shifter is the SN74LS07N from Texas Instruments. It is a buffer with an open collector output stage. By using a pull-up resistor connected to the 3.3V rail, the output can be connected to the inputs of the encoder modules of the DSP.

2.10 SCI and SPI communication modules

The DSP implements two different communication modules: SCI (Serial Communication Interface) to send serial data (for example to the PC) and SPI (Serial Peripheral Interface) to communicate with other slave devices.

As the project implemented is not going to use such a connections, the final implementation was only focused in make their connections accessible. In order to use them, the user only has to implement new modules (with the adequate ICs) which can be connected directly to the connectors.

Fig. 24 shows in detail the connectors and its physical implementation in the interface board.

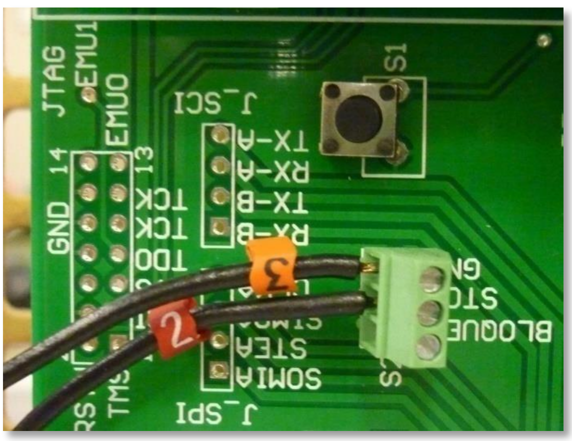


Fig. 24 SCI, SPI and JTAG connections

2.11 GPIO ports

In order to give the interface board functionality beyond of the control of the NPC inverter, the board has also, easily accessible a connector to use the general purpose input-output.

This module implements only a connector which can be used for external triggers, manage digital signals, block the gates pulses by software, etc. Fig. 25 shows the accessible connector for the GPIO ports.

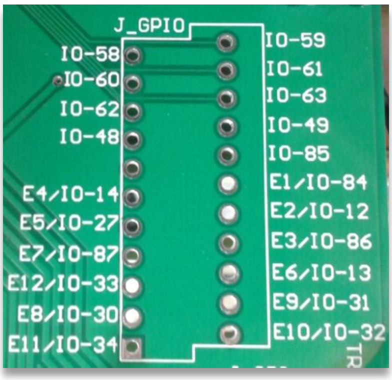


Fig. 25 GPIO connector footprint

2.12 Power stage

The interface board has four voltage rails. They are 3.3V for the DSP input signals, 5V for all the IC present in the circuit (latch, logical gates, transmitters and receivers, line drivers, differential receivers, etc.). Additionally, the operational amplifiers need two voltage rails composed by +15V and –15V to be correctly polarized.

The power stage makes profit of switched power supplies with the exact values needed for feed up the board. Hence, the power supply used has been the ECM60UT33 from XP Power that has enough power to supply correctly the entire board. Such a power supply has 3 different voltage rails: +5V, +15V and –15V. They can be connected directly to the power rails of the board.

In order to generate the 3.3V level, a low dropout voltage regulator (LDO) has been used. It receives power from the +5V rail and by means of a linear regulation, sets an output of 3.3V. This voltage level is ready to be used to adapt the error signal voltage level to a suitable level for the DSP.

In order to avoid noise effects, to provide current peaks and establish a constant voltage, three 1000µF/35V capacitors are located near the pluggable power connector between all the three voltage rails and the digital ground.

2.13 DSP board

As said, the microcontroller to be used is the TMS320F28335. As the building of a PCB board was physically too complicated to solder the microcontroller to a customized PCB, the solution adopted was to use a commercial daughter board released by Texas Instruments.

The board finally used was the TMDSCNCD28335. Such a control card implements a low pass filter stage, isolated RS-232 communication, several I/O ports or JTAG emulation.

Fig. 26 shows the card used to control the inverter. The card is connected to the interface board using a 100 pin memory socket.

Fig. 26 TMDSCNCD28335 card connected to the interface board

Chapter 3

Experimental setup

In addition to the hardware designed previously, some commercial devices have been used. This way, the work can be only focused in the control part of the system (hardware and software). The power devices used in the project are explained following.

Fig. 27 shows the laboratory experimental setup.

Fig. 27 Laboratory setup overview

3.1 Medium Voltage induction machine

The selected electric motor has been a M2QA225M2A from ABB motors (Fig. 28). It is a medium voltage induction machine that is capable to be fed up with 1.5kV ph-ph in star connection.

Fig. 28 Medium voltage induction machine

Its ratings are shown in the next table:

Parameter	Value
Vph-ph star connection	690V
Frequency	50Hz
Power	45kW
rpm	2970
Maximum current	45.69A
cos(φ)	0.89
Pole	2

Table 2 Induction machine ratings

An encoder Heidenhain ERN430 has been used. It has been attached to the rear part of its shaft by using a flexible coupling (Fig. 29).

Fig. 29 Encoder attached to the shaft of the machine

3.2 NPC Inverter

The NPC inverter used for the power stage part has been a customized NPC inverter manufactured by ELINSA. ELINSA is a Spanish company that designs, tests and manufactures all kind of electronic equipment in several areas such as marine, renewable energies and industrial sector.

The power ratings of the inverter are shown in the table below:

Parameter	Value
Maximum Current	36ADC
Maximum Voltage	4kV
Levels	3
Topology	NPC
Protection level	IP23
Isolation voltage level	6kV

Table 3 NPC inverter ratings

Fig. 30 shows in detail the power stage of the inverter.

Fig. 30 NPC inverter power stage

3.3 Power Supply

The machine is fed by a medium voltage power. The one selected for the work has been a MTD4000-36 from Magna-Power Electronics (Fig. 31).

Fig. 31 DC Power Supply

Its main parameters are shown in the table below:

Parameter	Value
Maximum DC output voltage	4000VDC
Maximum DC output current	36ADC
Maximum power	150kW
cos(φ)	0.92

Table 4 High Voltage power supply parameters

Chapter 4

Control implementation

In this chapter, the control of the machine is studied. In the first section, the control implementation is detailed, explaining both the speed and the current loops. In the second section of this chapter, the software algorithm is explained.

4.1 Control implementation

A speed control has been implemented. Basically, the control performed implements two different loops: an outer speed control loop which sets the mechanical speed of the machine and an inner current control loop which controls the current that flows to the load.

Fig. 32 shows the control block diagram. In the figure, a classical speed control is implemented. The outer control loop which sets the rotor speed of the machine takes a reference given by the user. Such a reference is compared with the mechanical speed of the machine (read from the encoder) to extract the error among both magnitudes.

The error, as usual, is connected to the input of a PI controller, generating the current vector which will be injected into the machine (I_q). The equation below shows the PI regulator implemented for all the controllers:

$$G(s) = K_p \cdot \left(1 + \frac{K_i}{s}\right)$$

Such a current, as in the case of the speed control, is compared by means of a subtraction with the measured currents. This operation sets the deviation between the reference current and the measured one. The error is the input of the PI current controller, which will give the q-axis voltage reference component that the inverter will generate.

As the d-axis component of the current is needed only to magnetize the machine, there is no speed control action in this component. Only a current control loop is needed. Both the d and q-axis components of the current are controlled using the same parameters for the PI controllers.

On the other hand, the q-axis component of the current will generate the necessary torque (a small one since the machine is working at no load condition) to rotate the machine.

The tuning of the PI controllers has been done taking in account the estimated parameters of the machine and studying the response of the machine to a step in its speed reference.

Finally, the calculation of the duty cycles to be applied to the power switches has to be done by applying a dq to abc transformation. The mechanical angle estimated is used to carry out such a transformation. As the actual mechanical speed of the machine is known (by reading the encoder), its angle is known just by integrating its value every acquisition.

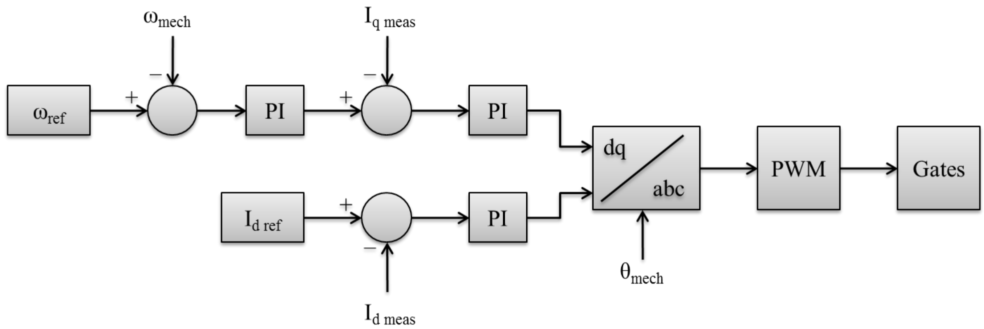


Fig. 32 Implemented control strategy

The parameters finally used for the PI controllers are shown in the Table 5.

Parameter	Value
Speed control P constant (q-axis)	0.01
Speed control I constant (q-axis)	0.3
Current control P constant (both dq axis)	1.5
Current control I constant (both dq-axis)	40

Table 5 Parameters chosen for the regulators

4.2 Software routines

To implement the previous control, a few software routines have been implemented. The entire source code developed can be read in Annex I.

The block diagram shown in Fig. 33 explains the way of operation of the implemented control software. The DSP (after the initialization of all the variables and required modules of the DSP) is running in an idle situation where any instruction is being executed. All the control of the machine is done using interruptions.

As the A/D acquisition can be started triggered by any event, the selected event has been the PWM. Every time the event is triggered by the PWM module, a start of conversion (SOC) is launched. The functionality is provided by the DSP itself that facilitates the development of the A/D acquisition. A/D channels calibration is not detailed in this work. It can be further studied in [7].

Also, as the PWM frequency does not vary any time of the program, the A/D samples are constant through the time, performing an easier discrete control.

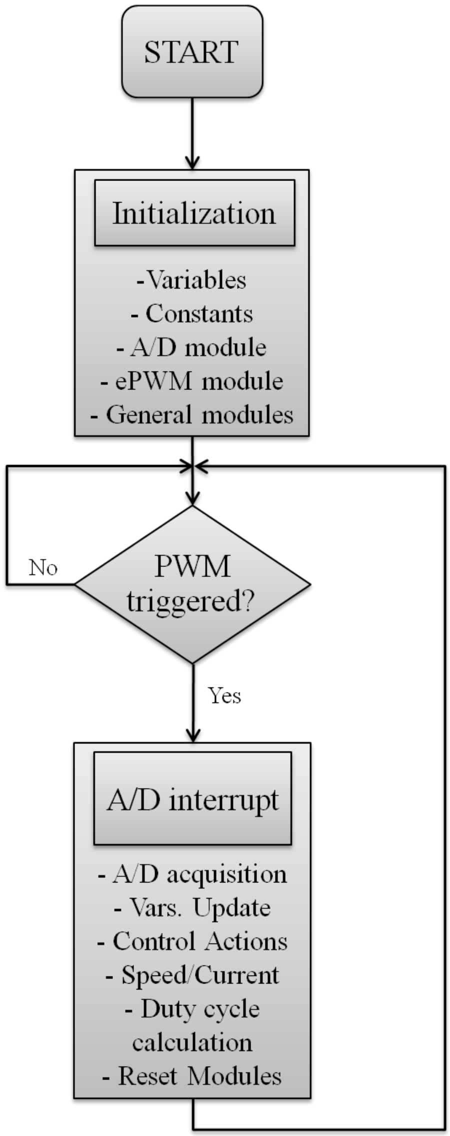


Fig. 33 Implemented control code block diagram

Chapter 5

Experimental Results

In this chapter, the experimental operation of the entire system is demonstrated. Several figures will show the function of the inverter studying the signals of the system. Also, the main signals of one switch of the NPC inverter are presented in order to study its operation.

5.1 Power switches signals

To study the correct operation of the NPC inverter, only one switch will be studied. The most representative voltages of a power transistor are: gate-emitter voltage (V_{GE}), collector-emitter voltage (V_{CE}).

Fig. 34 shows the voltage signals mentioned. When V_{GE} is positive (+15V), the transistors turns on, becomes to conduct current and the V_{CE} is only related to the saturation of the transistor (2.8V). On the other hand, when the V_{GE} is negative (–15V) the transistor is turned off and the current lows to zero, and the V_{CE} is 0 or $V_{DC}/2$ depending on the state of the other switches.

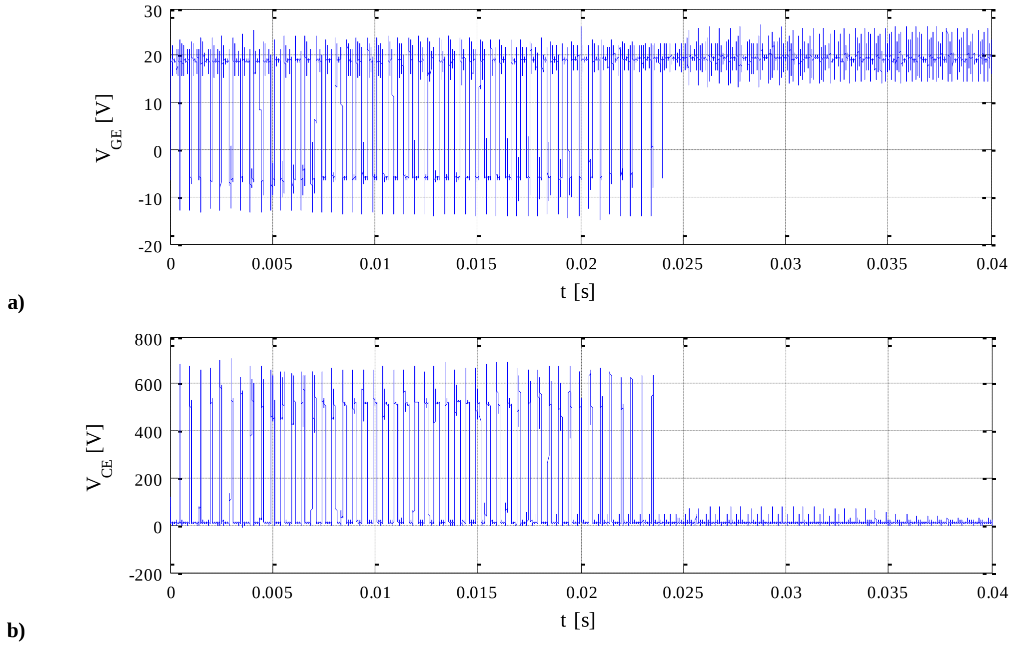
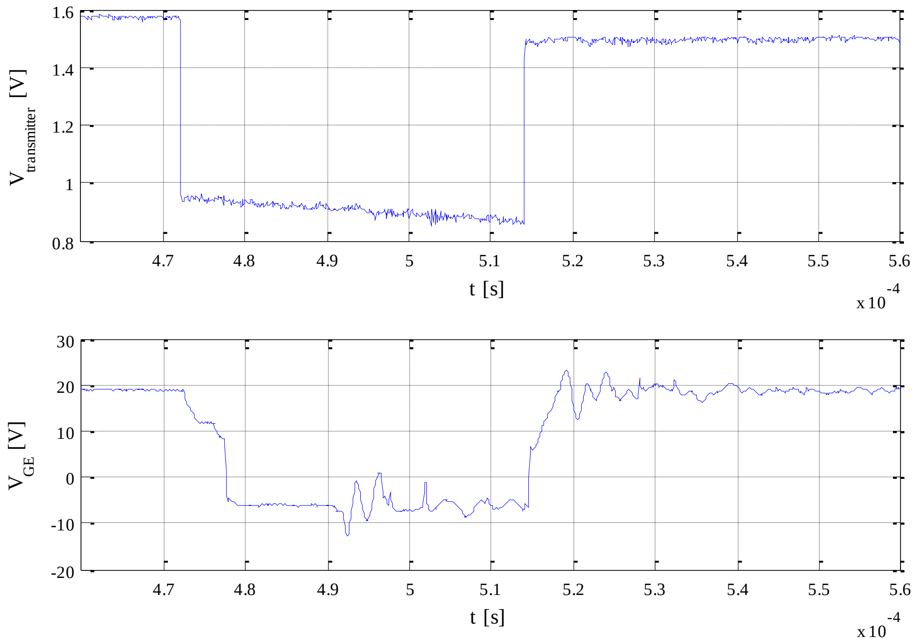


Fig. 34 a) PWM applied to the gates; b) CE Voltage withstood by the transistor

A soft switching technique implemented automatically by the driver called active clamping can be observed (Fig. 35). The driver turns off the transistor by setting the gate voltage to an intermediate level. This behaviour lowers the voltage stress that the switches have to support when the turning off takes place.



a)

b)

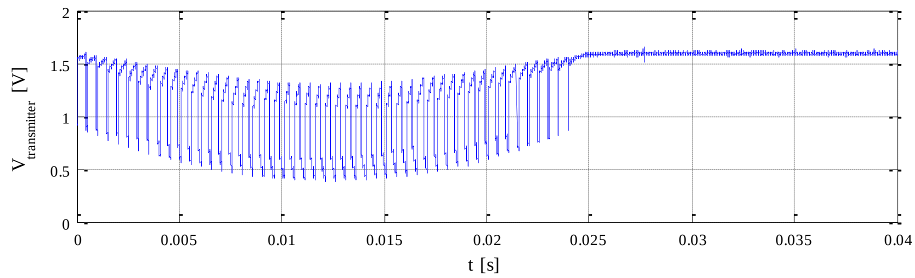
Fig. 35 Turning OFF and ON: Transmitters (a); Gates (b)

5.2 Board signals

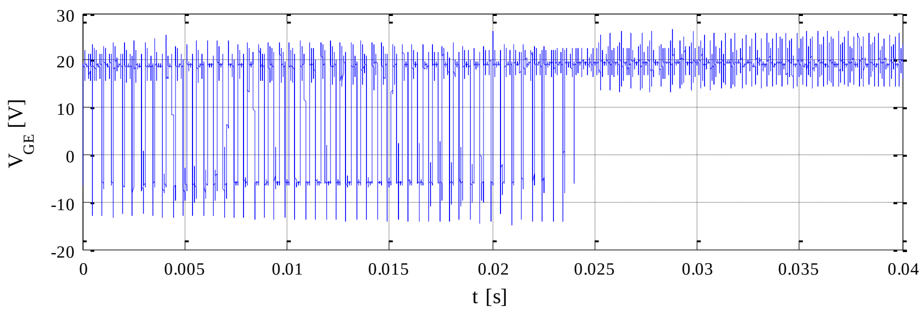
The interface board implements several modules, however, some of the modules implemented were not used, so a few signals are going to be studied in this section. The most important signals are: PWM, errors, filtering stage and encoder signals.

5.2.1 PWM signals

The PWM signals are related to the control of the switches themselves. Fig. 36 a) the PWM waveform sent by the transmitter for one of the switches (not all the signals are studied since they all are analogue) while Fig. 36 b) shows the gate voltage applied to the transistor. The variation of the duty cycle in order to generate the correct voltage can be observed clearly.



a)



b)

Fig. 36 a) PWM signals transmitters; b) Gates

The PWM waveform of Fig. 36 a) has been read in the point that the red circle in Fig. 37 indicates. Such waveform is due to the combined capacitance of the transmitter itself and the one introduced by the line driver.

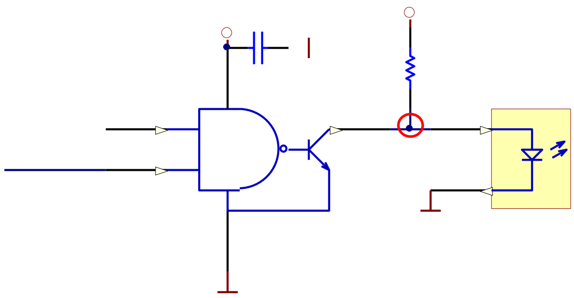
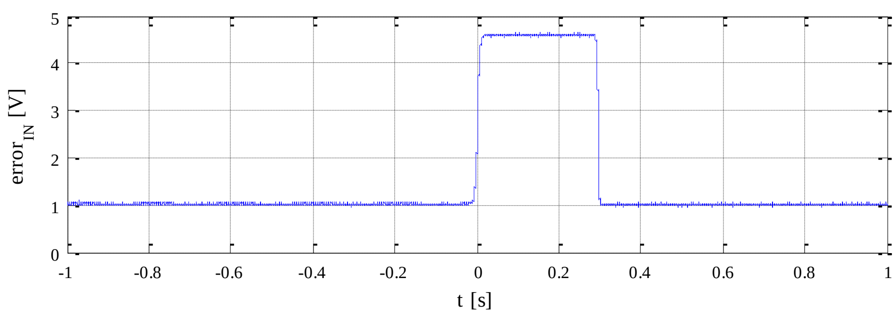


Fig. 37 Point of transmitter PWM reading

5.2.2 Error signals

An error has been simulated to demonstrate the correct operation of the error management part. As the Fig. 38 shows, the error signal remains at low level (Fig. 38, a) and when the error occurs, its rising lows the STOP signal to the low level (Fig. 38, b). This causes in the gates to put a logic zero on their outputs and the PWM are blocked down (Fig. 38, c).

When the reset button is pressed, the PWM signals are allowed to be sent to the transmitters operating in a normal situation (not shown in the figure).



a)

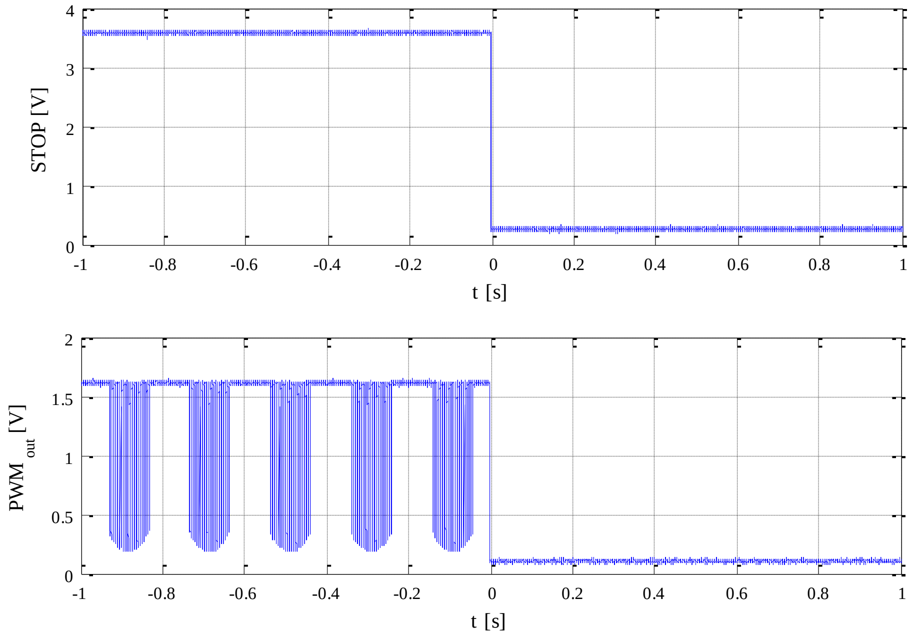


Fig. 38 Error signal (a); STOP signal (b); PWM signal (c)

5.2.3 Filtering stage

Filtering stage is one of the most important modules implemented in the board. Fig. 39 shows the current before and after the filtering stage. As the switching frequency is set to 2kHz, and the filtering stage has its cutoff frequency equal to 1kHz, the effect of the filter is to remove components with frequency more than such 1kHz. Also, the offset in order to achieve the supported values of the DSP can be observed (signals stands between 0 and 3V all the time).

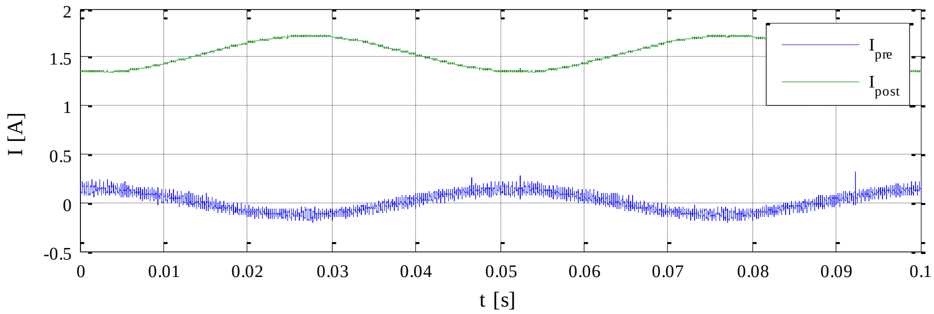


Fig. 39 Post filtered current (green); Prefiltered current (blue)

5.2.4 Encoder signals

The encoder is a device that provides three signals (A, B and I), but only A and B are used in this work. Fig. 40 shows the signals at the output of the encoder (A, $\overline{A}$, B and $\overline{B}$), the signals received by the differential receiver and the single signals got at the output of the differential receiver.

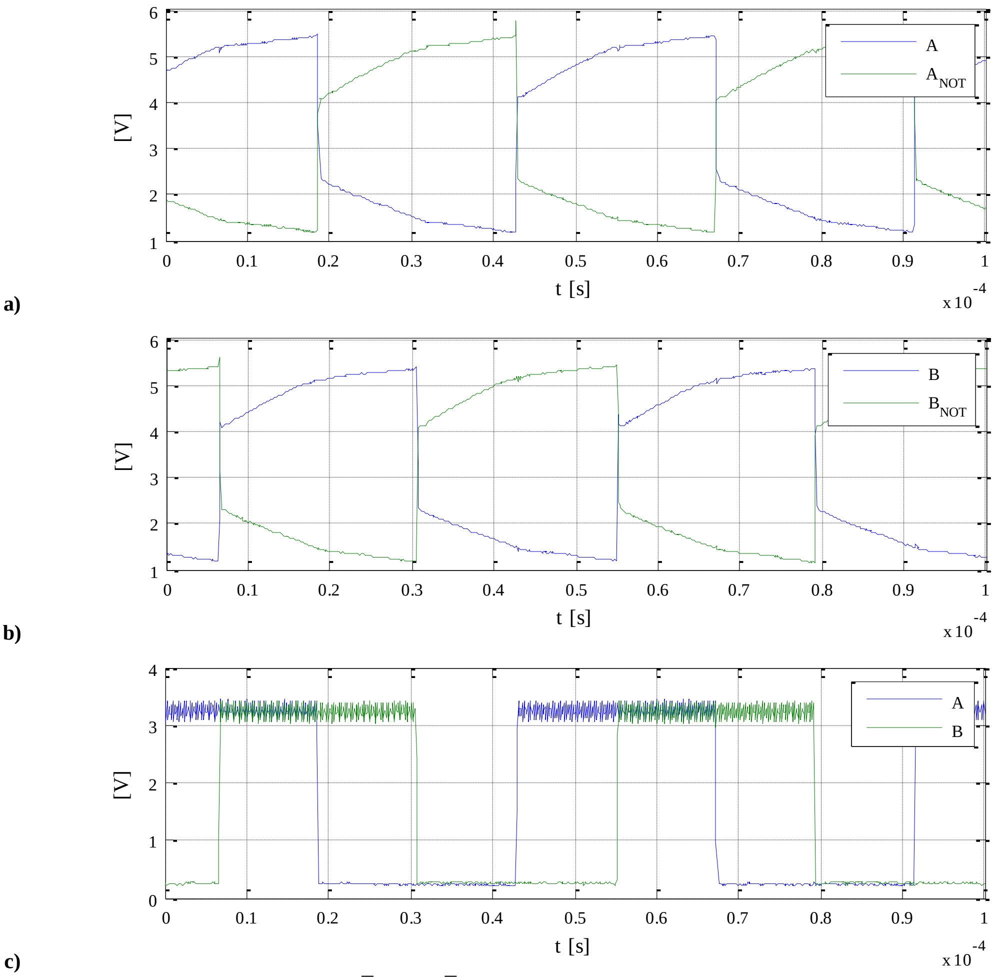


Fig. 40 A, $\overline{A}$ (a); B, $\overline{B}$ (b); A and B outputs (blue and green, c)

5.2.5 Speed control

To verify the correct operation of the speed control, the speed of the machine has been saved and analysed. Fig. 41shows the evolution of the machine speed when a step like change of 20Hz has been applied at t=5s. As it is observed the steady state is reached in less than 50 seconds.

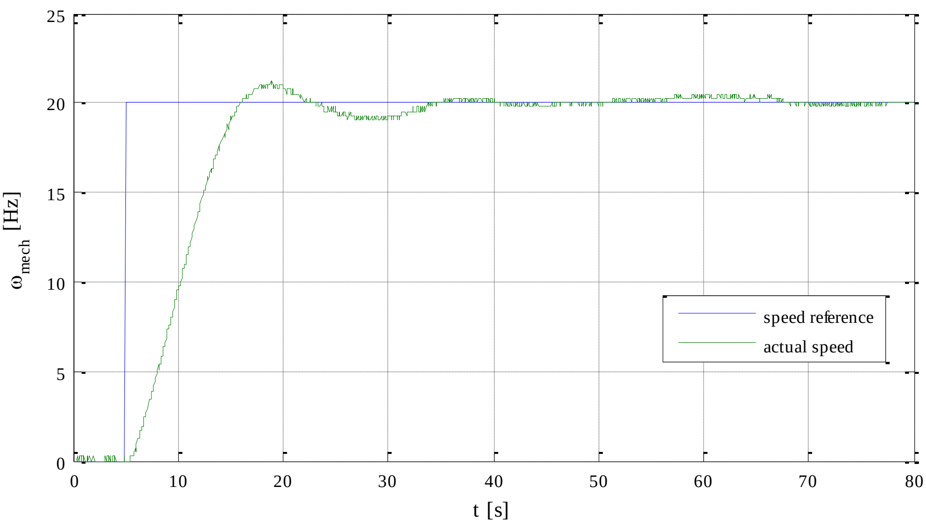


Fig. 41 Reference speed (blue); Actual speed (green)

Chapter 6

Conclusions and further improvements

The work developed in this thesis covers the start-up of a custom commercial NPC multilevel inverter, the design and building of the interface board and the implementation and debugging of the software routines to perform a closed-loop speed control of a high voltage induction machine.

The thesis focussed on the first tests using a commercial power devices to verify the correct operation of the algorithms. Actually the algorithms are working properly so the next step of the project will be to build a NPC multilevel inverter using discrete SiC power transistors to compare the operation of the commercial devices versus the SiC ones.

Although the power supply is able to deliver up to 4kV, the machines in the laboratory were not able to support more than 1.5kV in safety conditions. Hence, to avoid hazardous situations, the maximum voltage used to feed the machine was 1kV. Also, the inverter has some snubber capacitors which causes in the internal circuits to reflow huge amount of currents rising the temperature of all the power switches and bars.

More machines with higher voltage capability are located in other laboratory. However, due to their size, they could not be moved to the same laboratory that the used equipment was. Such machines are going to be used to rise the bus voltage to 4kV.

The first version of the interface board designed has many features that allow the user to make profit of all the powerful characteristics of the DSP.

However, as in all first prototypes, it has some mistakes that should be reviewed and rethought. Mainly, the design lacks of built-in standard modules as RS-232, or SPI. These modules can be built separately but, in order to ensure a better mechanical fixation, the modules should be implemented inside the board. As all the functionalities were implemented in a modular way, it can be used or not whether the application needs it without affecting the operation of the rest of the modules.

This first prototype has been designed using through hole ICs and passive components. If the IC´s used were SMD technology, the board could be smaller.

The LED connected to each one of the error channels have the drawback of blinking for a while (typically milliseconds) while the error is being triggered, but the error signal coming from the driver disappears and hence the LED turns off. Hence, the effect is that no error can be observed. To surpass this issue, there are two different solutions depending on the information that the user wants to know:

- Remove the entire individual error LED and maintain only the one attached to the latch: This fact allows to reduce the complexity of the board and its associated cost.
- Include a latch for every LED: This solution gives to the user better information on where the error has occurred and what switched has caused it. The major drawback of this solution is that the components needed to implement such new functionality is that its associated cost and the complexity of the board.

In order to use a cheaper power supply and improve the overall efficiency of the power stage, a DC/DC converter can be implemented to generate +15V, –15V and 3.3V starting from a +5V single channel power supply.

Related to the control of the machine, the next step in the algorithm is to remove the encoder (which caused a lot of troubles in the very beginning because of its mechanical attachment) and to develop a sensorless control.

Also, a GUI could be developed in order to extract some parameters from the memory of the DSP since its memory map is not so large. Also, such a GUI could be used to extract real-time data from the DSP.

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Annex I: Source Code

```
#include "MW_Circ_v2.h"
#include "RN_174.h"
#include "Constants.h"
#include "DataStorage.h"
#include "FilterAndRotations.h"
#include "QDOperations.h"
#include "Utils.h"
#include "qep.h"

#define Imax            80
#define Vbusmax  1000

#define vel_ref         5       //Speed reference (Hz)
#define Kp              1.5
#define Ki              40

#define Kp_v            0.01
#define Ki_v            0.3

#define DTF             (0.0005)
#define DT              (_IQ(DTF))      // sampling rate
#define DTDIV2  (_IQ(DTF/2))
#define INVDT           (_IQ(1/DTF))

// this machine #defines
#define ENCODER_LINES  1024
#define POLE_PAIRS              1
#define T_QEP                   1000//1000

const _iq Rs = _IQ(0.6);                // stator resistance (Ohm)
const _iq Rr = _IQ(0.022);              // rotor resistance (Ohm)
const _iq Lm = _IQ(0.03317);                    // magnetizing inductance (H)
const _iq Lls = _IQ(0.0022);            // stator leakage inductance (H)
const _iq tau_r = _IQ(1.6);             // rotor time constant (s)

// Prototype statements for functions found within this file.
void delay_loop(long);
void Configure_RN174 (void);

extern void InitFlash(void);
extern void InitAdc(void);
extern void InitPieCtrl(void);
extern void InitPieVectTable(void);
extern void InitSysCtrl(void);

extern unsigned int RamfuncsLoadStart;
extern unsigned int RamfuncsLoadEnd;
extern unsigned int RamfuncsRunStart;

interrupt void adc_isr(void);  // ADC  End of Sequence ISR
interrupt void cpu_timer0_isr(void); //Timer0 Interrupt Service

// Global Variables
volatile _iq ia, ib, ic, vbus_top, vbus_bot;

volatile _iq vas, vbs, vcs, vu_ref, vv_ref, vw_ref, D_top_u, D_bot_u, D_top_v, D_bot_v, D_top_w, D_bot_w;
volatile _iq m = _IQ(0.8);
volatile _iq t = 0;
```

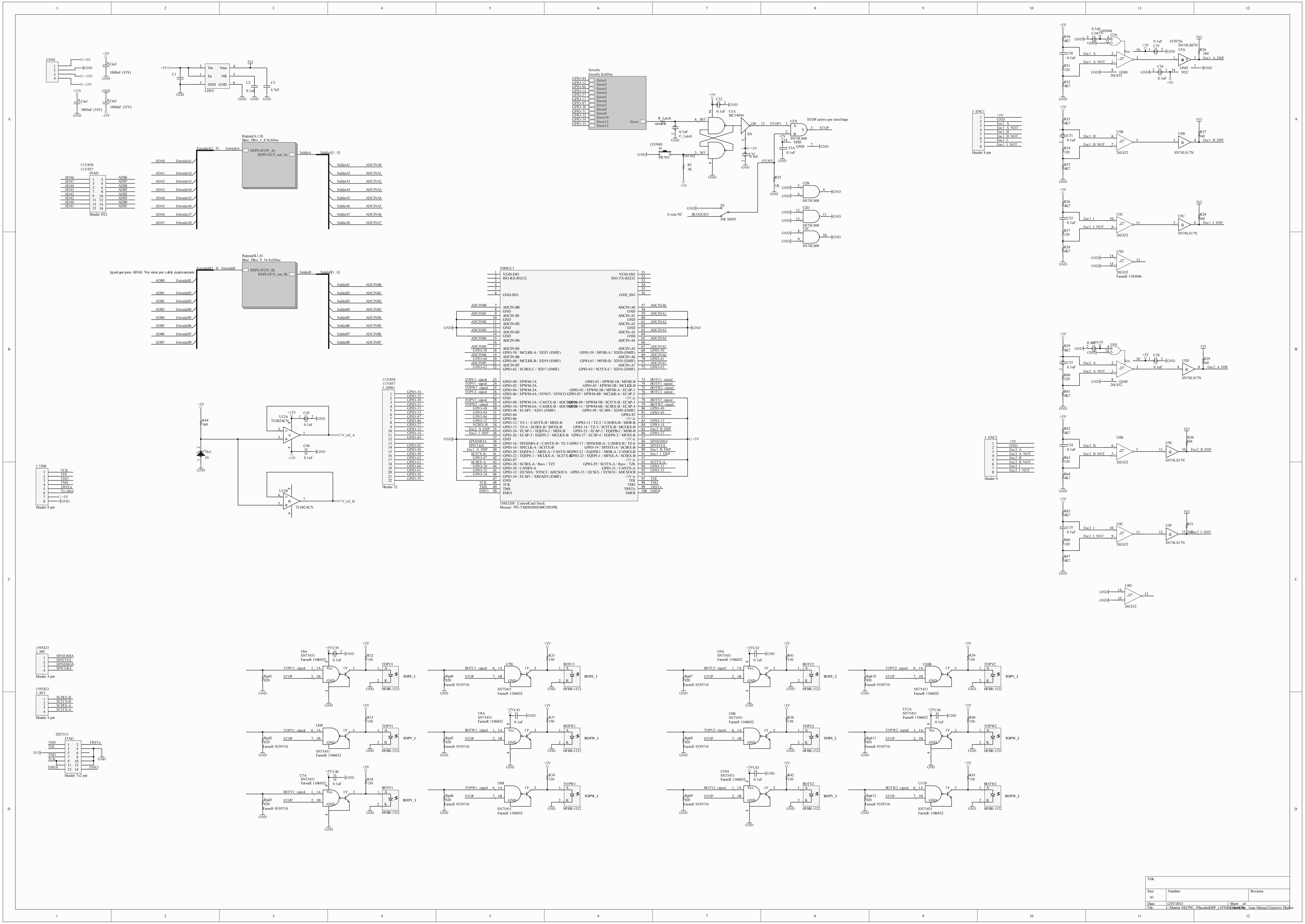
```
volatile _iq phi = 0;
volatile _iq dphi = _IQ(2*3.1416*50*1e-4);
const _iq desfase = _IQ(2.094395102393195);

//Current regulator
volatile struct sqddata idqe_ref ; //reference current vector in stationary reference frame
volatile struct sqddata idqs; //current vector
volatile struct sqddata idqe; //current vector
volatile struct qddata err_idqe; //current regulator error
volatile struct qddata vdqs; //voltage vector in stationary reference frame
volatile struct qddata vdqe; //current vector
volatile data w_flux_hat; //
volatile data theta_flux_hat; //
volatile data w_elec;              //
_iq Kp_current = _IQ(Kp);//_IQ(193.8);//_IQ(55);
_iq Ki_current = _IQ(Ki);//_IQ(5); //constantes del regulador de corriente
_iq Fref_iq = _IQ(Fref);

//Speed regulator
volatile _iq w_refhz = _IQ(vel_ref);
volatile _iq w_ref = _IQ(vel_ref*6.28318530717959);
volatile data error_w;
volatile data T_ref;
volatile data phase_rotor;
_iq Kp_vel = _IQ(Kp_v);//_IQ(193.8);//_IQ(55);
_iq Ki_vel = _IQ(Ki_v);//_IQ(5); //constantes del regulador de corriente
volatile _iq w_hz = _IQ(0.0);

//FAILSAFE PROTECTIONS
int fallo_bus = 0;
int fallo_i = 0;

//###########################################################################
//                                                          main code
//###########################################################################
void main(void)
{

        idqe_ref.d = _IQ(0.0);
        idqe_ref.q = _IQ(0.0);
        INIT_QDDATA(vdqe);
        INIT_QDDATA(err_idqe);
        INIT_DATA(w_flux_hat);
        INIT_DATA(w_elec);
        INIT_DATA(error_w);
        INIT_DATA(T_ref);
        INIT_DATA(phase_rotor);
        INIT_DATA(theta_flux_hat);
        InitSystem();                   // Basic Core Initialization

        memcpy(&RamfuncsRunStart, &RamfuncsLoadStart, &RamfuncsLoadEnd - &RamfuncsLoadStart);

        InitFlash();

        DINT;                                   // Disable all interrupts
        Gpio_config();
        InitPieCtrl();                  // basic setup of PIE table; from DSP2833x_PieCtrl.c
        InitPieVectTable();// default ISR's in PIE
        EALLOW;
        PieVectTable.ADCINT = &adc_isr;
        EDIS;

        InitAdc();                              // Basic ADC setup, incl. calibration

        Setup_ADC();

        //EQEP CONFIGURATION
```

```
	ConfigureQEP1(0/*QEP1Interrupt*/, T_QEP, PCRM_MAX_POS, ENCODER_LINES, POLE_PAIRS);

	PieCtrlRegs.PIEIER1.bit.INTx6 = 1;		// ADC

	IER |=1;

	EINT;
	ERTM;

	EnableQEP1();

	EALLOW;

	while(1)
	{
		asm(" IDLE");
	}
}

interrupt void  adc_isr(void)
{

	//A/D acquisitions
	ia = _IQmpy(((long)AdcMirror.ADCRESULT0)<<GLOBAL_Q,GAINA0)+OFFSETA0;
	ib = _IQmpy(((long)AdcMirror.ADCRESULT3)<<GLOBAL_Q,GAINB0)+OFFSETB0;
	ic = _IQmpy(((long)AdcMirror.ADCRESULT2)<<GLOBAL_Q,GAINB2)+OFFSETB2;
	vbus_top = _IQmpy(((long)AdcMirror.ADCRESULT4)<<GLOBAL_Q,GAINB1)+OFFSETB1;
	vbus_bot = _IQmpy(((long)AdcMirror.ADCRESULT1)<<GLOBAL_Q,GAINA1)+OFFSETA1;

	ia = _IQmpy(ia,_IQ(-1.0));
	ib = _IQmpy(ib,_IQ(-1.0));
	ic = _IQmpy(ic,_IQ(-1.0));

	QEP1VelocityAndPosition();

	//Overcurrent protection
	if (_IQabs(ia) >= _IQ(Imax) || _IQabs(ib) >= _IQ(Imax) || _IQabs(ic) >= _IQ(Imax))
	{
		ModulationOFF();
		fallo_i = 1;
	}

	//Overvoltage protection
	if (vbus_top >= _IQ(Vbusmax) || vbus_bot >= _IQ(Vbusmax))
	{
		ModulationOFF();
		fallo_bus = 1;
	}

	//SPEED CONTROL
		//update states
		UPDATEQD_STATE(err_idqe);
		UPDATEQD_STATE(vdqe);
		UPDATE_STATE(theta_flux_hat);
		UPDATE_STATE(w_flux_hat);
		UPDATE_STATE(w_elec);
		UPDATE_STATE(error_w);
		UPDATE_STATE(T_ref);
		UPDATE_STATE(phase_rotor);
		w_ref = _IQmpy(w_refhz,TWOPI);
		PH2QD(ia,ib,idqs);

		phase_rotor[N]= qep1.theta_elec;
		w_elec[N] = qep1.w_elec;
		w_hz = _IQmpy(qep1.w_elec,ONEOVERTWOPI);
```

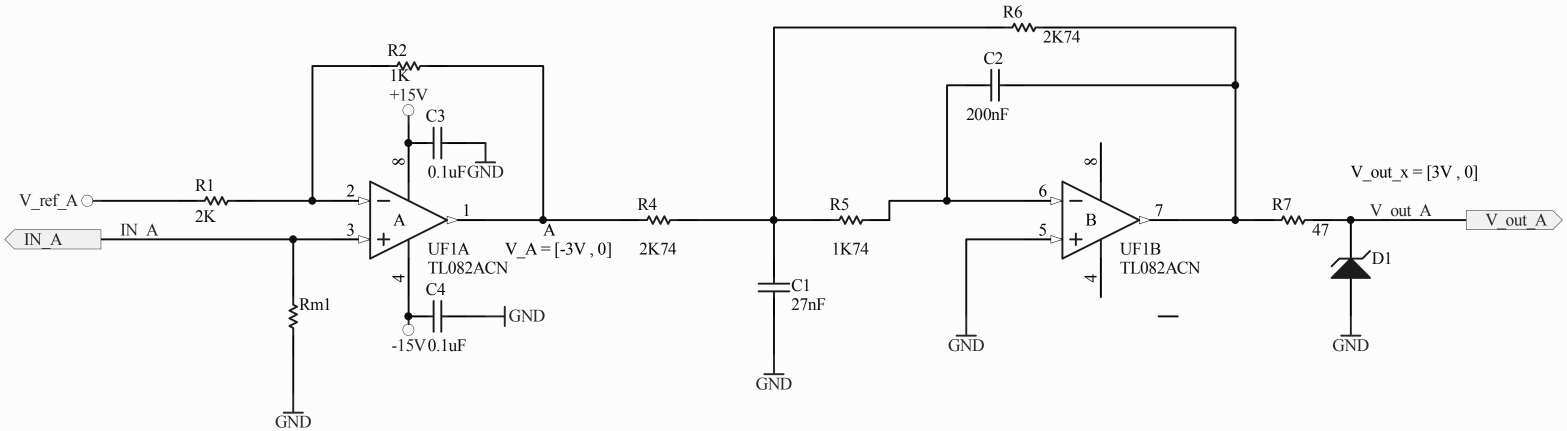
```
		if (_IQabs(w_elec[N]-w_elec[N1])>=_IQ(5))
		{
			w_elec[N]=w_elec[N1];
		}

		SROTATE_POS(idqs,idqe,theta_flux_hat[N1]);

		// Flux observer
		if(_IQabs(idqe.d)<_IQ(1.0))
			w_flux_hat[N] = w_flux_hat[N1];
		else
			w_flux_hat[N] = w_elec[N] + _IQdiv(-idqe.q,_IQmpy(idqe.d,tau_r));

		INT(w_flux_hat,theta_flux_hat);
		WRAP2PI(theta_flux_hat[N]);

		error_w[N]= w_elec[N] - w_ref;
		PI_REG(error_w,T_ref,Kp_vel,Ki_vel);

		LIM(T_ref[N],_IQ(50));//Imax
		idqe_ref.q = T_ref[N];
		idqe_ref.d = _IQ(18);

		LIM(idqe_ref.d,_IQ(30));//Imax
		LIM(idqe_ref.q,_IQ(50));//Imax

		//Current Regulator
		err_idqe.d[N] = idqe_ref.d -idqe.d;
		err_idqe.q[N] = idqe_ref.q -idqe.q;
		PI_QD_REG(err_idqe,vdqe,Kp_current, Ki_current);
		//dq to abc
		ROTATE_NEG(vdqe,vdqs,theta_flux_hat[N1]);
		if(_IQabs(vdqs.q[N]) >= (_IQdiv((vbus_top+vbus_bot),_IQ(2.0))))
		{
			LIM(vdqs.q[N],_IQdiv((vbus_top+vbus_bot),_IQ(2.0)));
			ROTATE_POS(vdqs,vdqe,theta_flux_hat[N1]);
			INV_PI_QD_REG(err_idqe,vdqe,Kp_current,Ki_current);
		}
		DQ2PH_QDDATA(vdqs,vas,vbs,vcs);
		LIM(vas,_IQdiv((vbus_top+vbus_bot),_IQ(2.0)));
		LIM(vbs,_IQdiv((vbus_top+vbus_bot),_IQ(2.0)));
		LIM(vcs,_IQdiv((vbus_top+vbus_bot),_IQ(2.0)));
		vu_ref = _IQdiv(_IQmpy(vas,_IQ(2.0)),(vbus_top+vbus_bot));
		vv_ref = _IQdiv(_IQmpy(vbs,_IQ(2.0)),(vbus_top+vbus_bot));
		vw_ref = _IQdiv(_IQmpy(vcs,_IQ(2.0)),(vbus_top+vbus_bot));


	//Duty cycle calculations and limits
	D_top_u = vu_ref;
	if(D_top_u <= 0)
		D_top_u = 0;
	D_bot_u = vu_ref + _IQ(1.0);
	if(D_bot_u <= 0)
		D_bot_u = 0;
	D_top_v = vv_ref;
	if(D_top_v <= 0)
		D_top_v = 0;
	D_bot_v = vv_ref + _IQ(1.0);
	if(D_bot_v <= 0)
		D_bot_v = 0;
	D_top_w = vw_ref;
	if(D_top_w <= 0)
		D_top_w = 0;
	D_bot_w = vw_ref + _IQ(1.0);
	if(D_bot_w <= 0)
		D_bot_w = 0;
```

```
        //Duty cycles update
        UpdatePWM1(D_top_u);
        UpdatePWM2(D_bot_u);
        UpdatePWM3(D_top_v);
        UpdatePWM4(D_bot_v);
        UpdatePWM5(D_top_w);
        UpdatePWM6(D_bot_w);

        // Reinitialize for next ADC sequence
        AdcRegs.ADCTRL2.bit.RST_SEQ1 = 1;       // Reset SEQ1
        AdcRegs.ADCST.bit.INT_SEQ1_CLR = 1;             // Clear INT SEQ1 bit
        AdcRegs.ADCTRL2.bit.RST_SEQ2 = 1;       // Reset SEQ1
        AdcRegs.ADCST.bit.INT_SEQ2_CLR = 1;             // Clear INT SEQ1 bit
        PieCtrlRegs.PIEACK.all = PIEACK_GROUP1; // Acknowledge interrupt to PIE
}

// ========        End of Source Code          =========\\
```

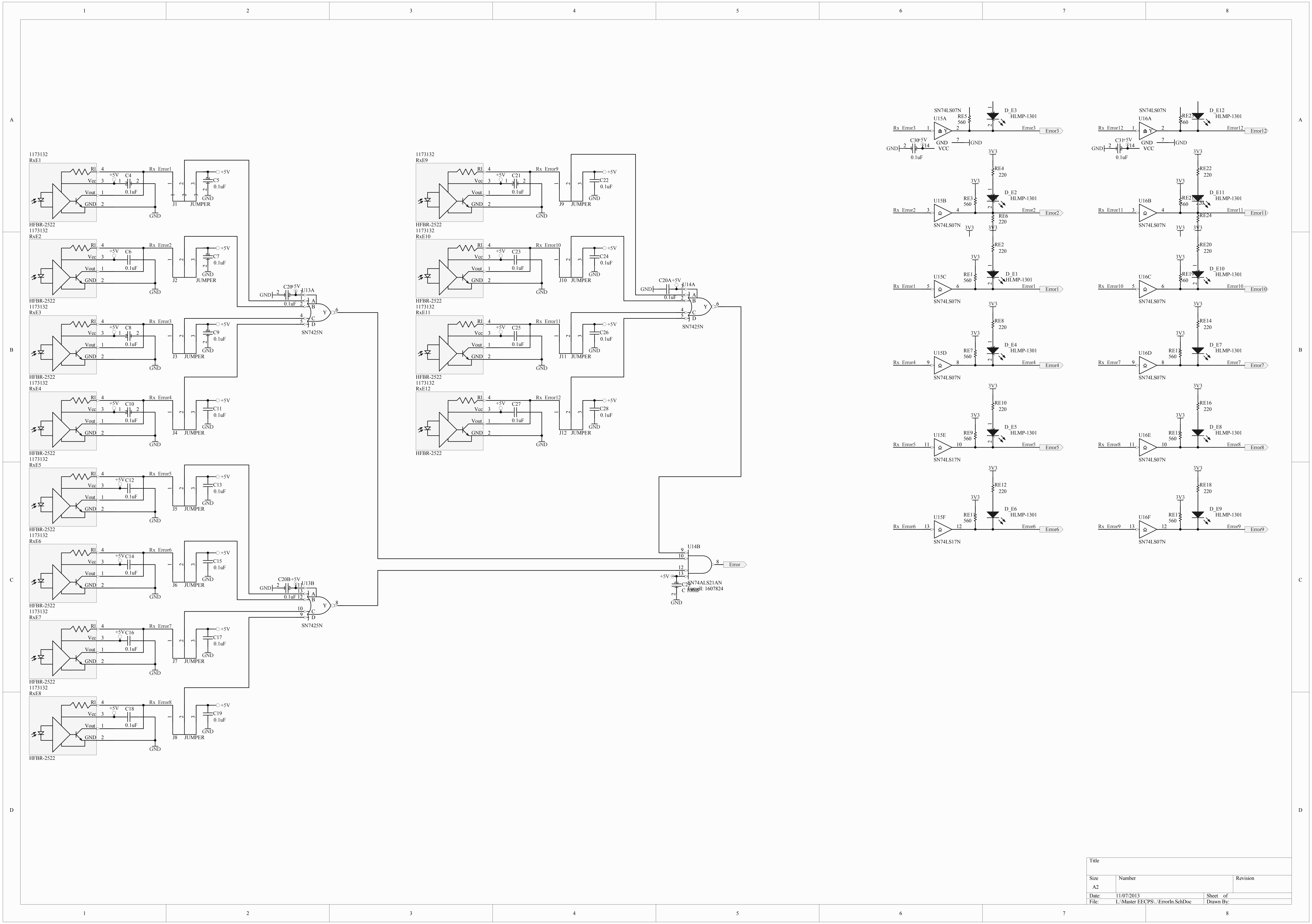
Annex II: Schematics



STOP activo por nivel bajo
Igual que para ADA0, Vin viene por cable expresamente
A seta NC
Title
Size
A1
Number
Revision
Date: 12/07/2013
Sheet of
File: L:\Master EECPS_PlacaIntDSP_v1FIN…
Drawn By: Juan Manuel Guerrero Muñoz
1 2 3 4 5 6 7 8 9 10 11 12
A B C D



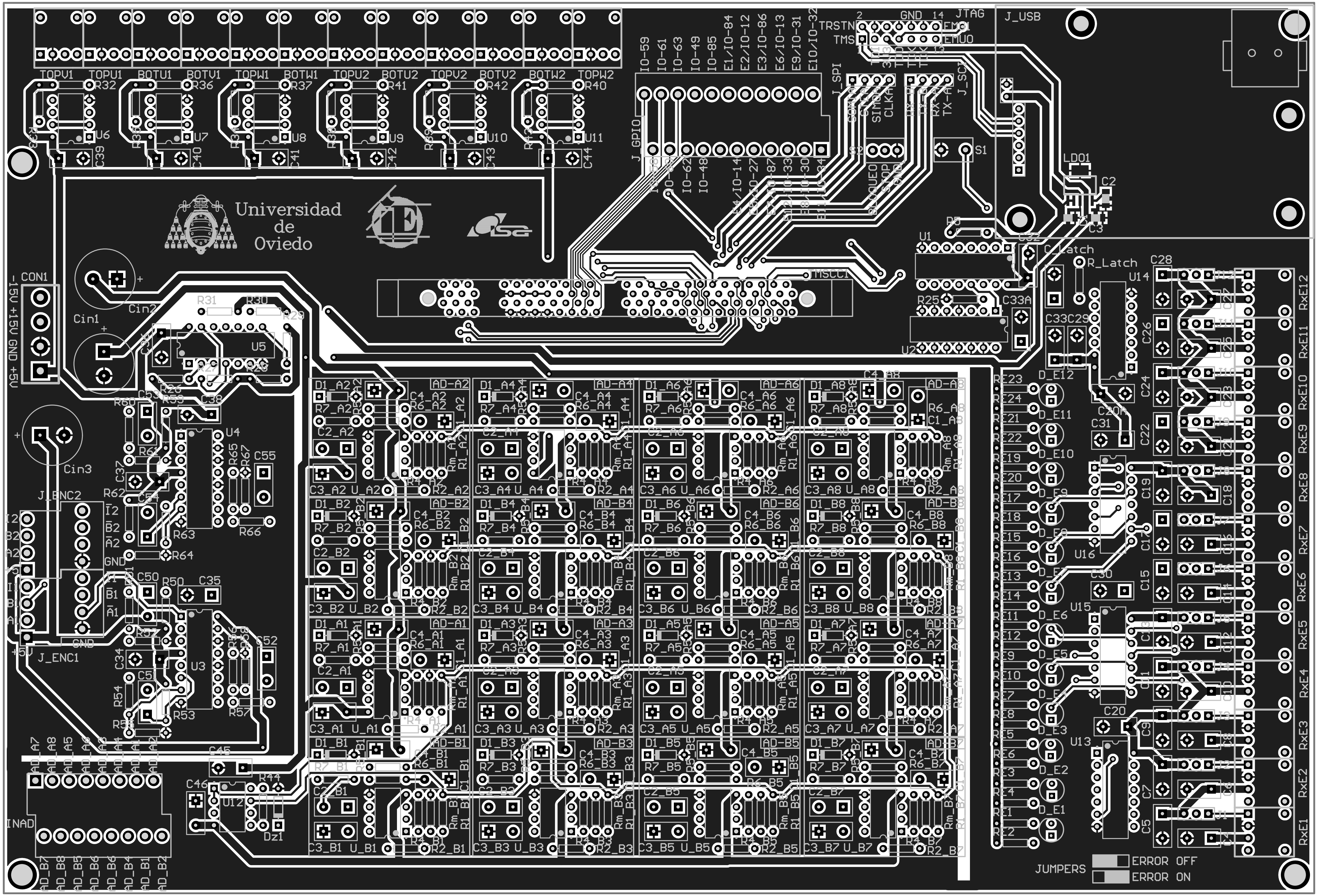
Title			
Size A4	Number		Revision
Date:	11/07/2013	Sheet of	
File:	L:\Master EECPS\..\Base_filtro_1_8.SchDoc	Drawn By:	



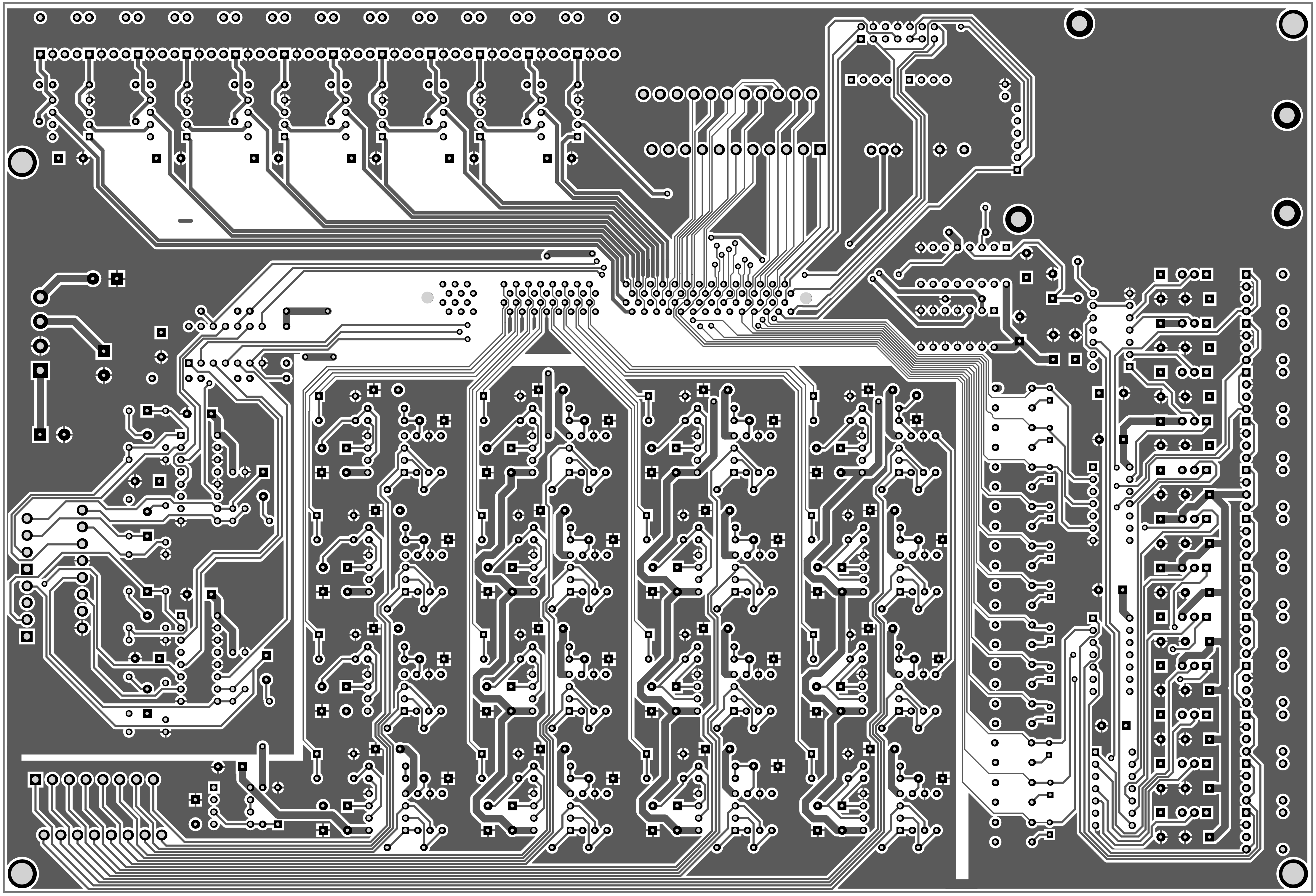
1173132
RxE1
RxE2
RxE3
RxE4
RxE5
RxE6
RxE7
RxE8
RxE9
RxE10
RxE11
RxE12
HFBR-2522
RI
Vcc
Vout
GND
+5V
0.1uF
JUMPER
Rx_Error1
Rx_Error2
Rx_Error3
Rx_Error4
Rx_Error5
Rx_Error6
Rx_Error7
Rx_Error8
Rx_Error9
Rx_Error10
Rx_Error11
Rx_Error12
U13A
U13B
U14A
SN7425N
U14B
SN74ALS21AN
Farnell: 1607824
Error
SN74LS07N
SN74LS17N
U15A
U15B
U15C
U15D
U15E
U15F
U16A
U16B
U16C
U16D
U16E
U16F
HLMP-1301
3V3
560
220
VCC
Error1
Error2
Error3
Error4
Error5
Error6
Error7
Error8
Error9
Error10
Error11
Error12
Title
Size
A2
Number
Revision
Date:
11/07/2013
Sheet of
File:
L:\Master EECPS\..\ErrorIn.SchDoc
Drawn By:

Annex III: PCB

PCB TOP layer


Universidad
de
Oviedo
J_USB
JTAG
CON1
JUMPERS
ERROR OFF
ERROR ON

PCB BOTTOM layer



Annex IV: Datasheets

HFBR-RXXYYY Series (POF)
HFBR-EXXYYY Series (POF)

Plastic Optical Fiber Cable and Accessories for Versatile Link

Data Sheet

Cable Description

The HFBR-R/EXXYYY series of plastic fiber optic cables are constructed of a single step-index fiber sheathed in a black polyethylene jacket. The duplex fiber consists of two simplex fibers joined with a zipcord web.

Standard attenuation and extra low loss POF cables are identical except for attenuation specifications.

Polyethylene jackets on all plastic fiber cables comply with UL VW-1 flame retardant specification (UL file # E89328).

Cables are available in unconnectored or connectored options. Refer to the Ordering Guide for part number information.

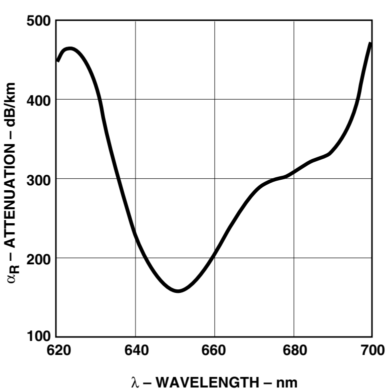


Figure 1. Typical POF attenuation vs. wavelength.

Features

- Compatible with Avago Versatile Link Family of connectors and fiber optic components
- 1 mm diameter Plastic Optical Fiber (POF) in two grades: low cost standard POF with 0.22 dB/m typical attenuation, or high performance extra low loss POF with 0.19 dB/m typical attenuation

Applications

- Industrial data links for factory automation and plant control
- Intra-system links; board-to-board, rack-to-rack
- Telecommunications switching systems
- Computer-to-peripheral data links, PC bus extension
- Proprietary LANs
- Digitized video
- Medical instruments
- Reduction of lightning and voltage transient susceptibility
- High voltage isolation

Plastic Optical Fiber Specifications: HFBR-R/EXXYYY

Absolute Maximum Ratings

Parameter		Symbol	Min.	Max.	Unit	Note
Storage and Operating Temperature		$T_{S,O}$	-55	+85	°C	
Recommended Operating Temperature		T_O	-40	+85	°C	
Installation Temperature		T_I	-20	+70	°C	1
Short Term Tensile Force	Single Channel	F_T		50	N	2
	Dual Channel	F_T		100	N	
Short Term Bend Radius		r	25		mm	3, 4
Long Term Bend Radius		r	35		mm	
Long Term Tensile Load		F_T		1	N	
Flexing				1000	Cycles	4

Mechanical/Optical Characteristics, T_A = -40 to +85°C unless otherwise specified.

Parameter		Symbol	Min.	Typ.[5]	Max.	Unit	Condition
Cable Attenuation	Standard Cable, Type "R"	α_O	0.15	0.22	0.27	dB/m	Source is HFBR-15XX (660 mm LED, 0.5 NA)
	Extra Low Loss, Type "E"		0.15	0.19	0.23		ℓ= 50 meters
Reference Attenuation	Standard Cable, Type "R"	α_R	0.12	0.19	0.24	dB/m	Source is 650 nm, 0.5 NA monochrometer,
	Extra Low Loss, Type "E"		0.12	0.16	0.19		ℓ= 50 meters Note 7, Figure 1
Numerical Aperture		NA	0.46	0.47	0.50		>2 meters
Diameter, Core and Cladding		D_C	0.94	1.00	1.06	mm	
Diameter, Jacket		D_J	2.13	2.20	2.27	mm	Simplex Cable
Propagation Delay Constant		l/v		5.0		ns/m	Note 6
Mass per Unit Length/Channel				5.3		g/m	Without Connectors
Cable Leakage Current		I_L		12		nA	50 kV, ℓ= 0.3 meters
Refractive Index	Core	n		1.492			
	Cladding			1.417			

Notes:

1. Installation temperature is the range over which the cable can be bent and pulled without damage. Below -20°C the cable becomes brittle and should not be subjected to mechanical stress.
2. Short Term Tensile Force is for less than 30 minutes.
3. Short Term Bend Radius is for less than 1 hour nonoperating.
4. 90° bend on 25 mm radius mandrel. Bend radius is the radius of the mandrel around which the cable is bent.
5. Typical data are at 25°C.
6. Propagation delay constant is the reciprocal of the group velocity for propagation delay of optical power. Group velocity is v=c/n where c is the velocity of light in free space (3×10^8 m/s) and n is the effective core index of refraction.
7. Note that α_R rises at the rate of about 0.0067 dB/°C, where the thermal rise refers to the LED temperature changes above 25°C. Please refer to Figure 1 which shows the typical plastic optical fiber attenuation versus wavelength at 25°C.

Plastic Fiber Connector Styles

Connector Description

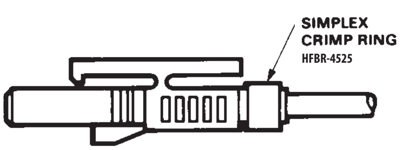
Four connector styles are available for termination of plastic optical fiber: simplex, simplex latching, duplex and duplex latching. All connectors provide a snap-in action when mated to Versatile Link components. Simplex connectors are color coded to facilitate identification of transmitter and receiver connections. Duplex connectors are keyed so that proper orientation is ensured during insertion. If the POF cable/connector will be used at extreme operating temperatures or experience frequent and wide temperature cycling effects, the cable/connector attachment can be strengthened with an RTV adhesive (see Plastic Connectoring Instructions for more detail). The connectors are made of a flame retardant VALOX UL94 V-0 material (UL file # E121562).

SIMPLEX CONNECTOR STYLES

HFBR-4501/4511 – Simplex

The simplex connector provides a quick and stable connection for applications that require a component-to-connector retention force of 8 Newtons (1.8 lb.). These connectors are available in gray (HFBR-4501) or blue (HFBR-4511).

HFBR-4503/4513 – Simplex Latching

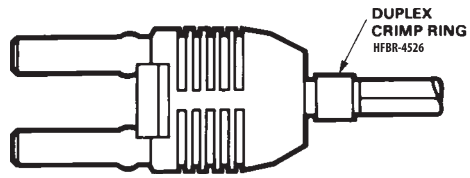


The simplex latching connector is designed for rugged applications requiring a greater retention force — 80 Newtons (18 lb.) — than provided by a simplex nonlatching connector. When inserting the simplex latching connector into a module, the connector latch mechanism should be aligned with the top surface of the horizontal modules, or with the tall vertical side of the vertical modules. Misalignment of an inserted latching connector into either module will not result in a positive latch. The connector is released by depressing the rear section of the connector lever, and then pulling the connector assembly away from the module housing.

The simplex latching connector is available in gray (HFBR-4503) or blue (HFBR-4513).

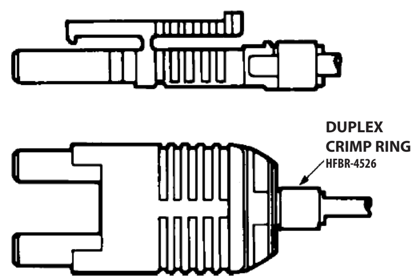
DUPLEX CONNECTOR STYLES

HFBR-4506 – Duplex



Duplex connectors provide convenient duplex cable termination and are keyed to prevent incorrect insertion into duplex configured modules. The duplex connector is compatible with dual combinations of horizontal or vertical Versatile Link components (e.g., two horizontal transmitters, two vertical receivers, a horizontal transmitter with a horizontal receiver, etc.). The duplex non-latching connector is available in parchment, off-white (HFBR-4506).

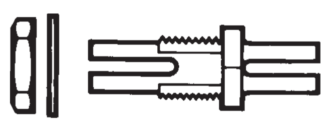
HFBR-4516 – Duplex Latching



The duplex latching connector is designed for rugged applications requiring greater retention force than the nonlatching duplex connector. When inserting the duplex latching connector into a module, the connector latch mechanism should be aligned with the top surface of the dual combination of horizontal or vertical Versatile Link components. The duplex latching connector is available in gray (HFBR-4516).

Feedthrough/Splice

HFBR-4505/4515 Bulkhead Adapter



The HFBR-4505/4515 adapter mates two simplex connectors for panel/bulkhead feedthrough of HFBR-4501/4511 terminated plastic fiber cable. Maximum panel thickness is 4.1 mm (0.16 inch). This adapter can serve as a cable in-line splice using two simplex connectors. The adapters are available in gray (HFBR-4505) and blue (HFBR-4515). This adapter is not compatible with POF duplex, POF simplex latching, or HCS connectors.

Plastic Optical Fiber Connector Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit	Note
Storage and Operating Temperature	$T_{S,O}$	-40	85	°C	1
Recommended Operating Temperature	T_O	-40	85	°C	1
Installation Temperature	T_I	0	70	°C	1
Nut Torque HFBR-4505/4515 Adapter	T_N		0.7	N-m	2
			100	OzF-in.	

Notes:
1. Storage and Operating Temperatures refer to the ranges over which the connectors can be used when not subjected to mechanical stress. Installation Temperature refers to the ranges over which connectors may be installed onto the fiber and over which connectors can be connected and disconnected from transmitter and receiver modules.
2. Recommended nut torque is 0.57 N-m.

Plastic Optical Fiber Connector Mechanical/Optical Characteristics

T_A = -40 to +85°C, Unless Otherwise Specified.

Parameter	Part Number	Symbol	Min.	Typ.[1]	Max.	Units	Temp. °C	Note
Retention Force, Connector to Versatile Link Transmitters and Receivers	Simplex, HFBR-4501/4511	F_{R-C}	7	8		N	+25	2
			3				-40 to +85	
	Simplex Latching, HFBR-4503/4513		47	80			+25	
			11				-40 to +85	
	Duplex, HFBR-4506		7	12			+25	
			4				-40 to +85	
	Duplex Latching, HFBR-4516		50	80			+25	
			15				-40 to +85	
Tensile Force, Connector to Cable	Simplex, HFBR-4501/4511	F_T	8.5	22		N		3
	Simplex Latching, HFBR-4503/4513		8.5	22				
	Duplex, HFBR-4506		14	35				
	Duplex Latching, HFBR-4516		14	35				
Adapter Connector to Connector Loss	HFBR-4505/4515 with HFBR-4501/4511	α_{CC}	0.7	1.5	2.8	dB	25	4, 5
Retention Force Connector to Adapter	HFBR-4505/4515 with HFBR-4501/4511	F_{R-B}	7	8		N		
Insertion Force, Connector to Versatile Link Transmitters and Receivers	Simplex, HFBR-4501/4511	F_I		8	30	N		6
	Simplex Latching, HFBR-4503/4513			16	35			
	Duplex, HFBR-4506			13	46			
	Duplex Latching HFBR-4516			22	51			

Notes:
1. Typical data are at +25°C.
2. No perceivable reduction in retention force was observed after 2000 insertions. Retention force of non-latching connectors is lower at elevated temperatures. Latching connectors are recommended for applications where a high retention force at high temperatures is desired.
3. For applications where frequent temperature cycling over temperature extremes is expected, please contact Avago Technologies for alternate connectoring techniques.
4. Minimum and maximum limit for α_{CC} for 0°C to +70°C temperature range. Typical value of α_{CC} is at +25°C.
5. Factory polish or field polish per recommended procedure.
6. Destructive insertion force was typically at 178 N (40 lb.).

Step-by-Step Plastic Cable Connectoring Instructions

The following step-by-step guide describes how to terminate plastic fiber optic cable. It is ideal for both field and factory installation. Connectors can be easily installed on cable ends with wire strippers, cutters and a crimping tool.

Finishing the cable is accomplished with the Avago HFBR-4593 Polishing Kit, consisting of a Polishing Fixture, 600 grit abrasive paper and 3 µm pink lapping film (3M Company, OC3-14). The connector can be used immediately after polishing.

Materials needed for plastic fiber termination are:

1. Avago Plastic Optical Fiber Cable (Example: HFBR-RUS500, HFBR-RUD500, HFBR-EUS500, or HFBR-EUD500)
2. Industrial Razor Blade or Wire Cutters
3. 16 Gauge Latching Wire Strippers (Example: Ideal Stripmaster™ type 45-092).
4. HFBR-4597 Crimping Tool
5. HFBR-4593 Polishing Kit
6. One of the following connectors:

   a) HFBR-4501/4503 Gray Simplex/Simplex Latching Connector and HFBR-4525 Simplex Crimp Ring

   b) HFBR-4511/4513 Blue Simplex/Simplex Latching Connector and HFBR-4525 Simplex Crimp Ring

   c) HFBR-4506 Parchment (off-white) Duplex Connector and HFBR-4526 Duplex Crimp Ring

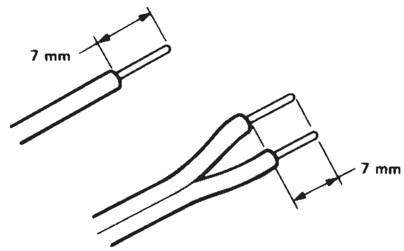
   d) HFBR-4516 Gray Latching Duplex Connector and HFBR-4526 Duplex Crimp Ring

Step 1

The zip cord structure of the duplex cable permits easy separation of the channels. The channels should be separated a minimum of 100 mm (4 in) to a maximum of 150 mm (6 in) back from the ends to permit connectoring and polishing.

After cutting the cable to the desired length, strip off approximately 7 mm (0.3 in.) of the outer jacket with the 16 gauge wire strippers. Excess webbing on the duplex cable may have to be trimmed to allow the simplex or simplex latching connector to slide over the cable.

When using the duplex connector and duplex cable, the separated duplex cable must be stripped to equal lengths on each cable. This allows easy and proper seating of the cable into the duplex connector.



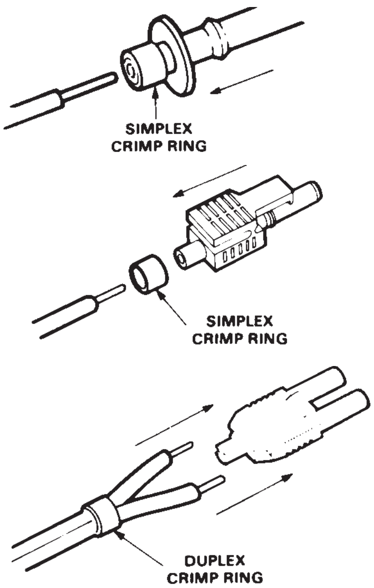
Step 2

Place the crimp ring and connector over the end of the cable; the fiber should protrude about 3 mm (0.12 in.) through the end of the connector. Carefully position the ring so that it is entirely on the connector with the rim of the crimp ring flush with the connector, leaving a small space between the crimp ring and the flange. Then crimp the ring in place with the crimping tool. One crimp tool is used for all POF connector crimping requirements.

For applications with extreme temperature operation or frequent temperature cycling, improved connector to cable attachment can be achieved with the use of an RTV (GE Company, RTV-128 or Dow Corning 3145-RTV) adhesive. The RTV is placed into the connector prior to insertion of the fiber and the fiber is crimped normally. The connector can be polished after the RTV has cured and is then ready for use.

Note: By convention, place the gray connector on the transmitter cable end and the blue connector on the receiver cable end to maintain color coding (different color connectors are mechanically identical).

Simplex connector crimp rings cannot be used with duplex connectors and duplex connector crimp rings cannot be used with simplex connectors because of size differences. The simplex crimp has a dull luster appearance; the duplex ring is glossy and has a thinner wall.



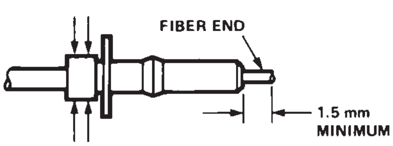
Step 3

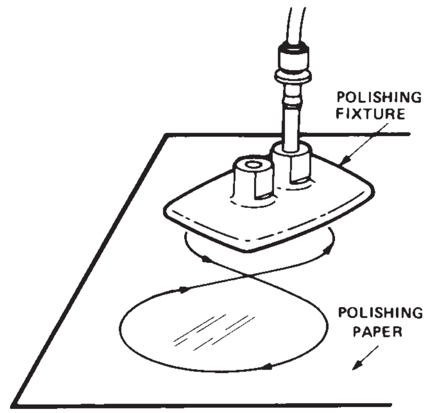
Any excess fiber protruding from the connector end may be cut off; however, the trimmed fiber should extend at least 1.5 mm (0.06 in) from the connector end.

Insert the connector fully into the polishing fixture with the trimmed fiber protruding from the bottom of the fixture. This plastic polishing fixture can be used to polish two simplex connectors or simplex latching connectors simultaneously, or one duplex connector.

Note: The four dots on the bottom of the polishing fixture are wear indicators. Replace the polishing fixture when any dot is no longer visible. Typically, the polishing fixture can be used 10 times; 10 duplex connectors or 20 simplex connectors, two at a time.

Place the 600 grit abrasive paper on a flat smooth surface, pressing down on the connector, polish the fiber and the connector using a figure eight pattern of strokes until the connector is flush with the bottom of the polishing fixture. Wipe the connector and fixture with a clean cloth or tissue.





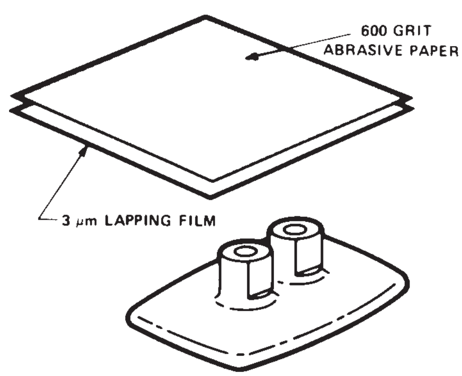
Step 4

Place the flush connector and polishing fixture on the dull side of the 3 µm pink lapping film and continue to polish the fiber and connector for approximately 25 strokes. The fiber end should be flat, smooth and clean.

This cable is now ready for use.

Note: Use of the pink lapping film fine polishing step results in approximately 2 dB improvement in coupling performance of either a transmitter-receiver link or a bulkhead/splice over a 600 grit polish alone. This fine polish is comparable to the Avago factory polish. The fine polishing step may be omitted where an extra 2 dB of optical power is not essential, as with short link lengths. Proper polishing of the tip of the fiber/connector face results in a tip diameter between 2.5 mm (0.098 in.) minimum and 3.2 mm (0.126 in.) maximum..

HFBR-4593 Polishing Kit



(USED WITH ALL CONNECTOR TYPES)

Ordering Guide for POF Connectors and Accessories

Plastic Optical Fiber Connectors

HFBR-4501	Gray Simplex Connector/Crimp Ring
HFBR-4511	Blue Simplex Connector/Crimp Ring
HFBR-4503	Gray Simplex Latching Connector with Crimp Ring
HFBR-4513	Blue Simplex Latching Connector with Crimp Ring
HFBR-4506	Parchment Duplex Connector with Crimp Ring
HFBR-4516	Gray Duplex Latching Connector with Crimp Ring
HFBR-4505	Gray Adapter (Bulkhead/Feedthrough)
HFBR-4515	Blue Adapter (Bulkhead/Feedthrough)

Plastic Optical Fiber Accessories

HFBR-4522	500 HFBR-0500 Products Port Plugs
HFBR-4525	1000 Simplex Crimp Rings
HFBR-4526	500 Duplex Crimp Rings
HFBR-4593	Polishing Kit (one polishing tool, two pieces 600 grit abrasive paper, and two pieces 3 µm pink lapping film)
HFBR-4597	Plastic Fiber Crimping Tool

Ordering Guide for POF Cable

For Example:

HFBR-RUD500 is a Standard Attenuation, Unconnectored, Duplex, 500 meter cable.

HFBR-RLS001 is a Standard Attenuation, Latching Simplex Connectored, Simplex, 1 meter cable.

HFBR-RMD010 is a Standard Attenuation, Standard Duplex Connectored, Duplex, 10 meter cable.

HFBR-RMD100 is a Standard Attenuation, Standard Duplex Connectored, Duplex, 100 meter cable.

Cable Length Tolerances:

The plastic cable length tolerances are: +10%/-0%.

NOTE: By convention, pre-connectored simplex POF cables have gray and blue colored connectors on the opposite ends of the same fiber; although oppositely colored, the connectors are mechanically identical. Duplex POF cables with duplex connectors use color- coded markings on the duplex fiber cable to differentiate between the channel.

HFBR- □□□□□□

Cable Code

R = Standard Attenuation POF
E = Extra Low Loss POF

Connector Code

U = Unconnectored
N = Standard Simplex Connectors
L = Latching Simplex Connectors
M = Standard Duplex Connectors
T = Latching Duplex Connectors

Channel Code

S = Simplex Cable
D = Duplex Zipcord Cable

Length Code

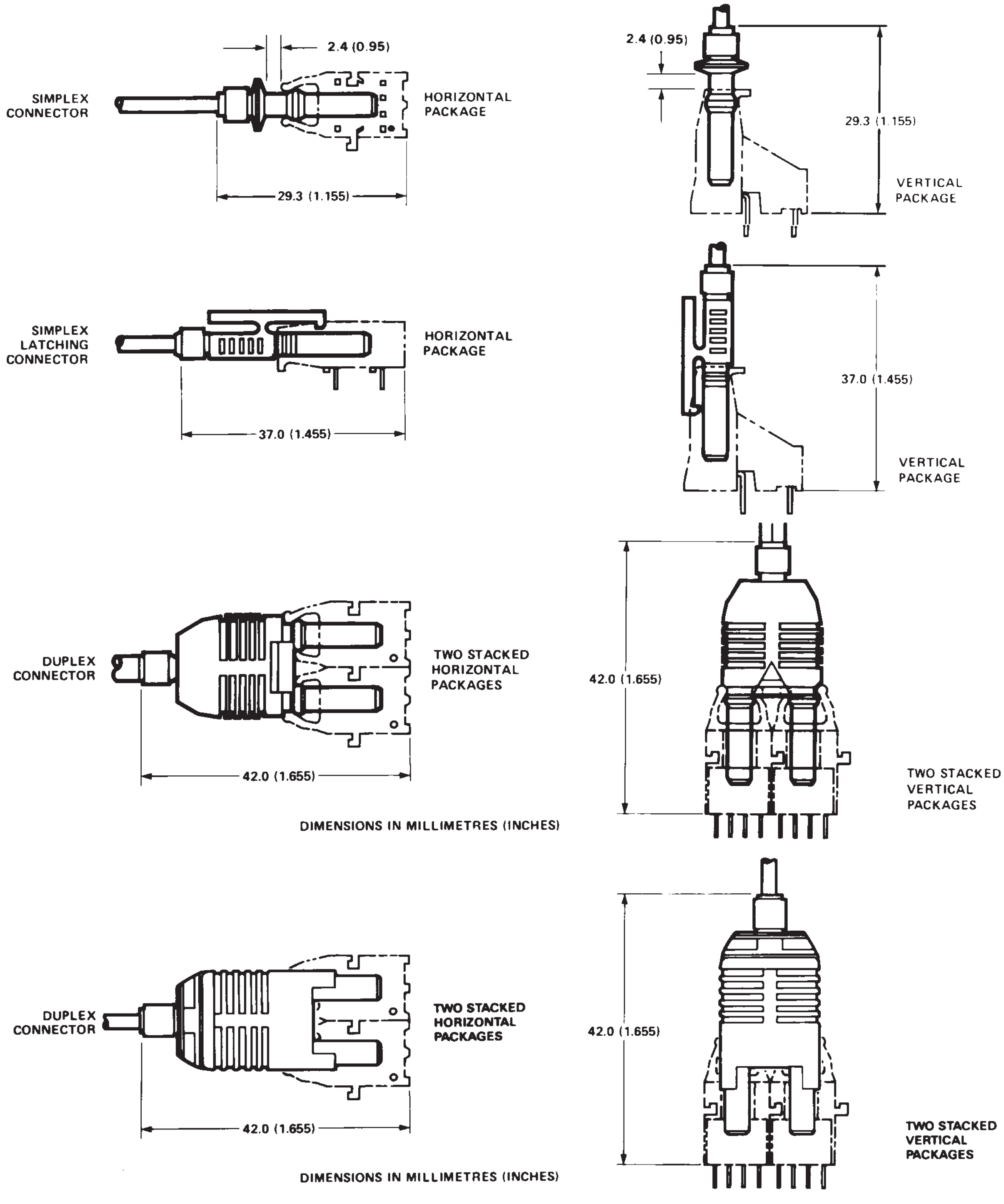
(measured from tip of connector to tip of connector)

1-500 meters in 1 meter increments
e.g. 015 = 15 meters
1-10 meters in 1 decimeter increments
e.g. 15D = 1.5 meters

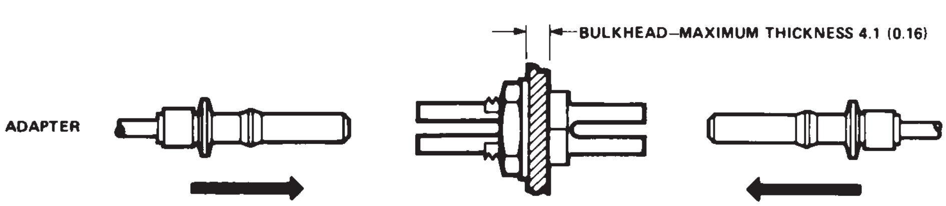
Note: Not all possible combinations reflect available part numbers.
Please contact your local Avago representative for a list of current available cable part numbers.

Connector Applications

Attachment to Avago Versatile Link Fiber Optic Components

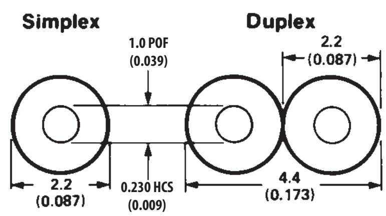


Bulkhead Feedthrough or Panel Mounting for HFBR-4501/4511 Simplex Connectors

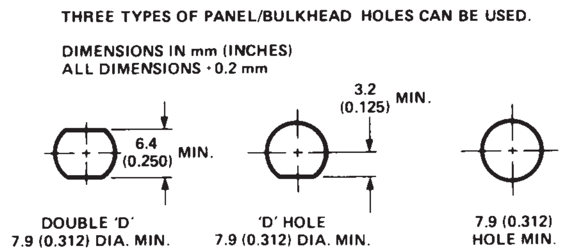


Versatile Link Mechanical Dimensions

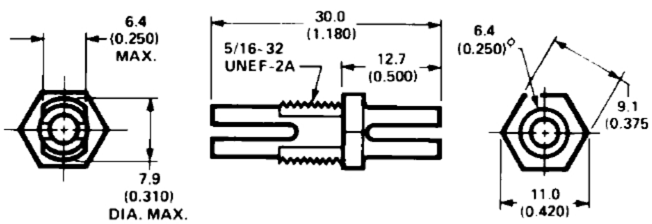
Fiber Optic Cable Dimensions



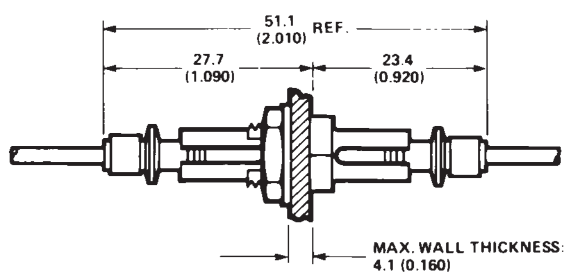
Panel Mounting – Bulkhead Feedthrough



HFBR-4505 (Gray)/4515 (Blue) Adapters



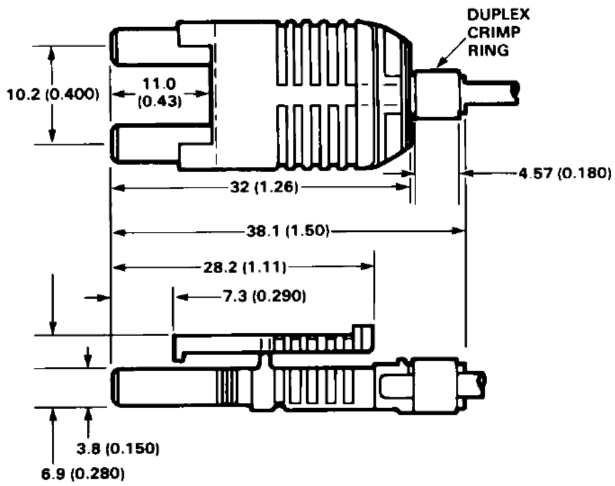
Bulkhead Feedthrough with Two HFBR-4501/4511 Connectors



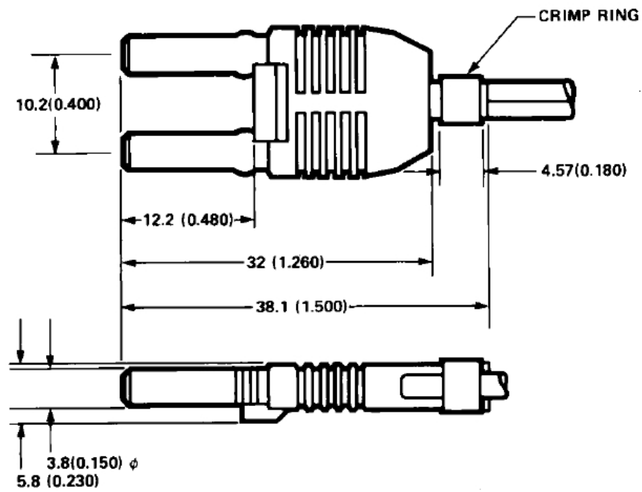
All dimensions in mm (inches).
All dimensions ±0.25 mm unless otherwise specified.

Versatile Link Mechanical Dimensions, continued

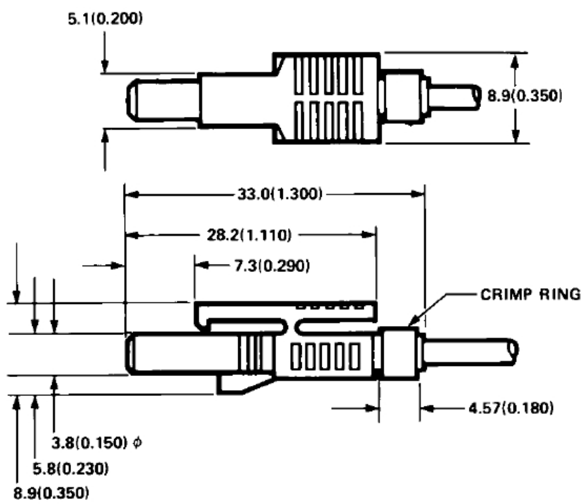
HFBR-4516 (Parchment) Duplex Latching Connector



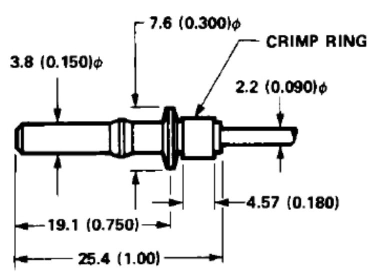
HFBR-4506 (Parchment) Duplex Connector



HFBR-4503 (Gray)/4513 (Blue) Simplex Latching Connector



HFBR-4501 (Gray)/4511 (Blue) Simplex Connector



CONNECTORS DIFFER ONLY IN COLOR

All dimensions in mm (inches).
All dimensions ±0.25 mm unless otherwise specified.

For product information and a complete list of distributors, please go to our website: **www.avagotech.com**

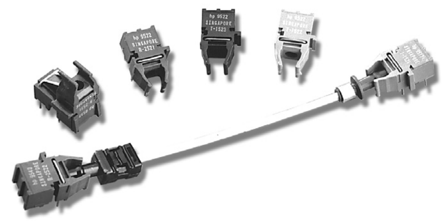
AV02-1848EN - March 31, 2009

HFBR-0500Z Series

Versatile Link

The Versatile Fiber Optic Connection

Data Sheet



Description

The Versatile Link series is a complete family of fiber optic link components for applications requiring a low cost solution. The HFBR-0500Z series includes transmitters, receivers, connectors and cable specified for easy design. This series of components is ideal for solving problems with voltage isolation/insulation, EMI/RFI immunity or data security. The optical link design is simplified by the logic compatible receivers and complete specifi-cations for each component. The key optical and electrical parameters of links configured with the HFBR-0500Z family are fully guaranteed from 0° to 70°C.

A wide variety of package configurations and connectors provide the designer with numerous mechanical solutions to meet application requirements. The transmitter and receiver components have been designed for use in high volume/low cost assembly processes such as auto insertion and wave soldering.

Transmitters incorporate a 660 nm LED. Receivers include a monolithic dc coupled, digital IC receiver with open collector Schottky output transistor. An internal pullup resistor is available for use in the HFBR-25X1Z/2Z/4Z receivers. A shield has been integrated into the receiver IC to provide additional, localized noise immunity.

Internal optics have been optimized for use with 1 mm diameter plastic optical fiber. Versatile Link specifications incorporate all connector interface losses. Therefore, optical calculations for common link applications are simplified.

Features

- RoHS-compliant
- Low cost fiber optic components
- Enhanced digital links: dc-5 MBd
- Extended distance links up to 120 m at 40 kBd
- Low current link: 6 mA peak supply current
- Horizontal and vertical mounting
- Interlocking feature
- High noise immunity
- Easy connectoring: simplex, duplex, and latching connectors
- Flame retardant
- Transmitters incorporate a 660 nm red LED for easy visibility
- Compatible with standard TTL circuitry

Applications

- Reduction of lightning/voltage transient susceptibility
- Motor controller triggering
- Data communications and local area networks
- Electromagnetic Compatibility (EMC) for regulated systems: FCC, VDE, CSA, etc.
- Tempest-secure data processing equipment
- Isolation in test and measurement instruments
- Error free signalling for industrial and manufacturing equipment
- Automotive communications and control networks
- Noise immune communication in audio and video equipment

HFBR-0500Z Series Part Number Guide

HFBR X5XXZ

1 = Transmitter
2 = Receiver

5 = 600 nm Transmitter and Receiver Products

2 = Horizontal Package
3 = Vertical Package

Z = RoHS-compliant

1 = 5 MBd High Performance Link
2 = 1 MBd High Performance Link
3 = 40 kBd Low Current/Extended Distance Link
4 = 1 MBd Standard Link
6 = 155 MBd Receiver
7 = 155 MBd Transmitter
8 = 10 MBd High Performance Link

Link Selection Guide

(Links specified from 0 to 70°C, for plastic optical fiber unless specified.)

Signal Rate	Distance (m) 25°C	Distance (m)	Transmitter	Receiver
40 kBd	120	110	HFBR-1523Z	HFBR-2523Z
1 MBd	20	10	HFBR-1524Z	HFBR-2524Z
1 MBd	55	45	HFBR-1522Z	HFBR-2522Z
5 Mbd	30	20	HFBR-1521Z	HFBR-2521Z

Evaluation Kit

HFBR-0500Z 1 MBd Versatile Link:

This kit contains: HFBR-1524Z Tx, HFBR-2524Z Rx, polishing kit, 3 styles of plastic connectors, Bulkhead feedthrough, 5 meters of 1 mm diameter plastic cable, lapping film and grit paper, and HFBR-0500Z data sheet.

Application Literature

Application Note 1035 (Versatile Link)

Package and Handling Information

The compact Versatile Link package is made of a flame retardant VALOX® UL 94 V-0 material (UL file # E121562) and uses the same pad layout as a standard, eight pin dual-in-line package. Vertical and horizontal mountable parts are available. These low profile Versatile Link packages are stackable and are enclosed to provide a dust resistant seal. Snap action simplex, simplex latching, duplex, and duplex latching connectors are offered with simplex or duplex cables.

Package Orientation

Performance and pinouts for the vertical and horizontal packages are identical. To provide additional attachment support for the vertical Versatile Link housing, the designer has the option of using a self-tapping screw through a printed circuit board into a mounting hole at the bottom of the package. For most applications this is not necessary.

Package Housing Color

Versatile Link components and simplex connectors are color coded to eliminate confusion when making connections. Receivers are blue and transmitters are gray, except for the HFBR-15X3Z transmitter, which is black.

VALOX® is a registered trademark of the General Electric Corporation.

Handling

Versatile Link components are auto-insertable. When wave soldering is performed with Versatile Link components, the optical port plug should be left in to prevent contamination of the port. Do not use reflow solder processes (i.e., infrared reflow or vapor-phase reflow). Nonhalogenated water soluble fluxes (i.e., 0% chloride), not rosin based fluxes, are recommended for use with Versatile Link components.

Versatile Link components are moisture sensitive devices and are shipped in a moisture sealed bag. If the components are exposed to air for an extended period of time, they may require a baking step before the soldering process. Refer to the special labeling on the shipping tube for details.

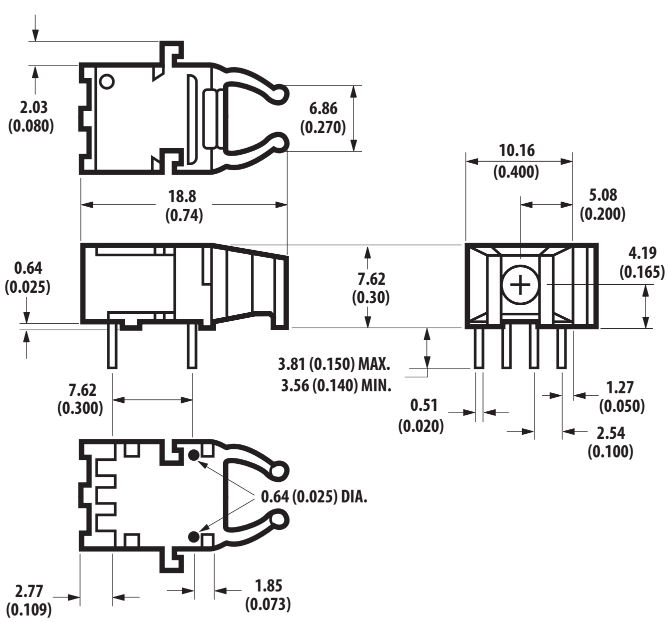
Recommended Chemicals for Cleaning/Degreasing

Alcohols: methyl, isopropyl, isobutyl. Aliphatics: hexane, heptane. Other: soap solution, naphtha.

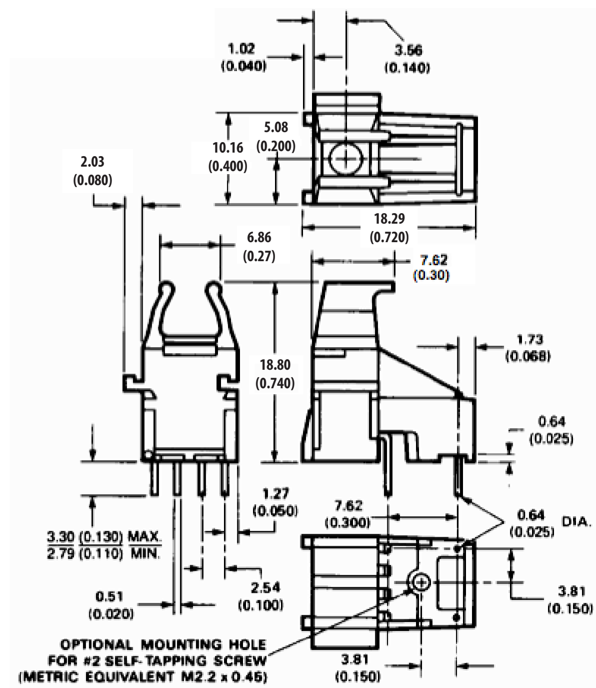
Do not use partially halogenated hydrocarbons such as 1,1.1 trichloroethane, ketones such as MEK, acetone, chloroform, ethyl acetate, methylene dichloride, phenol, methylene chloride, or N-methylpyrolldone. Also, Avago does not recommend the use of cleaners that use halogenated hydrocarbons because of their potential environmental harm.

Mechanical Dimensions

Horizontal Modules

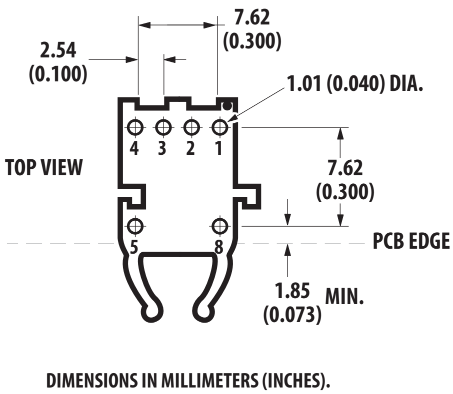


Vertical Modules

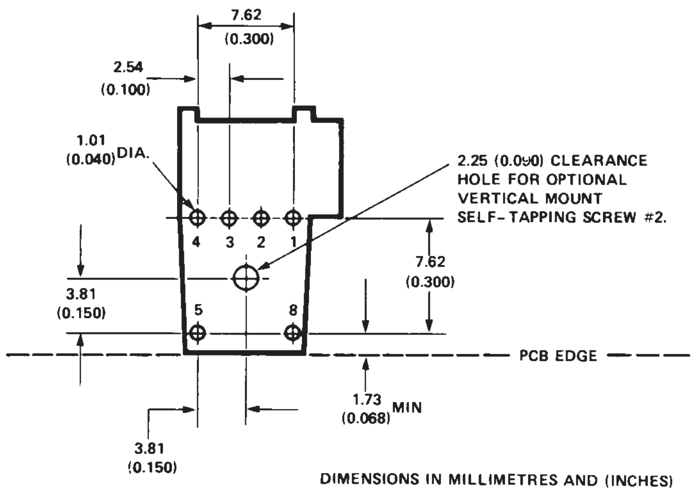


Versatile Link Printed Board Layout Dimensions

Horizontal Module



Vertical Module

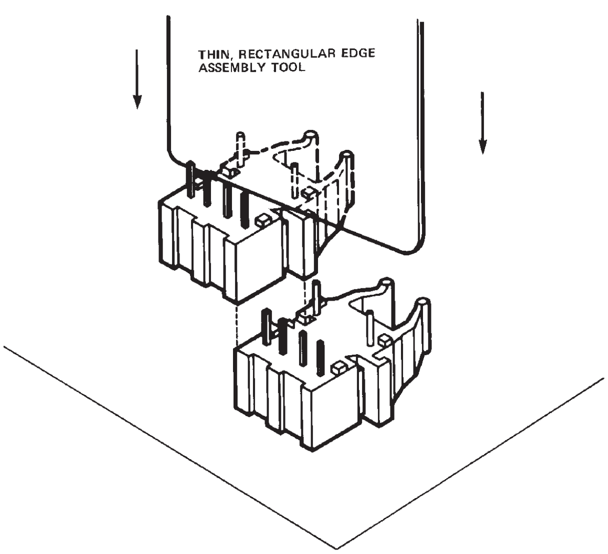


Interlocked (Stacked) Assemblies (refer to Figure 1)

Horizontal packages may be stacked by placing units with pins facing upward. Initially engage the interlocking mechanism by sliding the L bracket body from above into the L slot body of the lower package. Use a straight edge, such as a ruler, to bring all stacked units into uniform alignment. This technique prevents potential harm that could occur to fingers and hands of assemblers from the package pins. Stacked horizontal packages can be disengaged if necessary. Repeated stacking and unstacking causes no damage to individual units.

To stack vertical packages, hold one unit in each hand, with the pins facing away and the optical ports on the bottom. Slide the L bracket unit into the L slot unit. The straight edge used for horizontal package alignment is not needed.

Stacking Horizontal Modules



Stacking Vertical Modules

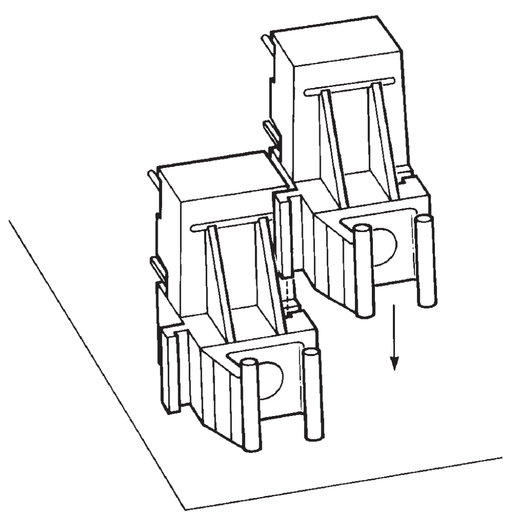


Figure 1. Interlocked (stacked) horizontal or vertical packages

5 MBd Link (HFBR-15X1Z/25X1Z)

System Performance 0 to 70°C unless otherwise specified.

	Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions	Ref.
High	Data Rate		dc		5	MBd	BER $\leq 10^{-9}$, PRBS:2^7-1	
Performance	Link Distance	ℓ	19			m	I_{Fdc} = 60 mA	Fig. 3
5 MBd	(Standard Cable)		27	48		m	I_{Fdc} = 60 mA, 25°C	Note 3
	Link Distance	ℓ	22			m	I_{Fdc} = 60 mA	Fig. 4
	(Improved Cable)		27	53		m	I_{Fdc} = 60 mA, 25°C	Note 3
	Propagation	t_{PLH}		80	140	ns	R_L = 560 Ω, C_L = 30 pF	Fig. 5, 8
	Delay	t_{PHL}		50	140	ns	fiber length = 0.5 m	Notes 1, 2
							-21.6 $\leq P_R \leq$ -9.5 dBm	
	Pulse Width	t_D		30		ns	P_R = -15 dBm	Fig. 5, 7
	Distortion t_{PLH}-t_{PHL}						R_L = 560 Ω, C_L = 30 pF	

Notes:
1. The propagation delay for one metre of cable is typically 5 ns.
2. Typical propagation delay is measured at P_R = -15 dBm.
3. Estimated typical link life expectancy at 40°C exceeds 10 years at 60 mA.

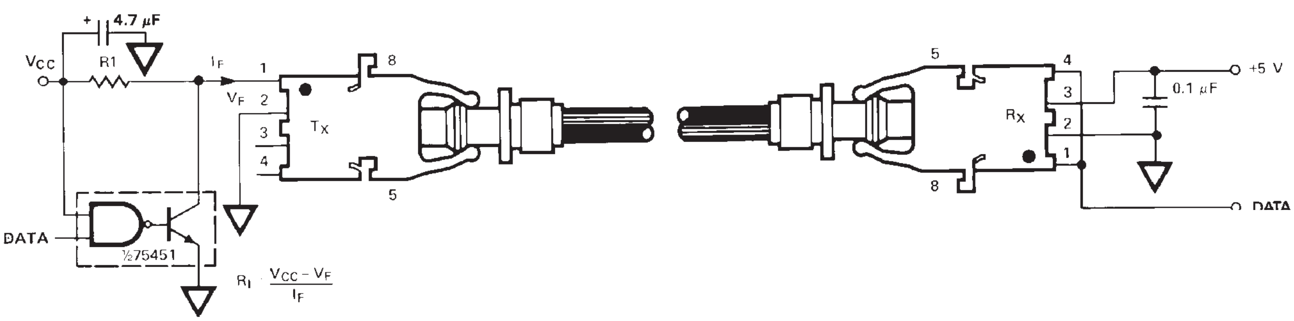


Figure 2. Typical 5 MBd interface circuit

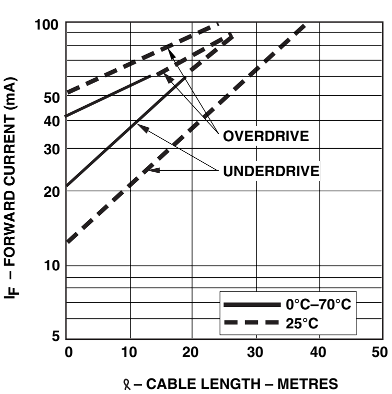


Figure 3. Guaranteed system performance with standard cable (HFBR-15X1Z/25X1Z)

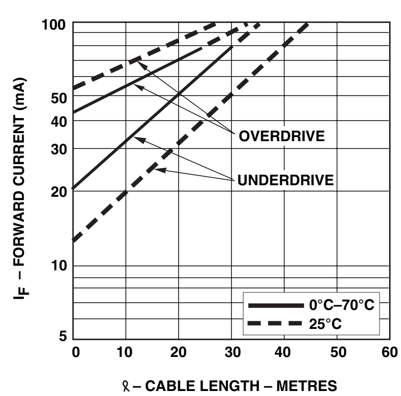


Figure 4. Guaranteed system performance with improved cable (HFBR-15X1Z/25X1Z)

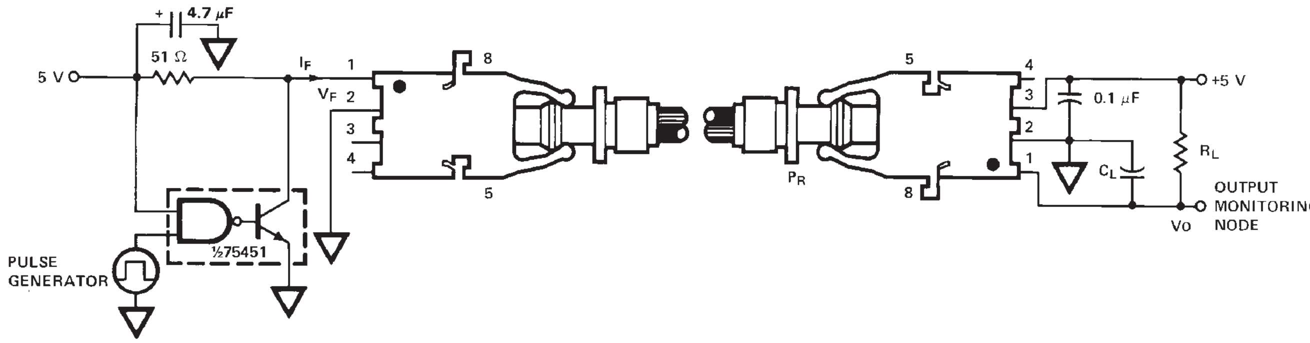


Figure 5. 5 MBd propagation delay test circuit

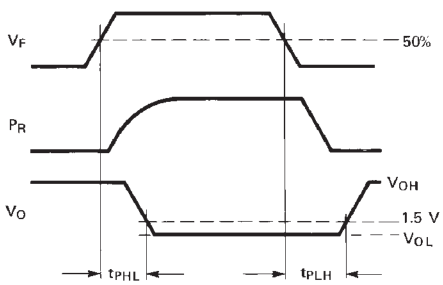


Figure 6. Propagation delay test waveforms

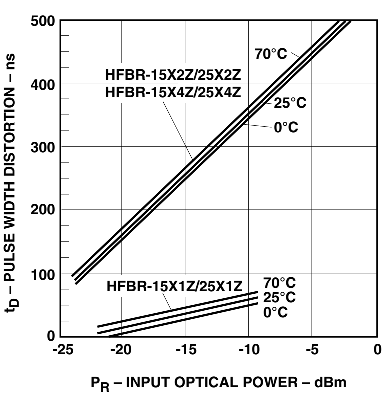


Figure 7. Typical link pulse width distortion vs. optical power

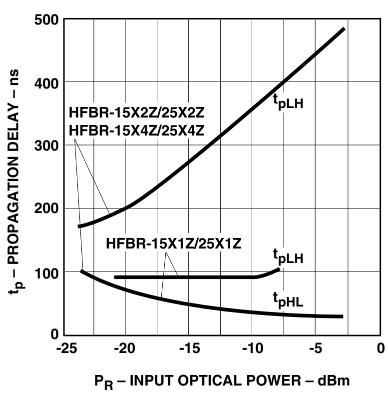
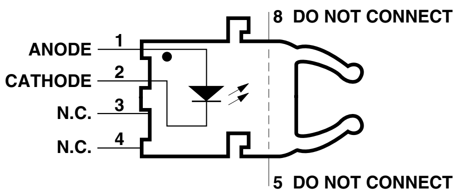


Figure 8. Typical link propagation delay vs. optical power

HFBR-15X1Z Transmitter



Pin #	Function
1	Anode
2	Cathode
3	Open
4	Open
5	Do not connect
8	Do not connect

Note: Pins 5 and 8 are for mounting and retaining purposes only. Do not electrically connect these pins.

Absolute Maximum Ratings

Parameter		Symbol	Min.	Max.	Units	Reference
Storage Temperature		T_S	–40	+85	°C	
Operating Temperature		T_A	–40	+85	°C	
Lead Soldering Cycle	Temp.			260	°C	Note 1, 4
	Time			10	sec	
Forward Input Current		I_{FPK}		1000	mA	Note 2, 3
		I_{Fdc}		80		
Reverse Input Voltage		V_{BR}		5	V	

Notes:
1. 1.6 mm below seating plane.
2. Recommended operating range between 10 and 750 mA.
3. 1 µs pulse, 20 µs period.
4. Moisture sensitivity level (MSL) is 3.

All HFBR-15XXZ LED transmitters are classified as IEC 825-1 Accessible Emission Limit (AEL) Class 1 based upon the current proposed draft scheduled to go into effect on January 1, 1997. AEL Class 1 LED devices are considered eye safe. Contact your local Avago sales representative for more information.

Transmitter Electrical/Optical Characteristics 0°C to 70°C unless otherwise specified.

Parameter	Symbol	Min.	Typ.[5]	Max.	Units	Conditions	Ref.
Transmitter Output Optical Power	P_T	-16.5		-7.6	dBm	I_{Fdc} = 60 mA	Notes 1, 2
		-14.3		-8.0	dBm	I_{Fdc} = 60 mA, 25°C	
Output Optical Power Temperature Coefficient	$\Delta P_T/\Delta T$		-0.85		%/°C		
Peak Emission Wavelength	λ_{PK}		660		nm		
Forward Voltage	V_F	1.45	1.67	2.02	V	I_{Fdc} = 60 mA	
Forward Voltage Temperature Coefficient	$\Delta V_F/\Delta T$		-1.37		mV/°C		Fig. 9
Effective Diameter	D		1		mm		
Numerical Aperture	NA		0.5				
Reverse Input Breakdown Voltage	V_{BR}	5.0	11.0		V	I_{Fdc} = 10 µA, T_A = 25°C	
Diode Capacitance	C_O		86		pF	V_F = 0, f = MHz	
Rise Time	t_r		80		ns	10% to 90%, I_F = 60 mA	Note 3
Fall Time	t_f		40		ns		

Notes:
1. Measured at the end of 0.5 m standard fiber optic cable with large area detector.
2. Optical power, P (dBm) = 10 Log [P(µW)/1000 µW].
3. Rise and fall times are measured with a voltage pulse driving the transmitter and a series connected 50 Ω load. A wide bandwidth optical to electrical waveform analyzer, terminated to a 50 Ω input of a wide bandwidth oscilloscope, is used for this response time measurement.

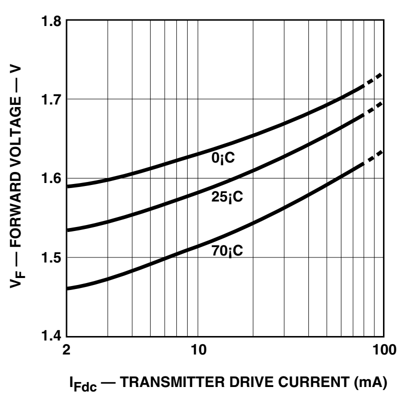


Figure 9. Typical forward voltage vs. drive current

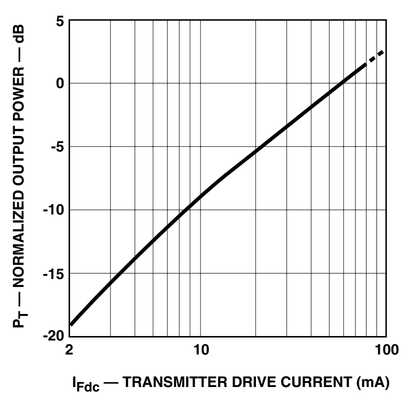
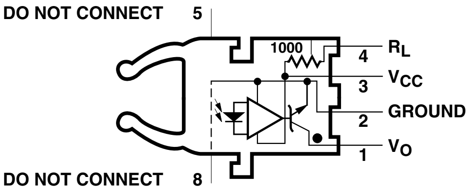


Figure 10. Normalized typical output power vs. drive current

HFBR-25X1Z Receiver



Pin #	Function
1	V_O
2	Ground
3	V_{CC}
4	R_L
5	Do not connect
8	Do not connect

Note: Pins 5 and 8 are for mounting and retaining purposes only. Do not electrically connect these pins.

Absolute Maximum Ratings

Parameter		Symbol	Min.	Max.	Units	Reference
Storage Temperature		T_S	–40	+85	°C	
Operating Temperature		T_A	–40	+85	°C	
Lead Soldering Cycle	Temp.			260	°C	Note 1, 3
	Time			10	sec	
Supply Voltage		V_{CC}	–0.5	7	V	Note 2
Output Collector Current		I_{OAV}		25	mA	
Output Collector Power Dissipation		P_{OD}		40	mW	
Output Voltage		V_O	–0.5	18	V	
Pull-up Voltage		V_P	–5	V_{CC}	V	
Fan Out (TTL)		N		5		

Notes:
1. 1.6 mm below seating plane.
2. It is essential that a bypass capacitor 0.1 µF be connected from pin 2 to pin 3 of the receiver. Total lead length between both ends of the capacitor and the pins should not exceed 20 mm.
3. Moisture sensitivity level (MSL) is 3.

Receiver Electrical/Optical Characteristics 0°C to 70°C, 4.75 V $\le V_{CC} \le$ 5.25 V unless otherwise specified.

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions	Ref.
Input Optical Power Level for Logic "0"	$P_{R(L)}$	–21.6		–9.5	dBm	V_{OL} = 0.5 V, I_{OL} = 8 mA	Notes 1, 2, 4
		–21.6		–8.7		V_{OL} = 0.5 V, I_{OL} = 8 mA, 25°C	
Input Optical Power Level for Logic "1"	$P_{R(H)}$			–43	dBm	V_{OL} = 5.25 V, $I_{OH} \le$ 250 µA	Note 1
High Level Output Current	I_{OH}		5	250	µA	V_O = 18 V, P_R = 0	Note 3
Low Level Output Current	V_{OL}		0.4	0.5	V	I_{OL} = 8 mA, $P_R = P_{R(L)MIN}$	Note 3
High Level Supply Current	I_{CCH}		3.5	6.3	mA	V_{CC} = 5.25 V, P_R = 0	Note 3
Low Level Supply Current	I_{CCL}		6.2	10	mA	V_{CC} = 5.25 V, P_R = -12.5 dBm	Note 3
Effective Diameter	D		1		mm		
Numerical Aperture	NA		0.5				
Internal Pull-up Resistor	R_L	680	1000	1700	Ω		

Notes:
1. Optical flux, P (dBm) = 10 Log [P (µW)/1000 µW].
2. Measured at the end of the fiber optic cable with large area detector.
3. R_L is open.
4. Pulsed LED operation at I_F > 80 mA will cause increased link t_{PLH} propagation delay time. This extended t_{PLH} time contributes to increased pulse width distortion of the receiver output signal.

1 MBd Link

(High Performance HFBR-15X2Z/25X2Z, Standard HFBR-15X4Z/25X4Z)

System Performance Under recommended operating conditions unless otherwise specified.

	Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions	Ref.
High Performance 1 MBd	Data Rate		dc		1	MBd	BER ≤10^{-9}, PRBS:2^7-1	
	Link Distance (Standard Cable)	ℓ	39 47	 70		m m	I_{Fdc} = 60 mA I_{Fdc} = 60 mA, 25°C	Fig. 14 Notes 1, 3, 4
	Link Distance (Improved Cable)	ℓ	45 56	 78		m m	I_{Fdc} = 60 mA I_{Fdc} = 60 mA, 25°C	Fig. 15 Notes 1, 3, 4
	Propagation Delay	t_{PLH} t_{PHL}		180 100	250 140	ns ns	R_L = 560 Ω, C_L = 30 pF l = 0.5 metre P_R = -24 dBm	Fig. 16, 18 Notes 2, 4
	Pulse Width Distortion t_{PLH}-t_{PHL}	t_D		80		ns	P_R = -24 dBm R_L = 560 Ω, C_L = 30 pF	Fig. 16, 17 Note 4

	Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions	Ref.
Standard 1 MBd	Data Rate		dc		1	MBd	BER ≤10^{-9}, PRBS:2^7-1	
	Link Distance (Standard Cable)	ℓ	8 17	 43		m m	I_{Fdc} = 60 mA I_{Fdc} = 60 mA, 25°C	Fig. 12 Notes 1, 3, 4
	Link Distance (Improved Cable)	ℓ	10 19	 48		m m	I_{Fdc} = 60 mA I_{Fdc} = 60 mA, 25°C	Fig. 13 Notes 1, 3, 4
	Propagation Delay	t_{PLH} t_{PHL}		180 100	250 140	ns ns	R_L = 560 Ω, C_L = 30 pF l = 0.5 metre P_R = -20 dBm	Fig. 16, 18 Notes 2, 4
	Pulse Width Distortion t_{PLH}-t_{PHL}	t_D		80		ns	P_R = -20 dBm R_L = 560 Ω, C_L = 30 pF	Fig. 16, 17 Note 4

Notes:

1. For I_{FPK} > 80 mA, the duty factor must be such as to keep I_{Fdc} ≤80 mA. In addition, for I_{FPK} > 80 mA, the following rules for pulse width apply:
   I_{FPK} ≤160 mA: Pulse width ≤1 ms
   I_{FPK} > 160 mA: Pulse width ≤1 µS, period ≥20 µS.
2. The propagation delay for one meter of cable is typically 5 ns.
3. Estimated typical link life expectancy at 40°C exceeds 10 years at 60 mA.
4. Pulsed LED operation at I_{FPK} > 80 mA will cause increased link t_{PLH} propagation delay time. This extended t_{PLH} time contributes to increased pulse width distortion of the receiver output signal.

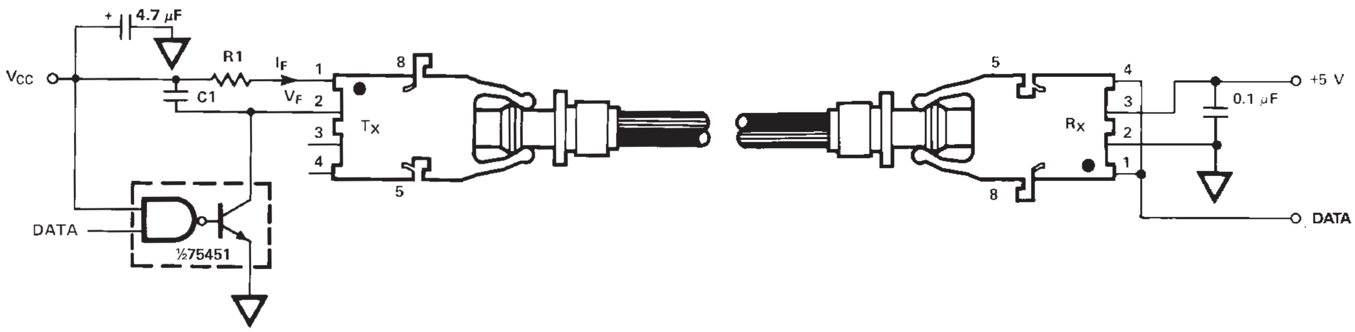


Figure 11. Required 1 MBd interface circuit

The HFBR-25X2Z receiver cannot be overdriven when using the required interface circuit shown in Figure 11

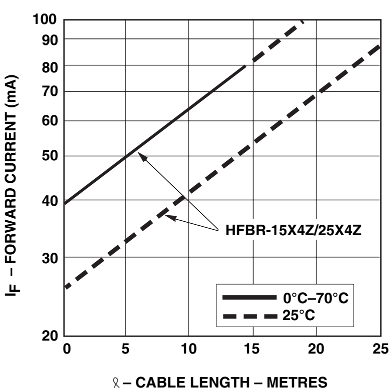


Figure 12. Guaranteed system performance for the HFBR-15X4Z/25X4Z link with standard cable

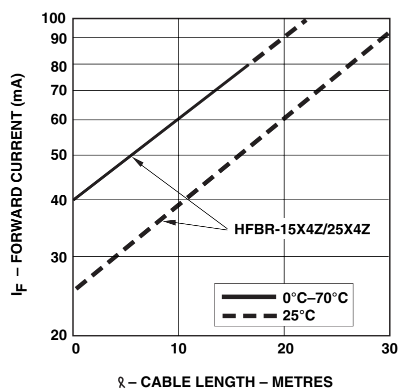


Figure 13. Guaranteed system performance for the HFBR-15X4Z/25X4Z link with improved cable

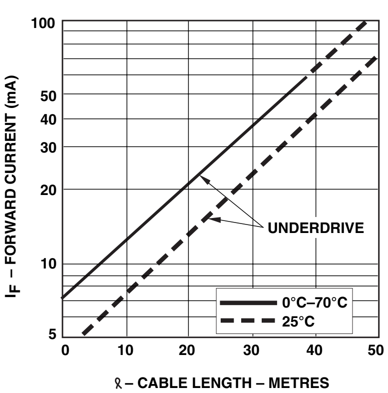


Figure 14. Guaranteed system performance for the HFBR-15X2Z/25X2Z link with standard cable

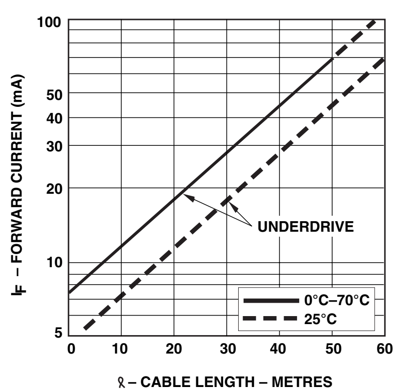


Figure 15. Guaranteed system performance for the HFBR-15X2Z/25X2Z link with improved cable

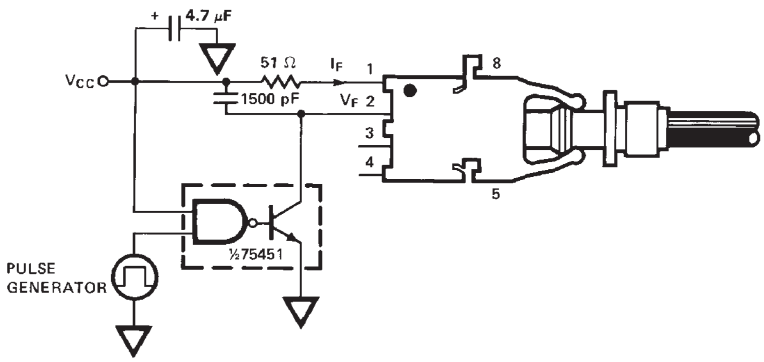


Figure 16. 1 MBd propagation delay test circuit

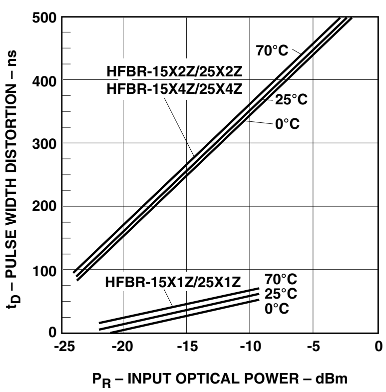


Figure 17. Pulse width distortion vs. optical power

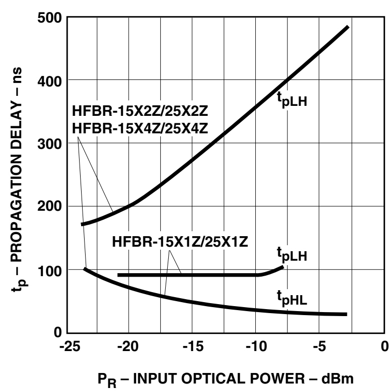


Figure 18. Typical link propagation delay vs. optical power

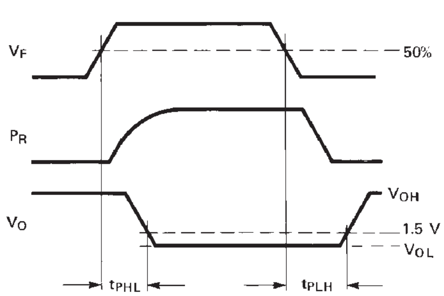
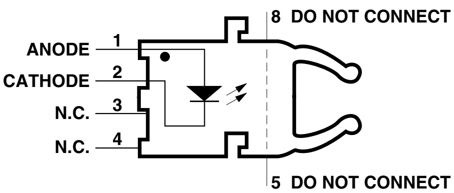


Figure 19. Propagation delay test waveforms

HFBR-15X2Z/15X4Z Transmitters



Pin #	Function
1	Anode
2	Cathode
3	Open
4	Open
5	Do not connect
8	Do not connect

Note: Pins 5 and 8 are for mounting and retaining purposes only. Do not electrically connect these pins.

Absolute Maximum Ratings

Parameter		Symbol	Min.	Max.	Units	Reference
Storage Temperature		T_S	–40	+85	°C	
Operating Temperature		T_A	–40	+85	°C	
Lead Soldering Cycle	Temp.			260	°C	Note 1, 4
	Time			10	sec	
Forward Input Current		I_{FPK}		1000	mA	Note 2, 3
		I_{Fdc}		80		
Reverse Input Voltage		V_{BR}		5	V	

Notes:
1. 1.6 mm below seating plane.
2. Recommended operating range between 10 and 750 mA.
3. 1 µs pulse, 20 µs period.
4. Moisture sensitivity level (MSL) is 3.

All HFBR-15XXZ LED transmitters are classified as IEC 825-1 Accessible Emission Limit (AEL) Class 1 based upon the current proposed draft scheduled to go into effect on January 1, 1997. AEL Class 1 LED devices are considered eye safe. Contact your Avago sales representative for more information.

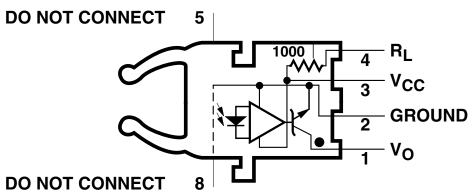
Transmitter Electrical/Optical Characteristics 0°C to 70°C unless otherwise specified.

For forward voltage and output power vs. drive current graphs.

Parameter		Symbol	Min.	Typ.	Max.	Units	Conditions	Ref.
Transmitter Output	HFBR-15X2Z	P_T	–13.6		–4.5	dBm	I_{Fdc} = 60 mA	
			–11.2		–5.1		I_{Fdc} = 60 mA, 25°C	
Optical Power	HFBR-15X4Z	P_T	–17.8		–4.5	dBm	I_{Fdc} = 60 mA	
			–15.5		–5.1		I_{Fdc} = 60 mA, 25°C	
Output Optical Power Temperature Coefficient		$\Delta P_T/\Delta T$		–0.85		%/°C		
Peak Emission Wavelength		λ_{PK}		660		nm		
Forward Voltage		V_F	1.45	1.67	2.02	V	I_{Fdc} = 60 mA	
Forward Voltage Temperature Coefficient		$\Delta V_F/\Delta T$		–1.37		mV/°C		Fig. 11
Effective Diameter		D_T		1		mm		
Numerical Aperture		NA		0.5				
Reverse Input Breakdown Voltage		V_{BR}	5.0	11.0		V	I_{Fdc} = 10 µA, T_A = 25°C	
Diode Capacitance		C_O		86		pF	V_F = 0, f = 1 MHz	
Rise Time		t_r		80		ns	10% to 90%,	Note 1
Fall Time		t_f		40		ns	I_F = 60 mA	

Note:
1. Rise and fall times are measured with a voltage pulse driving the transmitter and a series connected 50 Ω load. A wide bandwidth optical to electrical waveform analyzer, terminated to a 50 Ω input of a wide bandwidth oscilloscope, is used for this response time measurement.

HFBR-25X2Z/25X4Z Receivers



Pin #	Function
1	V_O
2	Ground
3	V_{CC}
4	R_L
5	Do not connect
8	Do not connect

Note: Pins 5 and 8 are for mounting and retaining purposes only. Do not electrically connect these pins.

Absolute Maximum Ratings

Parameter		Symbol	Min.	Max.	Units	Reference
Storage Temperature		T_S	–40	+85	°C	
Operating Temperature		T_A	–40	+85	°C	
Lead Soldering Cycle	Temp.			260	°C	Note 1, 3
	Time			10	sec	
Supply Voltage		V_{CC}	–0.5	7	V	Note 2
Output Collector Current		I_{OAV}		25	mA	
Output Collector Power Dissipation		P_{OD}		40	mW	
Output Voltage		V_O	–0.5	18	V	
Pull-up Voltage		V_P	–5	V_{CC}	V	
Fan Out (TTL)		N		5		

Notes:
1. 1.6 mm below seating plane.
2. It is essential that a bypass capacitor 0.1 µF be connected from pin 2 to pin 3 of the receiver. Total lead length between both ends of the capacitor and the pins should not exceed 20 mm.
3. Moisture sensitivity level (MSL) is 3.

Receiver Electrical/Optical Characteristics 0°C to 70°C, 4.75 V $\leq V_{CC} \leq$ 5.25 V unless otherwise specified.

Parameter		Symbol	Min.	Typ.	Max.	Units	Conditions	Ref.
Receiver Optical Input Power Level Logic 0	HFBR-2522Z	$P_{R(L)}$	–24			dBm	V_{OL} = 0 V, I_{OL} = 8 mA	Notes 1, 2, 3
	HFBR-2524Z		–20					Note 4
Optical Input Power Level Logic 1		$P_{R(H)}$			-43	dBm	V_{OH} = 5.25 V, I_{OH} = ≤250 µA	
High Level Output Current		I_{OH}		5	250	µA	V_O = 18 V, P_R = 0	Note 5
Low Level Output Voltage		V_{OL}		0.4	0.5	V	I_{OL} = 8 mA, $P_R = P_{R(L)MIN}$	Note 5
High Level Supply Current		I_{CCH}		3.5	6.3	mA	V_{CC} = 5.25 V, P_R = 0	Note 5
Low Level Supply Current		I_{CCL}		6.2	10	mA	V_{CC} = 5.25 V, P_R = -12.5 dBm	Note 5
Effective Diameter		D		1		mm		
Numerical Aperture		NA		0.5				
Internal Pull-up Resistor		R_L	680	1000	1700	Ω		

Notes:
1. Measured at the end of the fiber optic cable with large area detector.
2. Pulsed LED operation at I_F > 80 mA will cause increased link t_{PLH} propagation delay time. This extended t_{PLH} time contributes to increased pulse width distortion of the receiver output signal.
3. The LED drive circuit of Figure 11 is required for 1 MBd operation of the HFBR-25X2Z/25X4Z.
4. Optical flux, P (dBm) = 10 Log [P(µW)/1000 µW].
5. R_L is open.

40 kBd Link

System Performance Under recommended operating conditions unless otherwise specified.

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions	Ref.
Data Rate		dc		40	kBd	BER $\leq 10^{-9}$, PRBS: 2^7 - 1	
Link Distance (Standard Cable)	ℓ	13	41		m	I_{Fdc} = 2 mA	Fig. 21
		94	138		m	I_{Fdc} = 60 mA	Note 1
Link Distance (Improved Cable)	ℓ	15	45		m	I_{Fdc} = 2 mA	Fig. 22
		111	154		m	I_{Fdc} = 60 mA	Note 1
Propagation Delay	t_{PLH}		4		µs	R_L = 3.3 kΩ, C_L = 30 pF	Fig. 22, 25
	t_{PHL}		2.5		µs	P_R = -25 dBm, 1 m fiber	Note 2
Pulse Width Distortion t_{PLH}-t_{PHL}	t_D			7	µs	-39 $\leq P_R \leq$ - 14 dBm, R_L = 3.3 kΩ, C_L = 30 pF	Fig. 23, 24

Notes:

1. Estimated typical link life expectancy at 40°C exceeds 10 years at 60 mA.
2. The propagation delay for one metre of cable is typically 5 ns.

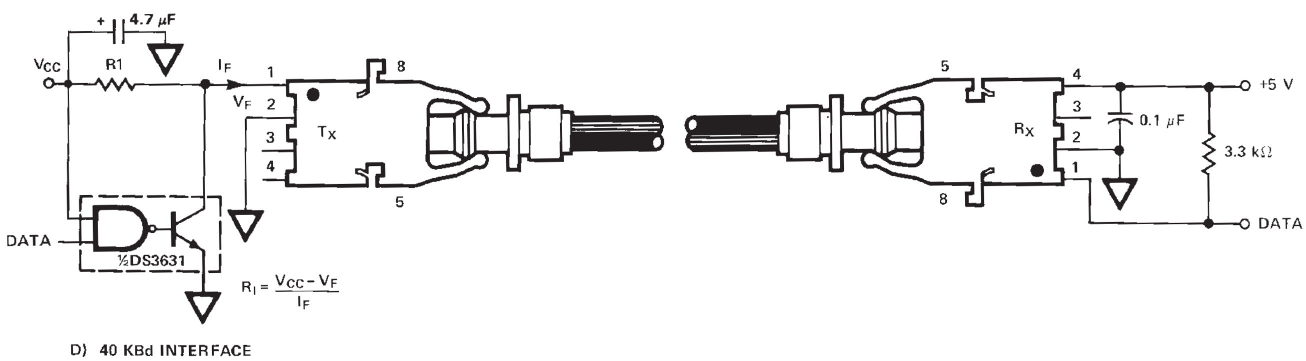


Figure 20. Typical 40 kBd interface circuit

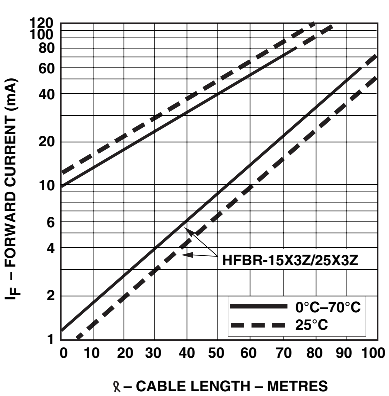


Figure 21. Guaranteed system performance with standard cable

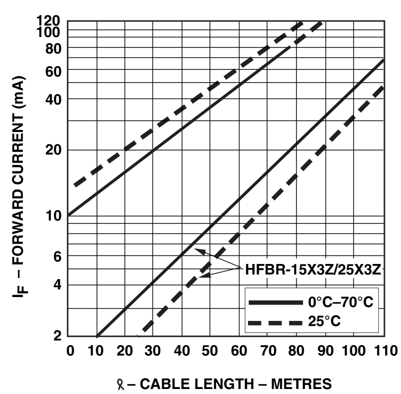


Figure 22. Guaranteed system performance with improved cable

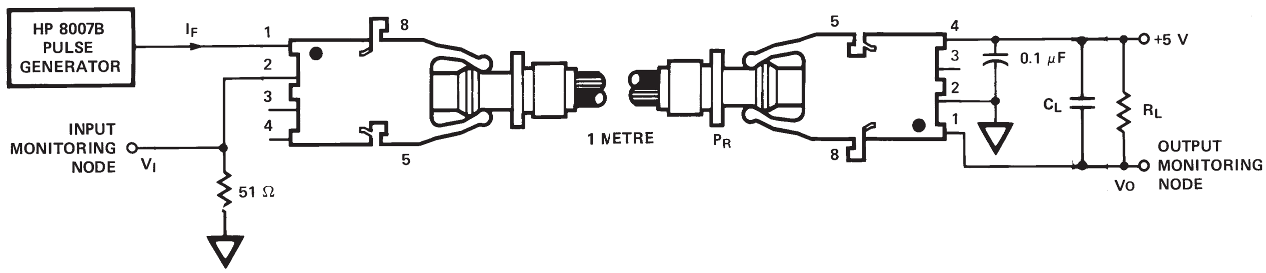


Figure 23. 40 kBd propagation delay test circuit

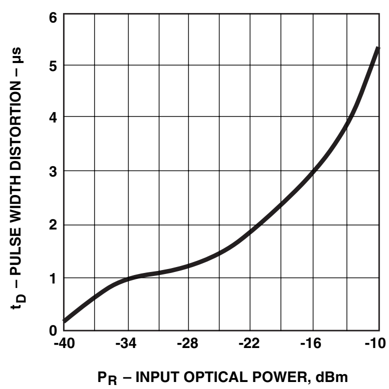


Figure 24. Typical link pulse width distortion vs. optical power

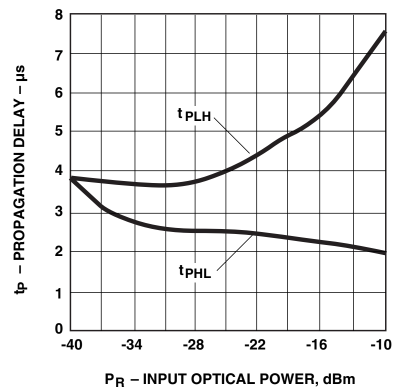


Figure 25. Typical link propagation delay vs. optical power

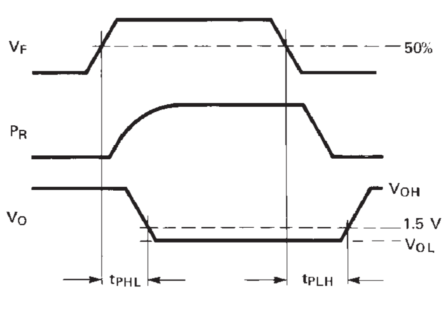
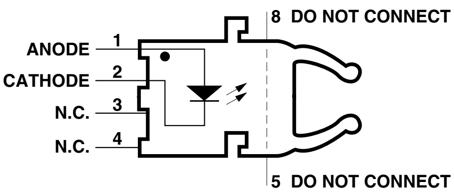


Figure 26. Propagation delay test waveforms

HFBR-15X3Z Transmitter



Pin #	Function
1	Anode
2	Cathode
3	Open
4	Open
5	Do not connect
8	Do not connect

Note: Pins 5 and 8 are for mounting and retaining purposes only. Do not electrically connect these pins.

Absolute Maximum Ratings

Parameter		Symbol	Min.	Max.	Units	Reference
Storage Temperature		T_S	–40	+85	°C	
Operating Temperature		T_A	–40	+85	°C	
Lead Soldering Cycle	Temp.			260	°C	Note 1, 4
	Time			10	sec	
Forward Input Current		I_{FPK}		1000	mA	Note 2, 3
		I_{Fdc}		80		
Reverse Input Voltage		V_{BR}		5	V	

Notes:
1. 1.6 mm below seating plane.
2. Recommended operating range between 10 and 750 mA.
3. 1 µs pulse, 20 µs period.
4. Moisture sensitivity level (MSL) is 3.

All HFBR-15XXZ LED transmitters are classified as IEC 825-1 Accessible Emission Limit (AEL) Class 1 based upon the current proposed draft scheduled to go into effect on January 1, 1997. AEL Class 1 LED devices are considered eye safe. Contact your Avago sales representative for more information.

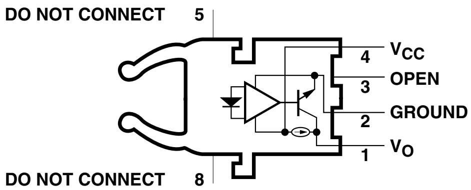
Transmitter Electrical/Optical Characteristics 0°C to 70°C unless otherwise specified.

For forward voltage and output power vs. drive current graphs.

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions	Ref.
Transmitter Output Optical Power	P_T	–11.2 –13.6 –35.5		–5.1 –4.5	dBm	I_{Fdc} = 60 mA, 25°C I_{Fdc} = 60 mA I_{Fdc} = 2 mA, 0-70°C	Notes 3, 4 Fig. 9, 10
Output Optical Power Temperature Coefficient	$\Delta P_T/\Delta T$		–0.85		%/°C		
Peak Emission Wavelength	λ_{PK}		660		nm		
Forward Voltage	V_F	1.45	1.67	2.02	V	I_{Fdc} = 60 mA	
Forward Voltage Temperature Coefficient	$\Delta V_F/\Delta T$		–1.37		mV/°C		Fig. 18
Effective Diameter	D		1		mm		
Numerical Aperture	NA		0.5				
Reverse Input Breakdown Voltage	V_{BR}	5.0	11.0		V	I_{Fdc} = 10 µA, T_A = 25°C	
Diode Capacitance	C_O		86		pF	V_F = 0, f = 1 MHz	
Rise Time	t_r		80		ns	10% to 90%,	Note 1
Fall Time	t_f		40			I_F = 60 mA	

Note:
1. Rise and fall times are measured with a voltage pulse driving the transmitter and a series connected 50 Ω load. A wide bandwidth optical to electrical waveform analyzer, terminated to a 50 Ω input of a wide bandwidth oscilloscope, is used for this response time measurement.

HFBR-25X3Z Receiver



Pin #	Function
1	V_O
2	Ground
3	Open
4	V_{CC}
5	Do not connect
8	Do not connect

Note: Pins 5 and 8 are for mounting and retaining purposes only. Do not electrically connect these pins.

Absolute Maximum Ratings

Parameter		Symbol	Min.	Max.	Units	Reference
Storage Temperature		T_S	–40	+85	°C	
Operating Temperature		T_A	–40	+85	°C	
Lead Soldering Cycle	Temp.			260	°C	Note 1, 3
	Time			10	sec	
Supply Voltage		V_{CC}	–0.5	7	V	Note 2
Average Output Collector Current		I_O	–1	5	mA	
Output Collector Power Dissipation		P_{OD}		25	mW	
Output Voltage		V_O	–0.5	7	V	

Notes:
1. 1.6 mm below seating plane.
2. It is essential that a bypass capacitor 0.1 µF be connected from pin 2 to pin 4 of the receiver.
3. Moisture sensitivity level (MSL) is 3.

Receiver Electrical/Optical Characteristics 0°C to 70°C, 4.5 V ≤V_{CC} ≤5.5 V unless otherwise specified.

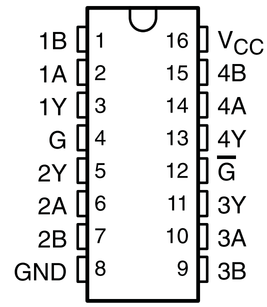
Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions	Ref.
Input Optical Power Level Logic 0	$P_{R(L)}$	–39		–13.7	dBm	$V_O = V_{OL}$, I_{OL} = 3.2 mA	Notes 1, 2, 3
		–39		–13.3		$V_O = V_{OL}$, I_{OH} = 8 mA, 25°C	
Input Optical Power Level Logic 1	$P_{R(H)}$			–53	dBm	V_{OH} = 5.5 V, I_{OH} = ≤40 µA	Note 3
High Level Output Voltage	V_{OH}	2.4			V	I_O = -40 µA, P_R = 0 µW	
Low Level Output Voltage	V_{OL}			0.4	V	I_{OL} = 3.2 mA, $P_R = P_{R(L)MIN}$	Note 4
High Level Supply Current	I_{CCH}		1.2	1.9	mA	V_{CC} = 5.5 V, P_R = 0 µW	
Low Level Supply Current	I_{CCL}		2.9	3.7	mA	V_{CC} = 5.5 V, $P_R = P_{RL}$ (MIN)	Note 4
Effective Diameter	D		1		mm		
Numerical Aperture	NA		0.5				

Notes:
1. Measured at the end of the fiber optic cable with large area detector.
2. Optical flux, P (dBm) = 10 Log P(µW)/1000 µW.
3. Because of the very high sensitivity of the HFBR-25X3Z, the digital output may switch in response to ambient light levels when a cable is not occupying the receiver optical port. The designer should take care to filter out signals from this source if they pose a hazard to the system.
4. Including current in 3.3 k pull-up resistor.

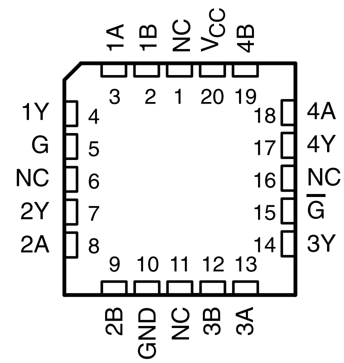
FEATURES

- **AM26LS32A Devices Meet or Exceed the Requirements of ANSI TIA/EIA-422-B, TIA/EIA-423-B, and ITU Recommendations V.10 and V.11**
- **AM26LS32A Devices Have ±7-V Common-Mode Range With ±200-mV Sensitivity**
- **AM26LS33A Devices Have ±15-V Common-Mode Range With ±500-mV Sensitivity**
- **Input Hysteresis . . . 50 mV Typical**
- **Operate From a Single 5-V Supply**
- **Low-Power Schottky Circuitry**
- **3-State Outputs**
- **Complementary Output-Enable Inputs**
- **Input Impedance . . . 12 kΩ Minimum**
- **Designed to Be Interchangeable With Advanced Micro Devices AM26LS32™ and AM26LS33™**

AM26LS32AC . . . D, N, NS, OR PW PACKAGE
AM26LS32AI, AM26LS33AC . . . D, OR N PACKAGE
AM26LS32AM, AM26LS33AM . . .J PACKAGE
(TOP VIEW)



AM26LS32AM, AM26LS33AM . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

DESCRIPTION

The AM26LS32A and AM26LS33A devices are quadruple differential line receivers for balanced and unbalanced digital data transmission. The enable function is common to all four receivers and offers a choice of active-high or active-low input. The 3-state outputs permit connection directly to a bus-organized system. Fail-safe design ensures that, if the inputs are open, the outputs always are high.

Compared to the AM26LS32 and the AM26LS33, the AM26LS32A and AM26LS33A incorporate an additional stage of amplification to improve sensitivity. The input impedance has been increased, resulting in less loading of the bus line. The additional stage has increased propagation delay; however, this does not affect interchangeability in most applications.

The AM26LS32AC and AM26LS33AC are characterized for operation from 0°C to 70°C. The AM26LS32AI is characterized for operation from –40°C to 85°C. The AM26LS32AM and AM26LS33AM are characterized for operation over the full military temperature range of –55°C to 125°C.

MC14043B, MC14044B

CMOS MSI

Quad R−S Latches

The MC14043B and MC14044B quad R−S latches are constructed with MOS P−Channel and N−Channel enhancement mode devices in a single monolithic structure. Each latch has an independent Q output and set and reset inputs. The Q outputs are gated through three−state buffers having a common enable input. The outputs are enabled with a logical “1” or high on the enable input; a logical “0” or low disconnects the latch from the Q outputs, resulting in an open circuit at the Q outputs.

Features

- Double Diode Input Protection
- Three−State Outputs with Common Enable
- Outputs Capable of Driving Two Low−power TTL Loads or One Low−Power Schottky TTL Load Over the Rated Temperature Range
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- These Devices are Pb−Free and are RoHS Compliant
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable

MAXIMUM RATINGS (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage Range	−0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage Range (DC or Transient)	−0.5 to V_{DD} + 0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient) per Pin	±10	mA
P_D	Power Dissipation, per Package (Note 1)	500	mW
T_A	Ambient Temperature Range	−55 to +125	°C
T_{stg}	Storage Temperature Range	−65 to +150	°C
T_L	Lead Temperature (8−Second Soldering)	260	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Temperature Derating:
   Plastic “P and D/DW” Packages: – 7.0 mW/°C From 65°C To 125°C

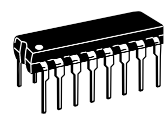
This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high−impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

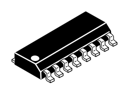
ON Semiconductor®

http://onsemi.com

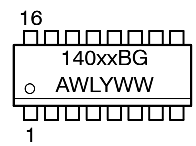
MARKING DIAGRAMS

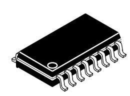


PDIP−16
P SUFFIX
CASE 648

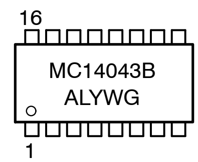


SOIC−16
D SUFFIX
CASE 751B





SOEIAJ−16
F SUFFIX
CASE 966



xx	=	Specific Device Code
A	=	Assembly Location
WL, L	=	Wafer Lot
YY, Y	=	Year
WW, W	=	Work Week
G	=	Pb−Free Indicator

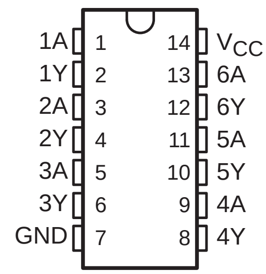
ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

The SN54LS07 and SN74LS17 are obsolete and are no longer supplied.

- **Convert TTL Voltage Levels to MOS Levels**
- **High Sink-Current Capability**
- **Input Clamping Diodes Simplify System Design**
- **Open-Collector Driver for Indicator Lamps and Relays**

SN54LS07 . . . J PACKAGE
SN74LS07, SN74LS17 . . . D, DB, N, OR NS PACKAGE
(TOP VIEW)



description/ordering information

These hex buffers/drivers feature high-voltage open-collector outputs to interface with high-level circuits or for driving high-current loads. They are also characterized for use as buffers for driving TTL inputs. The ’LS07 devices have a rated output voltage of 30 V, and the SN74LS17 has a rated output voltage of 15 V. The maximum sink current is 30 mA for the SN54LS07 and 40 mA for the SN74LS07 and SN74LS17.

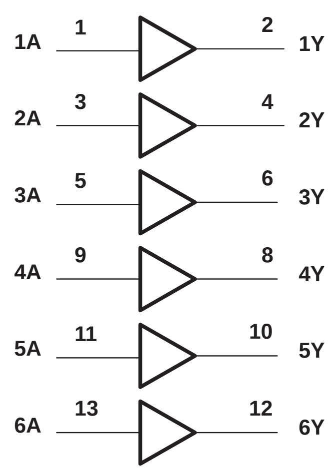
These circuits are compatible with most TTL families. Inputs are diode-clamped to minimize transmission-line effects, which simplifies design. Typical power dissipation is 140 mW, and average propagation delay time is 12 ns.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	PDIP − N	Tube	SN74LS07N	SN74LS07N
	SOIC − D	Tube	SN74LS07D	LS07
		Tape and reel	SN74LS07DR	
	SOP − NS	Tape and reel	SN74LS07NSR	74LS07
	SSOP − DB	Tape and reel	SN74LS07DBR	LS07

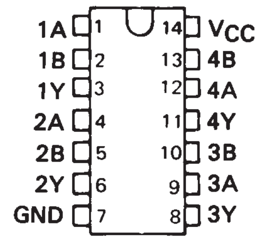
† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

logic diagram (positive logic)

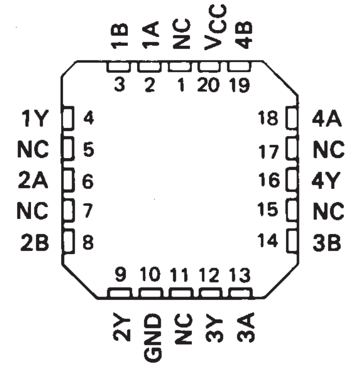


- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers and Flat Packages, and Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN5408, SN54LS08, SN54S08 . . . J OR W PACKAGE
SN7408 . . . J OR N PACKAGE
SN74LS08, SN74S08 . . . D, J OR N PACKAGE
(TOP VIEW)



SN54LS08, SN54S08 . . . FK PACKAGE
(TOP VIEW)



NC—No internal connection

description

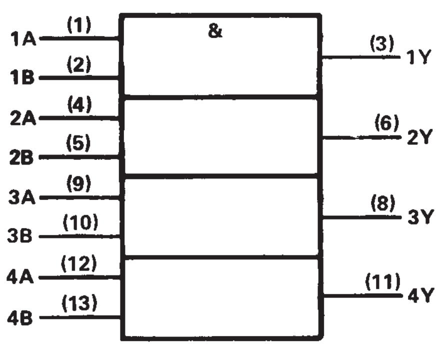
These devices contain four independent 2-input AND gates.

The SN5408, SN54LS08, and SN54S08 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN7408, SN74LS08 and SN74S08 are characterized for operation from 0° to 70°C.

FUNCTION TABLE (each gate)

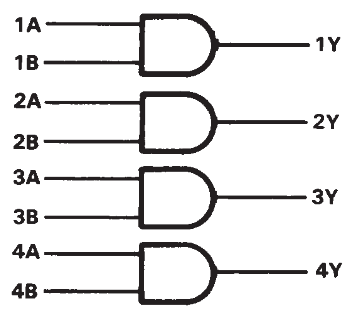
INPUTS		OUTPUT
A	B	Y
H	H	H
L	X	L
X	L	L

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, N, and W packages.

logic diagram (positive logic)

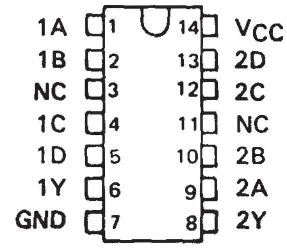


$Y = A \cdot B$ or $Y = \overline{\overline{A} + \overline{B}}$

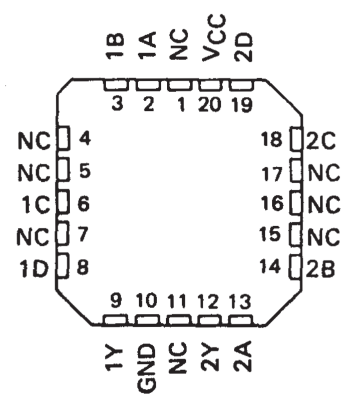
PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

- **Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers and Flat Packages, and Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

SN54LS21 . . . J OR W PACKAGE
SN74LS21 . . . D OR N PACKAGE
(TOP VIEW)



SN54LS21 . . . FK PACKAGE
(TOP VIEW)



NC–No internal connection

description

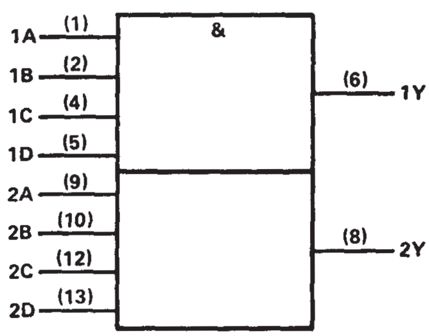
These devices contain two independent 4-input AND gates.

The SN54LS21 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74LS21 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE (each gate)

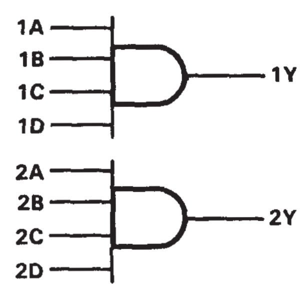
INPUTS				OUTPUT
A	B	C	D	Y
H	H	H	H	H
L	X	X	X	L
X	L	X	X	L
X	X	L	X	L
X	X	X	L	L

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for D, J, N, and W packages.

logic diagram



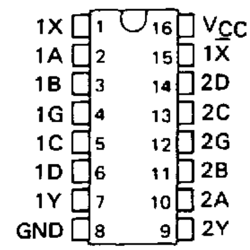
(positive logic) $Y = A \bullet B \bullet C \bullet D$ or $Y = \overline{\overline{A} + \overline{B} + \overline{C} + \overline{D}}$

SN5423, SN5425, SN7423, SN7425
DUAL 4-INPUT NOR GATES WITH STROBE

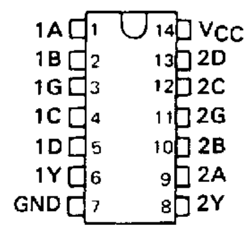
DECEMBER 1983—REVISED MARCH 1988

- **Package Options Include Plastic and Ceramic DIPs and Ceramic Flat Packages**
- **Dependable Texas Instruments Quality and Reliability**

SN5423 . . . J OR W PACKAGE
SN7423 . . . N PACKAGE
(TOP VIEW)



SN5425 . . . J OR W PACKAGE
SN7425 . . . N PACKAGE
(TOP VIEW)



description

These devices contain dual 4-input positive NOR gates with strobe. They perform the Boolean function:

$$Y = \overline{G(A+B+C+D)}$$

(with 1X and $1\overline{X}$ of '23 left open).

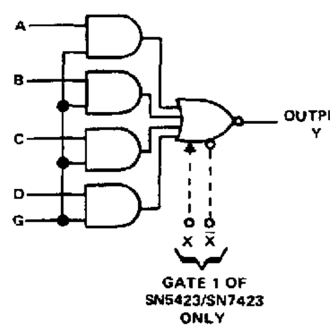
The SN5423 and the SN5425 are characterized for operation over the full military temperature range of −55°C to 125°C. The SN7423 and the SN7425 are characterized for operation from 0°C to 70°C.

FUNCTION TABLE

INPUTS					OUTPUT
A	B	C	D	G	Y
H	X	X	X	H	L
X	H	X	X	H	L
X	X	H	X	H	L
X	X	X	H	H	L
L	L	L	L	X	H
X	X	X	X	L	H

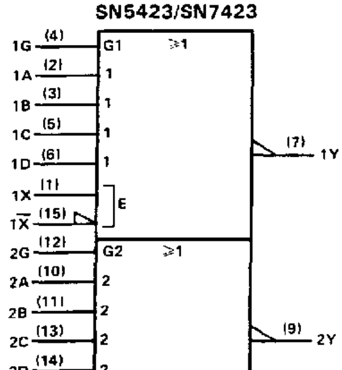
Expander inputs are open.
H = high level, L = low level, X = irrelevant

logic diagram

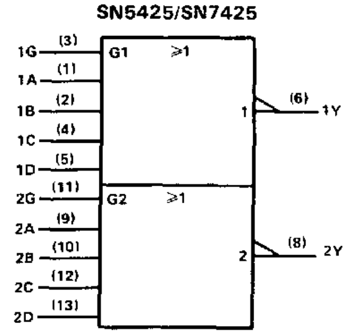


logic symbols†

SN5423/SN7423



SN5425/SN7425



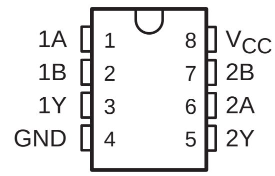
†These symbols are in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.
Pin numbers are for J, N, or W packages.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

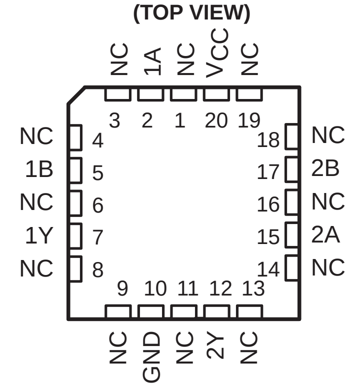
PERIPHERAL DRIVERS FOR HIGH-CURRENT SWITCHING AT VERY HIGH SPEEDS

- **Characterized for Use to 300 mA**
- **High-Voltage Outputs**
- **No Output Latch-Up at 20 V (After Conducting 300 mA)**
- **High-Speed Switching**
- **Circuit Flexibility for Varied Applications**
- **TTL-Compatible Diode-Clamped Inputs**
- **Standard Supply Voltages**
- **Plastic DIP (P) With Copper Lead Frame Provides Cooler Operation and Improved Reliability**
- **Package Options Include Plastic Small-Outline Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs**

SN55451B, SN55452B,
SN55453B, SN55454B . . . JG PACKAGE
SN75451B, SN75452B,
SN75453B, SN75454B . . . D OR P PACKAGE
(TOP VIEW)



SN55451B, SN55452B
SN55453B, SN55454B . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

SUMMARY OF DEVICES

DEVICE	LOGIC OF COMPLETE CIRCUIT	PACKAGES
SN55451B	AND	FK, JG
SN55452B	NAND	JG
SN55453B	OR	FK, JG
SN55454B	NOR	JG
SN75451B	AND	D, P
SN75452B	NAND	D, P
SN75453B	OR	D, P
SN75454B	NOR	D, P

description

The SN55451B through SN55454B and SN75451B through SN75454B are dual peripheral drivers designed for use in systems that employ TTL logic. This family is functionally interchangeable with and replaces the SN75450 family and the SN75450A family devices manufactured previously. The speed of the devices is equal to that of the SN75450 family, and the parts are designed to ensure freedom from latch-up. Diode-clamped inputs simplify circuit design. Typical applications include high-speed logic buffers, power drivers, relay drivers, lamp drivers, MOS drivers, line drivers, and memory drivers.

The SN55451B/SN75451B, SN55452B/SN75452B, SN55453B/SN75453B, and SN55454B/SN75454B are dual peripheral AND, NAND, OR, and NOR drivers, respectively (assuming positive logic), with the output of the logic gates internally connected to the bases of the npn output transistors.

The SN55’ drivers are characterized for operation over the full military range of –55°C to 125°C. The SN75’ drivers are characterized for operation from 0°C to 70°C.

TL082 Wide Bandwidth Dual JFET Input Operational Amplifier

Check for Samples: TL082-N

FEATURES

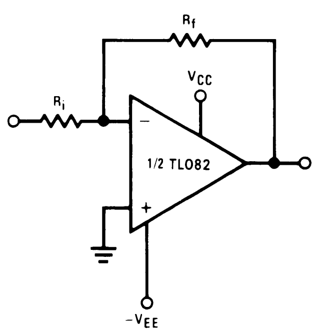
- **Internally Trimmed Offset Voltage: 15 mV**
- **Low Input Bias Current: 50 pA**
- **Low Input Noise Voltage: 16nV/√Hz**
- **Low Input Noise Current: 0.01 pA/√Hz**
- **Wide Gain Bandwidth: 4 MHz**
- **High Slew Rate: 13 V/μs**
- **Low Supply Current: 3.6 mA**
- **High Input Impedance: $10^{12}\Omega$**
- **Low Total Harmonic Distortion: ≤0.02%**
- **Low 1/f Noise Corner: 50 Hz**
- **Fast Settling Time to 0.01%: 2 μs**

DESCRIPTION

These devices are low cost, high speed, dual JFET input operational amplifiers with an internally trimmed input offset voltage (BI-FET II™ technology). They require low supply current yet maintain a large gain bandwidth product and fast slew rate. In addition, well matched high voltage JFET input devices provide very low input bias and offset currents. The TL082 is pin compatible with the standard LM1558 allowing designers to immediately upgrade the overall performance of existing LM1558 and most LM358 designs.

These amplifiers may be used in applications such as high speed integrators, fast D/A converters, sample and hold circuits and many other circuits requiring low input offset voltage, low input bias current, high input impedance, high slew rate and wide bandwidth. The devices also exhibit low noise and offset voltage drift.

Typical Connection



Connection Diagram

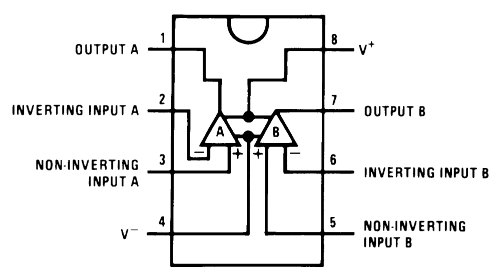
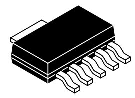


Figure 1. PDIP/SOIC Package (Top View)
See Package Number D0008A or P0008E



SLVS350A – OCTOBER 2002 – REVISED MARCH 2003

ULTRALOW-NOISE, HIGH PSRR, FAST RF 500-mA LOW-DROPOUT LINEAR REGULATORS

FEATURES

- **500-mA Low-Dropout Regulator With EN**
- **Available in 1.6-V, 1.8-V, 2.5-V, 3-V, 3.3-V, and Adjustable**
- **High PSRR (50 dB at 10 kHz)**
- **Ultralow Noise (33 μV)**
- **Fast Start-Up Time (50 μs)**
- **Stable With a 1-μF Ceramic Capacitor**
- **Excellent Load/Line Transient**
- **Very Low Dropout Voltage (110 mV at Full Load, TPS79530)**
- **5-Pin SOT223–5 Package**

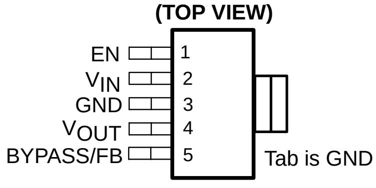
APPLICATIONS

- **Powering Noise-Sensitive Circuitry**
  - **RF**
  - **Audio**
  - **VCOs**
- **DSP/FPGA/Microprocessor Supplies**
- **Post Regulator for Switching Supplies**

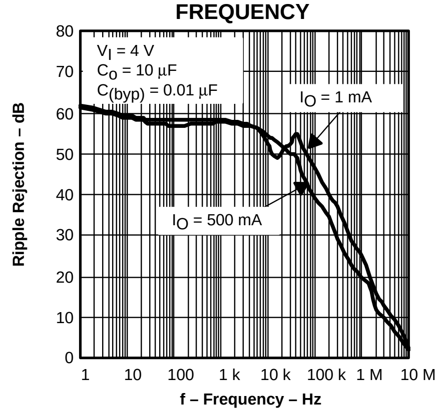
DESCRIPTION

The TPS795xx family of low-dropout (LDO) low-power linear voltage regulators features high power supply rejection ratio (PSRR), ultralow noise, fast start-up, and excellent line and load transient responses in a small outline, SOT223–5, package. Each device in the family is stable with a small 1-μF ceramic capacitor on the output. The family uses an advanced, proprietary BiCMOS fabrication process to yield extremely low dropout voltages (e.g., 110 mV at 500 mA). Each device achieves fast start-up times (approximately 50 μs with a 0.001-μF bypass capacitor) while consuming very low quiescent current (265 μA typical). Moreover, when the device is placed in standby mode, the supply current is reduced to less than 1 μA. The TPS79530 exhibits approximately 33 μV_{RMS} of output voltage noise with a 0.1-μF bypass capacitor. Applications with analog components that are noise sensitive, such as portable RF electronics, benefit from the high PSRR and low noise features, as well as the fast response time.

DCQ PACKAGE
SOT223-5
(TOP VIEW)



TPS79530
RIPPLE REJECTION
vs
FREQUENCY



TPS79530
OUTPUT SPECTRAL NOISE DENSITY
vs
FREQUENCY