Optimizing the Efficiency of a dc-dc Boost Converter Over 98% by Using Commercial SiC Transistors with Switching Frequencies from 100 kHz to 1MHz

Alberto Rodriguez, Marcos Fernandez, Aitor Vazquez, Diego. G. Lamar, Manuel Arias and Javier Sebastian
Universidad de Oviedo. Grupo de Sistemas Electrónicos de Alimentación (SEA)
Edificio Departamental nº 3. Campus Universitario de Viesques. 33204 Gijón. SPAIN
rodriguezalberto@uniovi.es

***Abstract*—In this paper an evaluation of Silicon Carbide (SiC) transistors currently available in the commercial market is presented. An experimental performance comparison between SiC JFET, Si MOSFET-SiC JFET cascode configuration and SiC MOSFET used as the main switch for a dc/dc boost converter (150 V/400 V) operating in Discontinuous Conduction Mode (DCM) is presented. The comparison of the different SiC devices is made in terms of the global boost-converter efficiency. Several experimental results dealing with the switching behavior of these SiC switches at different switching frequencies (from 100 kHz to 1 MHz) have been carried out in order to optimize the efficiency of the converter at different output power (300 W and 600 W). A good performance of all these switches is obtained from the point of view of the efficiency, highlighting the Si MOSFET-SiC JFET cascode behavior at 1MHz with an efficiency of 97.5% at 600 W. In addition, a possible application in the field of solar panels is proposed using the SiC JFET as the main switch. Continuous Conduction Mode (CCM) and DCM are tested at different switching frequencies with an output power of 1 kW and the results obtained are compared to the most widely reported in the bibliography.**

I. INTRODUCTION

Power electronic devices based on some wide bandgap semiconductor materials (e.g. Silicon Carbide (SiC) and Gallium Nitride (GaN)) have excellent theoretical characteristics to be the centre of the attention in the conversion of electrical energy in the coming years, substituting Silicon (Si) devices [1-3]. It is known that the electrical breakdown field of SiC is over eight times greater than Si and its thermal conductivity triples that of Si. Taking this into account, SiC power semiconductors are characterized by an outstanding performance concerning voltage blocking capability, on-state voltage drop, switching speed, and thermal resistance. Therefore, the future of SiC is now focused on developing new devices to design high-efficiency, high-frequency (subsequently low-size) and high-voltage converters at high power levels.

SiC Schottky barrier diodes have been available since 2001 [4-5], and some authors have presented several papers analyzing experimental results of SiC diodes, substituting directly Si diodes in their prototypes [6-8]. Nowadays, it is very common to include these SiC Schottky diodes to reduce the switching losses due to their theoretically negligible reverse recovery current. However, the availability of SiC transistors is slightly different. SiC transistors have only been commercially available in the last years. At the time of this writing, the companies that are commercially producing SiC switches include ROHM (Japan), Cree (USA) and SemiSouth (USA). ROHM and Cree produce SiC MOSFET, although ROHM devices are announced as "under development". SemiSouth (USA) produces SiC Vertical Trench JFET, where the best performance is obtained in normally-on devices. In both cases, Cree and SemiSouth devices, SiC switches cannot directly replace Si ones commonly used in power electronics. The best Semisouth devices are normally-on JFETs which require negative bias for blocking [9]. Therefore, new drivers and extra circuitry inherent to a normally-on device must be used (e.g. start-up, protections, etc…). In Cree MOSFETs, the recommended on-state gate-source voltage is 20 V in order to compensate their low transconductance values and off-state is between -2 V to -5 V to block the device properly [10] and, therefore, new drivers have to be implemented [10]. Some authors nowadays are developing new solutions [11-17] to overcome the aforementioned problem regarding the replacement of Si transistors with SiC ones.

This paper presents an experimental performance comparison between the SJDP120R085 SiC JFET by Semisouth and the CMF10120D SiC MOSFET by Cree used as the main switch for a dc/dc boost converter. Moreover, the SiC JFET has been tested in single configuration and in cascode configuration. The comparison of the SiC devices is carried out in terms of the efficiency obtained by the boost converter with the different SiC devices.

978-1-4673-4355-8/13/$31.00 ©2013 IEEE

The specifications of the boost converter are the following ones:

- 150 V input voltage.
- 400 V output voltage.
- Discontinuous Conduction Mode (DCM) close to the Boundary Conduction Mode.
- Switching frequencies between 100 kHz and 1 MHz.

The experimental tests were focused on increasing both the switching frequency (from 100 kHz to 1 MHz) and the output power (from 300 W to 600 W).

The input and output voltages of the boost converter described above are particularly suitable for photovoltaic (PV) applications. To fulfill the requirements of these applications, the output power has been increased up to 1 kW. CCM and DCM have been tested at different frequencies in order to find out which one is the best as a function of the switching frequency. These solutions have only been carried out using the normally-on JFET as the main switch because of its lower on-resistance compared to the SiC MOSFET and the cascode configuration and its good performance at the selected frequencies. The results obtained have been compared with the most widely extended solutions found in the bibliography.

The paper is organized as follows. Section II presents the switch configurations under test and the circuitry used to drive them. Experimental tests and the converter design will be described in Section III. Section IV will show, compare and discuss experimental results. Section V describes an example of application where SiC devices can improve the performance of the traditional Si-based solutions in a PV application. Finally, conclusions are presented in Section VI.

II. CONFIGURATION OF THE DEVICES UNDER TEST AND THEIR DRIVERS

Both SiC transistors under comparison in this paper are high-voltage (up to 1200 V) and high-current (up to 24 A) switches. The main characteristics of these two devices are shown in TABLE I. In both cases, these devices cannot replace directly Si MOSFETs commonly used in power electronics systems, because they require special driving signals.

In the case of the SiC JFET by Semisouth, a driver inherent to a normally-on device must be used. The manufacturer itself recommends a two stage, opto-coupled gate driver evaluation board [9]. This board (SGDR600P1) is optimized to drive normally-off SiC JFETs but with slight modifications it can also be used to drive the device under test (normally-on device). This driver has been tested in the developed boost converter with the SiC JFET under test with satisfactory results; however, the main disadvantage of this board is the limited switching frequency. In the datasheet of this board [18], special care with the temperature is recommended to be taken when the switching frequency is higher than 25 kHz and the maximum switching frequency of the driver is limited to 250 kHz. However, one of the main advantages of the SiC devices is their high-speed switching and, therefore, the performance of these devices is desired to be analyzed at higher switching frequencies. For this reason, a new driver has been developed following the same philosophy and structure of the recommended driver but taking special care with the cooling of the components. The schematic of the developed driver is presented in Figure 1. Figure 2 shows a picture of the connection of the driver to the gate of the JFET. The layout between the output of the driver and the gate of the JFET must be as short as possible to avoid the ringing in the gate signal.

In the case of the SiC MOSFETs developed by Cree, the manufacturer warns that these SiC switches should not be considered, in general, as a direct drop-in replacement in existing applications, because there are some differences in characteristics when they are compared to what is usually expected in high-voltage Si MOSFETs. Following the recommendations provided by the manufacturer and with a similar structure of the previously mentioned driver (Figure 1) a new driver has been designed and developed for the SiC MOSFET. This new board provides V_{GS} = +20 V for the on-state, required to optimize the performance due to the modest transconductance of these SiC MOSFETs, and V_{GS} = -5 V for the off-state, to avoid unintentional turn-on or partial turn-off (i.e., to block the device properly). The schematic of the developed driver is presented in Figure 3

In the case of the Si MOSFET-SiC JFET cascode configuration, a particular driver is not required because the gate of the low-voltage Si MOSFET (its main characteristics are also shown in TABLE I) is the controlled device. To switch quickly this MOSFET a common driver of Intersil (EL7156) has been used.

TABLE I MOST RELEVANT CHARACTERISTICS OF THE DEVICES UNDER TEST.

	Low Voltage Si MOSFET (IRF7455)		Normally-On SiC JFET (SJDP120R085)		High Voltage SiC MOSFET (CMF10120D)	
Manufacturer	International Rectifier		Semisouth		Cree	
V_{DS}_max (V)	30		1200		1200	
I_D_max (A)	15		27		24	
R_{DSon}_max (mΩ)	7.5		85		220	
V_{GS}_max/V_{GS}_threshold (V)	+12, -12 / 2		+15, -15 / -5		+25, -5 / 4	
C_{iss} (pF)	3480	V_{DS}=25 V	255	V_{DS}=100 V	928	V_{DS}=800 V
C_{oss} (pF)	870	f=1 MHz	80	f=100 kHz	63	f=1 MHz
C_{rss} (pF)	100		80		7.45	

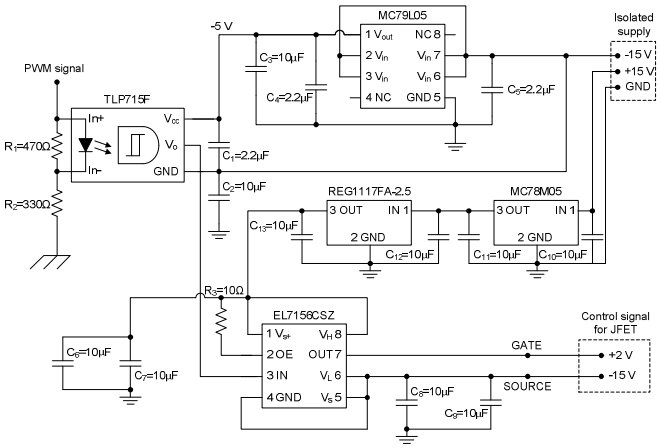


Figure 1 Detailed schematic of the developed driver for the normally-on SiC JFET.

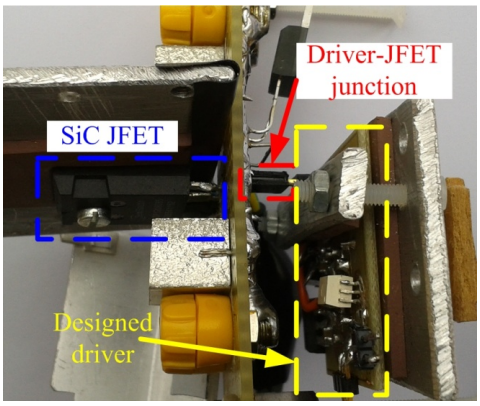


Figure 2 Detail of the junction between the driver and the gate of the JFET.

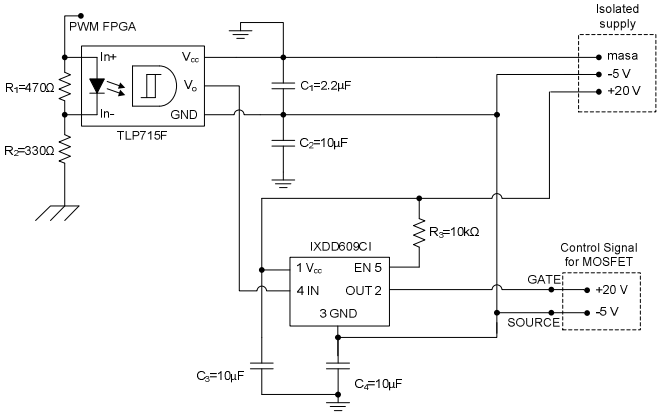


Figure 3 Detailed schematic of the developed driver for the SiC MOSFET.

III. Converter Design and Experimental Comparison

The main goal of this work is to compare the performance of two SiC switches in different configurations, frequencies and power levels. For its simplicity and to reduce the amount of components, a dc-dc boost converter (Figure 4) has been selected to carry out the comparison. The specifications of the boost converter are: 150 V input voltage, 400 V output voltage and switching frequencies of 100 kHz, 400 kHz and 1 MHz. The DCM has been chosen to minimize the switching losses, achieving Zero Voltage Switching (ZVS) in the turn-on of the main switch. Several experimental tests with different configurations for each of the SiC active switches have been developed for an output power of 300 W. The topologies with better efficiencies have been also tested at an output power of 600 W. All the presented efficiencies have been obtained without considering the driver losses. Input and output voltages and currents have been measured with digital multimeters (FLUKE 187).

To evaluate the performance of the devices under test properly, and to obtain a high global efficiency, the rest of the components in the converter should add the minimum possible losses. As the output diode of the boost converter, a SiC diode (in this case C3D10060A by Cree) has been used to reduce the switching losses due to its negligible reverse recovery current.

The inductors for 400 kHz and 1 MHz have been designed with only one layer of cooper wire to reduce the proximity losses, as it is shown in Figure 7. The inductor for 100 kHz has been designed using all the window area because the proximity losses at this frequency are not so significant. To obtain the desired operation point that minimizes the switching losses (i.e., reaching ZVS in the turn-on of the switch, as can be seen in Figure 8) in each experimental test, the inductance value is slightly modified changing the gap of the inductor. In Figure 5, a picture of the three inductors is shown and the bobbins and the magnetic material are also specified.

The active switch of the boost converter is the device under test and the two SiC transistors previously described have been tested for an output power of 300 W in the following different configurations (represented in Figure 6): a single configuration of the SiC JFET has been tested with a SiC and with a Si freewheeling diode (Figure 6a); the SiC MOSFET has been tested without additional freewheeling diode (Figure 6b) and also with a SiC and with a Si freewheeling diode (Figure 6c); the Si MOSFET-SiC JFET cascode configuration has been tested without (Figure 6d) and with Si and SiC freewheeling diode (Figure 6e), and also adding +2 V at the gate of the JFET instead of connecting it to the ground (Figure 6f). For an output power of 600 W, the same configurations with the exception of the JFET with Si freewheeling diode have been analyzed. For all these described configurations the output diode is always the same (the previously mentioned SiC diode C3D10060A).

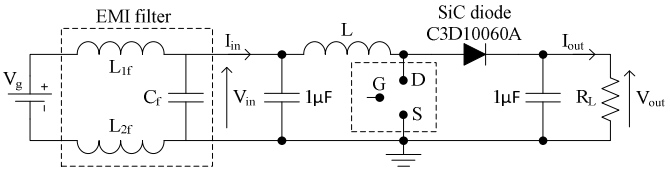


Figure 4 Schematic of the proposed boost converter to compare the SiC devices.

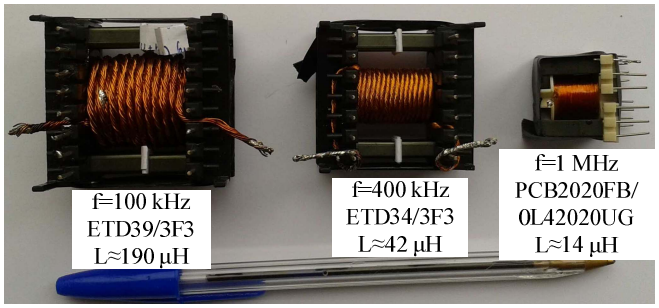


Figure 5 Picture of the developed inductors.

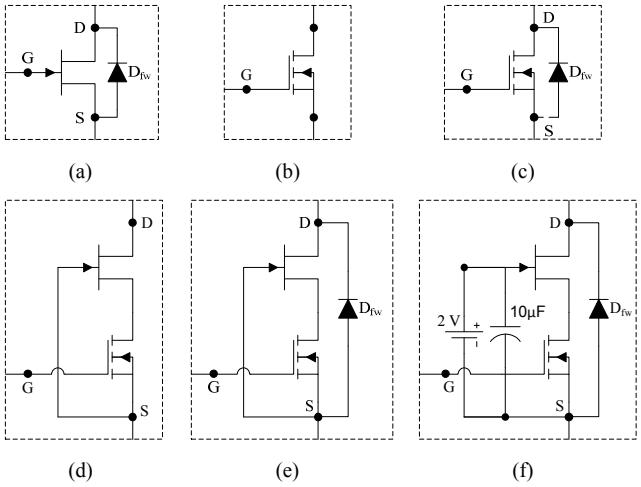


Figure 6 Different tested topologies. (a) SiC JFET with Si and SiC freewheeling diode, (b) SiC MOSFET, (c) SiC MOSFET with Si and SiC freewheeling diode, cascode (d) without freewheeling diode, (e) with Si and SiC freewheeling diode, and (f) with +2 V at the gate of the JFET and SiC freewheeling diode.

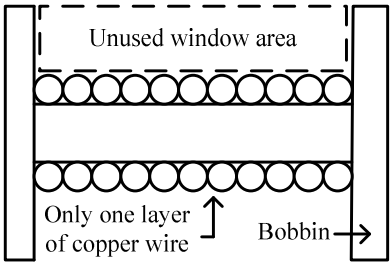


Figure 7 Distribution of the cooper wire to reduce the proximity losses in the inductors used at 400 kHz and 1 MHz switching frequencies.

IV. Experimental Results, Performance and Discussion

The efficiency of the converter is optimized operating in DCM, by turning-on the active switch when its drain-source voltage is zero. In this situation, not only Zero Current Switching (ZCS) in the turn-off of the output diode but also ZVS in the turn-on of the active switch are achieved. Figure 8 shows the main operation waveforms in the case of maximum efficiency obtained for an output power of 600 W at 1 MHz with the three aforementioned configurations (waveforms of other situations are very similar). This figure shows how V_{DS} starts decreasing when the inductor current becomes negative and V_{GS} is activated when V_{DS} reaches 0 V. The negative inductor current is required to discharge the output capacitance of the active switch and allows ZVS turn-on transition to be achieved. Figure 9 presents the efficiencies for all the previously described experimental tests.

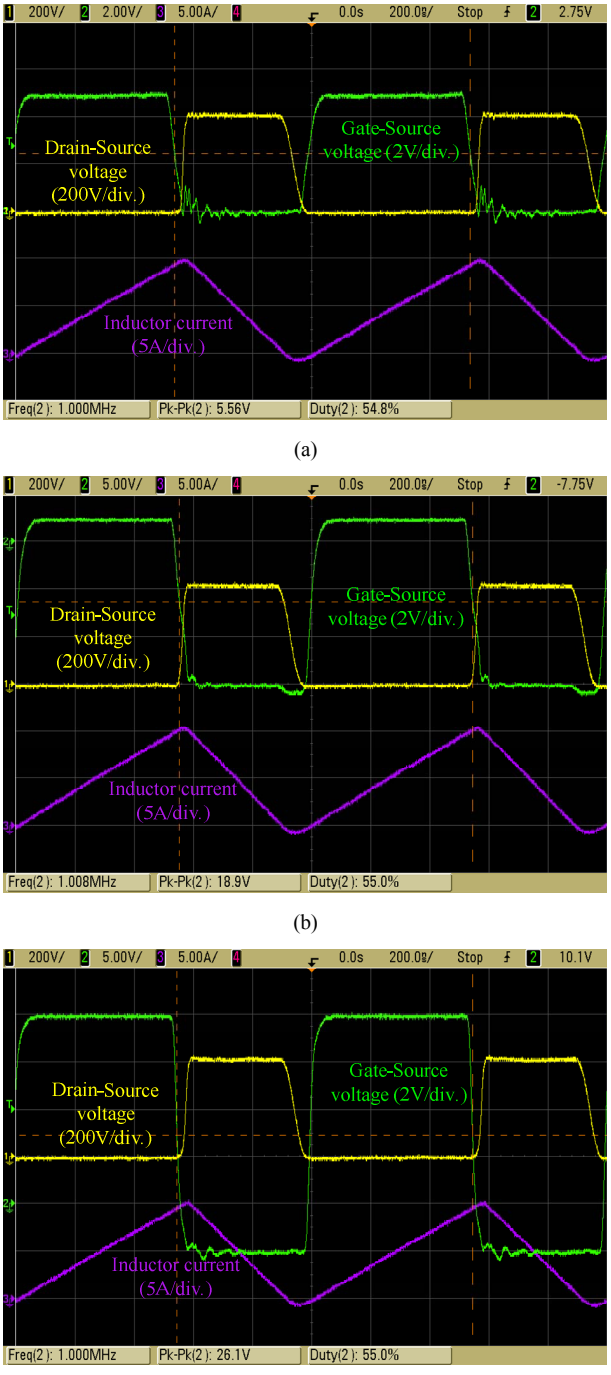
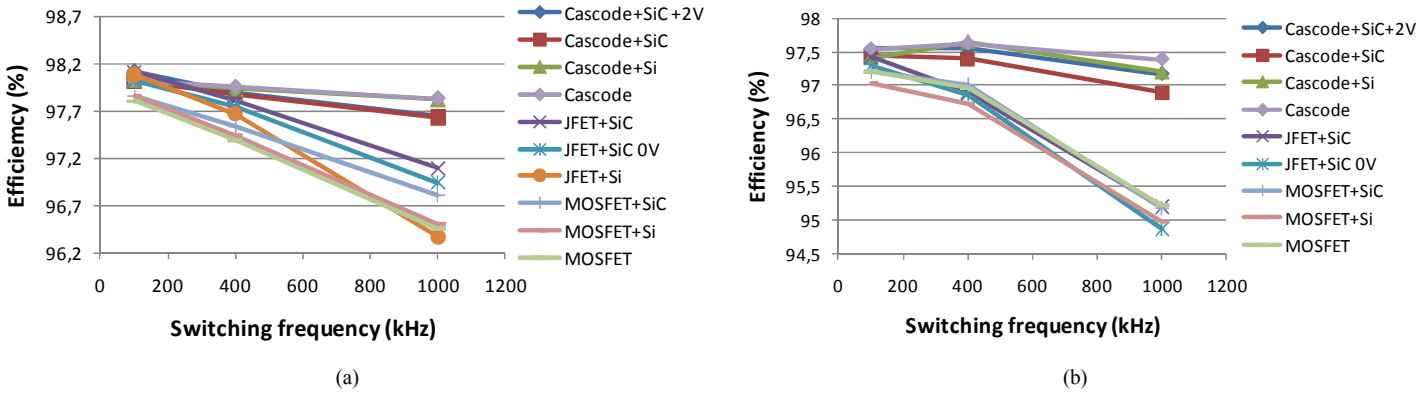


Figure 8 Main operation waveforms of three different configurations at 600 W output power and 1 MHz: a) Cascode with SiC freewheeling diode and 0 V at the gate of the JFET, (b) SiC JFET with SiC freewheeling diode and (c) SiC MOSFET.



(a) (b)

Figure 9 Efficiency values of the different configurations for an output power of (a) 300W and (b) 600 W.

Some conclusions can be highlighted thanks to these results. The results with an output power of 300 W show that:

- At 100 kHz the efficiency for all the configurations is roughly the same because the switching losses at this frequency are almost insignificant; the SiC MOSFET provides the lowest efficiency mainly due to its higher on-resistance.
- In the cascode configuration, the negative current that discharges the output capacitance of the switch can flow through the parasitic diode of the Si MOSFET and then through the channel of the JFET (normally-on). Consequently, the current through the freewheeling diode of the cascade can be neglected. As a consequence, in the efficiency curves there is no difference between using and not using a Si freewheeling diode. On the other hand, the capacitance added by the SiC diode (higher than a Si diode) reduces slightly the efficiency, what is clearly shown at 1MHz.
- The use of a SiC freewheeling diode with the JFET provides better efficiency than a Si one, (the difference is bigger for higher frequencies). The main reason is the best switching behavior of the SiC semiconductors. In this case the reactive current flows through the freewheeling diode once the output capacitance of the JFET has been discharged.
- The cascode configuration provides the best efficiency for frequencies of 400 kHz and 1 MHz. This configuration provides a better switching process that reduces the switching losses achieving efficiencies of almost 98% at 1 MHz for an output power of 300 W.
- Due to the higher parasitic capacitances of the SiC MOSFET and the higher on-resistance, the efficiencies obtained when using this device are lower.

From the results obtained when the output power is 600 W, almost the same conclusions can be extracted. Efficiencies obtained with SiC MOSFET are the lowest, but are almost the same as the ones obtained with the SiC JFET at 1 MHz. The best performance is obtained again with the cascode configuration, achieving efficiencies of 97.5% for 400 kHz and 1 MHz. This high efficiency is likely due to the lower switching losses of the cascode configuration because the JFET is operating in common-gate configuration and, therefore, no Miller effect takes place in this device.

V. PV SPECIFICATIONS EXAMPLE

Although the purpose of the paper is providing a thorough comparative of different SiC and Si devices, it is possible to depict a possible application for the boost converter used in this analysis. Taking into account the value of the input and output voltages and the maximum rated power used in the analysis, the presented boost converter can be a perfect candidate for PV applications.

Due to the low output voltage of a single PV panel, they are usually connected in a series configuration for increasing the overall output voltage (the exception to this approach can be found in PV modules [19]). This series-connected PV panels may be used in two different ways:

- Connecting several strings of PV panels in parallel by means of blocking diodes (Figure 10a). This arrangement is then connected to a dc-ac converter.
- Connecting each string to its own converter. This approach, with several advantages in comparison to the previous one, can be achieved with two different configurations of the converter.

  1. Each string is connected to its own dc-dc converter. These converters are then connected in parallel and the common output is connected to a dc-ac converter (Figure 10b).
  2. Each string is connected to its own dc-ac converter (Figure 10c). In this case, it may be a two-stage topology in which the first stage is a dc-dc converter in charge of calculating the MPPT and boosting the voltage provided by the PV string. The second stage is an inverter synchronized with the grid.

In the last two configurations, the most common topology is the boost converter. In this way, the number of PV panels can be reduced (improving the MPPT) as the voltage provided by them can be increased to a suitable value for the inverter.

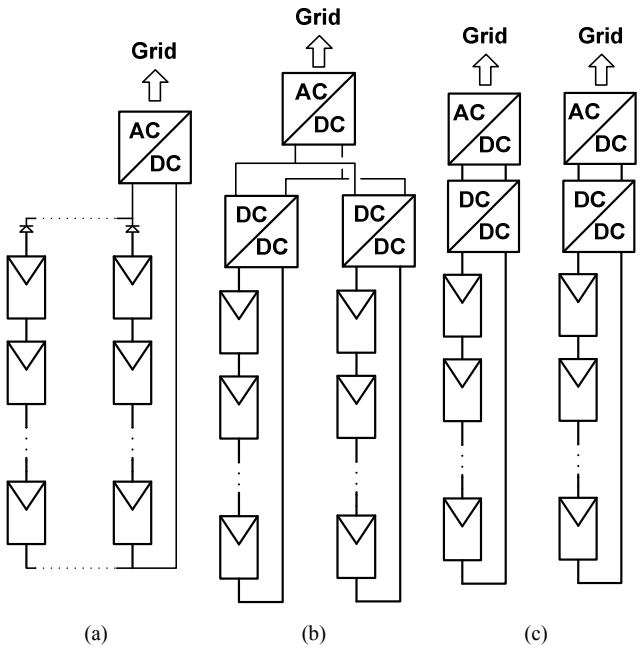


Figure 10 (a) Centralized topology. (b) Multi-string topology. (c) Single-string topology.

Typical output voltages of this boost converter may vary from 400 to 500 V. Typical input voltages may vary from 100 V to 400 V, or even higher (up to 600 V). In this last case, the boost converter operates with a duty cycle equal to zero, its output voltage is equal to the input one and defined by the PV panels (not by the boost converter). In this situation, the inverter has to operate taking this into account. The rated power for each converter is in the range of some kW.

As can be seen, the analyzed boost, used to compare the SiC devices, can be perfectly used as first stage in any PV application with a configuration similar to the ones presented in [20], [21] or [22].

In these topologies, efficiency may be as high as 99.5%. Nevertheless, this efficiency is achieved when the PV panels are providing a very high voltage and the boost converter is operating with close-to-zero duty cycles (i.e., the input voltage is only slightly lower than the output one). The efficiency when the input-output voltage ratio is close to the ratio of the proposed boost converter (150 V - 400 V) is around 98%. Besides, the switching frequency is always lower than 100 kHz and it may be as low as 20 kHz. Hence, the size of the converter increases. Nevertheless, this switching frequency is mandatory in order to reduce switching losses and to boost efficiency.

To minimize the size of the converters described above, a boost converter with higher switching frequencies has been developed, taking advantage of the fast switching transitions of the SiC devices. The output power of this converter has been extended to 1 kW and different input voltages (150, 300 and 320 V) for a fixed output voltage of 400 V have been tested so as to compare its efficiency with the typical efficiencies in other converters for this application. Two different conduction modes (CCM and DCM) have been tested in order to determine the most suitable one in terms of the efficiency as a function of the frequency.

Figure 11 represents the boost-converter efficiency operating in CCM and DCM as a function of the switching frequency for an output power of 1 kW and with different voltage conversions, using the normally-on JFET described in the previous sections as the main switch. The reason to use this device is mainly because of its good results in terms of the efficiency for the selected switching frequencies, and its lower on resistance compared with the other configurations described in this paper (cascode and SiC MOSFET), which makes it more suitable for higher output power. As can be seen in the CCM representations, the efficiency for a switching frequency of 100 kHz is always above 98%, even when the voltage conversion is from 150 to 400 V, and reaches up to 99.25% for lower conversion rates. As it could be expected, this efficiency decreases considerably with the switching frequency because of the fact that the converter operates in CCM and, at 200 kHz, its value stays slightly above 97% for an input voltage of 150 V and goes up to nearly 99% for input voltages of 300 V and 320 V. Finally, at 400 kHz, the efficiency falls below 96% for high voltage-conversion ratio and remains at 98% when the input voltage is 300 V or 320 V.

Figure 11 also shows that the efficiency decreases dramatically with the frequency when the converter operates in CCM. If the goal of the system is to reduce even more the size and, therefore, increase the switching frequency, another approach has to be taken into account. In this case, the DCM would be more appropriate as it reduces the switching losses achieving ZVS at the turn-on of the main switch.

In the case of DCM, only the test with an input voltage of 150 V has been carried out. The reason is that if the reverse recovery current of the output diode is disregarded (as a result of using a SiC Schottky diode), the drain-source voltage of the main switch falls down to a minimum value, due to the resonance between the inductance and the output capacitor of the main switch, which is equal to $2V_g - V_{out}$, as can be seen in Figure 12. This implies that ZVS at turn-on can only be achieved when the expression shown before is equal or lower than zero. As a result, when the output voltage is 400 V, no ZVS at turn-on of the main switch can be achieved for input voltages higher than 200 V, causing that DCM loses a bit its sense because switching losses would still increase considerably with frequency and the high current ripple in the inductor would have a great impact on this component and on the conduction losses of the switches (as the rms current goes up). With respect to this, an important consideration has to be taken into account when designing inductances for DCM at relatively high frequencies. In this case, the ac component of the magnetic field is clearly higher than the one when operating in CCM. The effects of the fringing flux around the core air-gap can increase considerably the copper losses [23]. To solve this problem, special care has to be taken in the design of the inductor, trying to separate as much as possible the windings from the gap. In addition to this, other aspects, like the proximity effect mentioned in Section III, have to be taken into account when designing inductors at high frequencies.

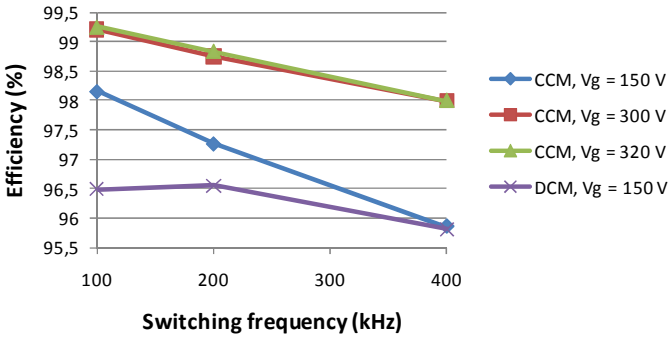


Figure 11 Efficiency values of the boost converter using the SiC JFET for an output power of 1 kW and different conduction modes.

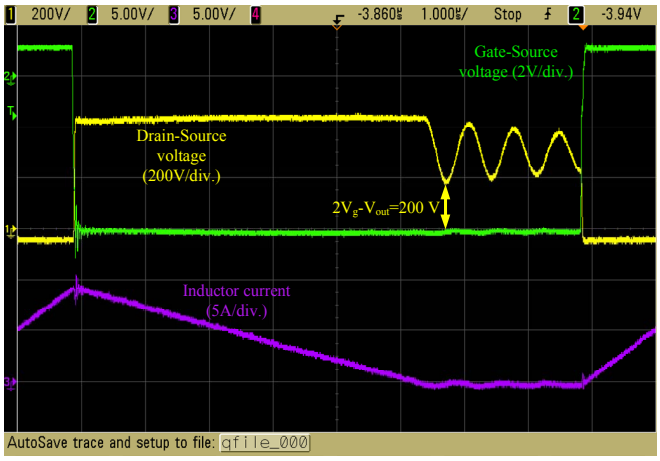


Figure 12 Detail of the drain-source resonance voltage in DCM when input voltage is higher than half of the output voltage. Vg=300 and Vout=400.

The efficiency of the boost converter operating in DCM as a function of the frequency is also shown in Figure 11. This figure shows clearly how the efficiency stays flat in the step between 100 and 200 kHz and reduces slightly when the switching frequency rises up to 400 kHz. This efficiency is lower than the obtained in CCM for low frequencies due to the fact that at these frequencies the switching losses are almost negligible and the higher current ripple of the inductor in DCM increases the conduction losses in the switches (as a result of the higher rms current) and the losses in the inductor itself. In fact, the temperature measurements point out an increase of 30 ºC in the temperature of the inductor in DCM with respect to CCM.

Figure 11 also shows that the decreasing slope of the efficiency as a function of the switching frequency is much more noticeable in the case of CCM than in DCM for the same voltage-conversion ratio, and the value of the efficiency equals at 400 kHz in both conduction modes. Therefore, DCM seems to be the better solution at frequencies higher than 400 kHz if only the efficiency is concerned. This solution would reduce the size of the system at the expense of penalizing the efficiency with respect to the case of operating in CCM at 100 kHz.

However, although the efficiency at 400 kHz is the same in CCM and DCM, it is important to remark that the losses are distributed in a different way among the components of the converter. In the case of DCM, the overall losses are distributed between the JFET, the output diode and the inductor, and none of these components achieves an excessively high temperature. On the contrary, in CCM the inductance has much lower losses than in the case of DCM because of the lowest current ripple and, therefore, the great majority of the losses are in the JFET and the output diode. As a consequence, special care must be taken in the cooling of these two components when operating in CCM at 400 kHz.

VI. CONCLUSIONS

The performance of two different SiC transistors for high-voltage applications has been tested and compared in the presented paper. The efficiency obtained with the SiC JFET is slightly better than the obtained using the SiC MOSFET, without considering the driver losses. The use of both devices requires new drivers and special care in the generation of the gate signal. The good performance expected from both SiC switches at high frequency has been demonstrated thanks to the developed experimentation.

The Si MOSFET-SiC JFET cascode configuration provides a surprising excellent efficiency, even better than the obtained with the single configuration of the SiC JFET. Moreover, this configuration allows the use of commercial common drivers because the controlled transistor is a low-voltage MOSFET. With this configuration an efficiency of almost 98% has been obtained for 400 kHz and it is maintained for 1 MHz, which shows that the switching losses are very low. The switching process with the cascode configuration seems to be particularly optimized.

In addition to the comparison between the different SiC devices currently available in the market, a PV application of 1 kW for the boost converter using the SiC JFET as the main switch has been proposed. The developed converter shows very good efficiency at 100 kHz operating in CCM with high voltage-conversion ratios, and almost 99.5% efficiency when the voltage conversion goes from 320 V to 400 V. Furthermore, this study point out that, at 400 kHz, the efficiency obtained with the CCM equals the DCM one. Consequently, the latter conduction mode seems to be the most suitable one for higher frequencies, leading to a considerable reduction in the size of the system at the expense of decreasing the efficiency.

ACKNOWLEDGMENT

This work has been supported by the Spanish Government under projects CONSOLIDER MICINN-10-CSD2009-00046 and MICINN-10-DPI2010-21110-C02-01 and FPU grant AP2008-03380.

REFERENCES

[1] J. A. Cooper, y A. Agarwal, "SiC power-switching devices. The second electronics revolution?", Proceedings of the IEEE, volumen 90, nº 6, junio de 2002, pp. 956-968.

[2] A. Elasser y P. Chow, "Silicon carbide benefits and advantages for power electronics circuits and systems", Proceedings of the IEEE, volumen 90, nº 6, junio de 2002, pp. 969-986.

[3] José Millán "Wide band-gap power semiconductor devices" IET Circuits Devices and Systems, 2007, volumen 1, nº 5, pp. 372-379.

[4] Badila, M.; Brezeanu, G.; Banu, V.; Godignon, P.; Millan, J.; Jorda, X.; Draghici, F.; , "SiC power Schottky diodes: industrial development," Semiconductor Conference, 2001. CAS 2001 Proceedings. International , vol.2, no., pp.337-340 vol.2, Oct 2001.

[5] http://www.infineon.com

[6] Elasser, A.; Kheraluwala, M.H.; Ghezzo, M.; Steigerwald, R.L.; Evers, N.A.; Kretchmer, J.; Chow, T.P.; , "A comparative evaluation of new silicon carbide diodes and state-of-the-art silicon diodes for power electronic applications," Industry Applications, IEEE Transactions on , vol.39, no.4, pp. 915- 921, July-Aug. 2003.

[7] Spiazzi, G.; Buso, S.; Citron, M.; Corradin, M.; Pierobon, R.; , "Performance evaluation of a Schottky SiC power diode in a boost PFC application," Power Electronics, IEEE Transactions on , vol.18, no.6, pp. 1249- 1253, Nov. 2003.

[8] Hernando, M.M.; Fernandez, A.; Garcia, J.; Lamar, D.G.; Rascon, M.; , "Comparing Si and SiC diode performance in commercial AC-to-DC rectifiers with power-factor correction," Industrial Electronics, IEEE Transactions on , vol.53, no.2, pp. 705- 707, April 2006

[9] Application Note AN-SS1"SiC Enhancement-Mode Junction Field Effect Transistor & Recommendation For Use", SemiSouth.

[10] http://www.cree.com/power/products/z-fet-sic-mosfet

[11] Friedli, T.; Round, S.D.; Hassler, D.; Kolar, J.W.; , "Design and Performance of a 200-kHz All-SiC JFET Current DC-Link Back-to-Back Converter," Industry Applications, IEEE Transactions on , vol.45, no.5, pp.1868-1878, Sept.-oct. 2009.

[12] Qingchun Zhang; Callanan, R.; Das, M.K.; Sei-Hyung Ryu; Agarwal, A.K.; Palmour, J.W.; , "SiC Power Devices for Microgrids," Power Electronics, IEEE Transactions on , vol.25, no.12, pp.2889-2896, Dec. 2010

[13] Rixin Lai; Fei Wang; Burgos, R.; Boroyevich, D.; Di Zhang; Puqi Ning; , "A Shoot-Through Protection Scheme for Converters Built With SiC JFETs," Industry Applications, IEEE Transactions on , vol.46, no.6, pp.2495-2500, Nov.-Dec. 2010.

[14] Kadavelugu, A.; Baek, S.; Dutta, S.; Bhattacharya, S.; Das, M.; Agarwal, A.; Scofield, J.; , "High-frequency design considerations of dual active bridge 1200 V SiC MOSFET DC-DC converter," Applied Power Electronics Conference and Exposition (APEC), 2011 Twenty-Sixth Annual IEEE , vol., no., pp.314-320, 6-11 March 2011

[15] Wrzecionko, B.; Bortis, D.; Biela, J.; Kolar, J.W.; , "Novel AC-Coupled Gate Driver for Ultrafast Switching of Normally Off SiC JFETs," Power Electronics, IEEE Transactions on , vol.27, no.7, pp.3452-3463, July 2012.

[16] Bernal, C.; Gaudo, P.M.; Gallego, A.; Otin, A.; Burdio, J.M.; , "Half-bridge resonant inverter for domestic induction heating based on silicon carbide technology," Applied Power Electronics Conference and Exposition (APEC), 2012 Twenty-Seventh Annual IEEE , vol., no., pp.2218-2222, 5-9 Feb. 2012.

[17] Gaudo, P.M.; Bernal, C.; Avellaned, J.; Burdio, J.M.; , "Intermodulation distortion in 1SW-ZVS multi-inverter for induction heating home appliances," Applied Power Electronics Conference and Exposition (APEC), 2012 Twenty-Seventh Annual IEEE , vol., no., pp.2223-2228, 5-9 Feb. 2012.

[18] Application Note AN-SS3, "SDGR600P1 – 6A Gate Driver Reference Design & Demoboard", SemiSouth.

[19] Rodriguez, C.; Amaratunga, G.A.J.; , "Long-Lifetime Power Inverter for Photovoltaic AC Modules," *Industrial Electronics, IEEE Transactions on* , vol.55, no.7, pp.2593-2601, July 2008.

[20] Ho, C.N.; Breuninger, H.; Pettersson, S.; Escobar, G.; Serpa, L.A.; Coccia, A.; , "Practical Design and Implementation Procedure of an Interleaved Boost Converter Using SiC Diodes for PV Applications," *Power Electronics, IEEE Transactions on* , vol.27, no.6, pp.2835-2845, June 2012.

[21] Ho, C.N.M.; Breuninger, H.; Pettersson, S.; Escobar, G.; Serpa, L.; Coccia, A.; , "Practical implementation of an interleaved boost converter using SiC diodes for PV applications," *Power Electronics and ECCE Asia (ICPE & ECCE), 2011 IEEE 8th International Conference on* , vol., no., pp.372-379, May 30 2011-June 3 2011.

[22] Ho, C.N.M.; Breuninger, H.; Pettersson, S.; Escobar, G.; Canales, F.; , "A comparative performance study of an interleaved boost converter using commercialized Si and SiC diodes for PV applications," *Power Electronics and ECCE Asia (ICPE & ECCE), 2011 IEEE 8th International Conference on* , vol., no., pp.1190-1197, May 30 2011-June 3 2011.

[23] W. Lundquist, "Switching Power Magnetics Design", Seminar T1-4, ECCE 2012, September 2012, Raleigh (NC), EEUU