Switching Performance Comparison of the SiC JFET and SiC JFET/Si MOSFET Cascode Configuration

Alberto Rodriguez, *Member, IEEE*, Marcos Fernandez, *Student Member, IEEE*, Diego G. Lamar, *Member, IEEE*, Manuel Arias, *Member, IEEE,* Marta M. Hernando, *Senior Member, IEEE*, and Javier Sebastian, *Senior Member, IEEE*

Abstract -- — **Silicon Carbide (SiC) devices are becoming increasingly available on the market due to the mature stage of development fact of their manufacturing process. Their numerous advantages compared to silicon (Si) devices, such as, for example, higher blocking capability, lower conduction voltage drop and faster transitions make them more suitable for high-power and high-frequency converters.**

The aim of this paper is to study the switching behavior of the two most-widely studied configurations of SiC devices in the literature: the normally-on SiC JFET and the cascode using a normally-on SiC JFET and a low-voltage Si MOSFET. A detailed comparison of the turn-on and turn-off losses of both configurations is provided and the results are verified against experimental efficiency results obtained in a boost converter operating in both Continuous Conduction Mode (CCM) and Discontinuous Conduction Mode (DCM). Furthermore, special attention will be paid to the switching behavior of the cascode configuration, analyzing the effect of its low-voltage Si MOSFET and comparing different devices. The study carried out will confirm that the overall switching losses of the JFET are lower, making it more suitable for operating in CCM in terms of the overall converter efficiency. However, the lower turn-off losses of the cascode show this device to be more suitable for DCM when ZVS is achieved at the turn-on of the main switch. Finally, all the theoretical results have been verified in an experimental 600W boost converter.

Index Terms— **Cascode configuration, High frequency converters, High efficiency converters, SiC JFET, Switching performance.**

I. INTRODUCTION

Silicon Carbide (SiC) devices have taken on greater relevance in the last few years due to the advanced stage of their technological development and their subsequent appearance on the market. The advantages of these devices with respect to their Silicon (Si) counterparts may be summarized in terms of their higher electrical breakdown field (eight times higher) and thermal conductivity (three times higher) [1-3]. These benefits derive in higher voltage block capability, faster switching transitions, a lower on-state voltage drop and lower thermal resistance, all of which make SiC devices suitable for high-power and high-frequency converters.

Although SiC diodes have been commercially available for a long time and are hence commonly used in Switching Mode Power Supplies (SMPS), the introduction of SiC transistors on the market is much more recent, not being so widespread in power electronics applications. There are currently a number of different SiC transistor configurations, such as MOSFETs, JFETs (normally-on and normally-off) and cascodes, although the most widespread configurations in the literature are the normally-on JFET and the cascode on account of their good performance. The main disadvantage of the former (i.e. JFET) is the need to implement new drivers [4-6] which supply negative voltages in order to turn off the device properly. Moreover, due to the normally-on feature of these devices, some solutions have to be included when replacing Si transistors (e.g. start-up circuitry, protections, etc.) [7-9]. With the cascode configuration, however, it is possible to turn a normally-on device like the JFET into a normally-off one by means of adding a low-voltage Si MOSFET. The price to pay is an increase in the on-resistance.

The cascode configuration is well known and has been used and studied in depth [10-14] for some time now, although its use has not been so widespread. However, the appearance of the new SiC devices has led to renewed use of this configuration due to the fact that it enables the speed of SiC devices to be exploited while maintaining a typical commercial driver to control the switch. In this respect, the study of the switching process in the SiC JFET/ Si MOSFET cascode configuration is an interesting topic in the world of SMPS aimed at making the most of this configuration. Several related papers have presented simulations and analyses of practical results in both transitions (i.e. turn-on and turn-off) in the switching process of the cascode [11] and [15]. However, a comparative study of both transitions between the SiC JFET and the SiC JFET/Si MOSFET cascode could introduce a new perspective as to which solution is more appropriate depending on the conditions under which the converter operates.

Aberto Rodriguez, Marcos Fernandez, Diego. G. Lamar, Manuel Arias, Marta M. Hernando and Javier Sebastian are with the Grupo de Sistemas Electrónicos de Alimentación (SEA), Universidad de Oviedo, 33204 Gijón, Spain (e-mail: rodriguezalberto@uniovi.es fernandezmarcos@uniovi.es, gonzalezdiego@uniovi.es; ariasmanuel@uniovi.es; mmhernando@uniovi.es; sebas@uniovi.es).

The aim of this paper is to present a comparison in terms of the switching performance of the normally-on JFET and the cascode configuration, made up of a normally-on JFET and a low-voltage Si MOSFET. First, a theoretical analysis of the cascode configuration in both switching transitions is presented, putting forward a model which defines all the voltage and current waveforms of the cascode from a circuitry analysis in the time domain. This model is complemented by a detailed explanation of the switching process, showing both the key conclusions to be drawn regarding it and the difference with the switching process of a normally-on JFET. The theoretical results and conclusions are subsequently verified experimentally in three ways: via the obtained time domain waveforms, by means of the switching losses determined from the experimental waveforms, and in terms of the efficiency of the converter. Furthermore, in the case of the cascode, two different options are assessed changing the low-voltage MOSFET as reported in [11]. In this case, a corroboration of the main benefits and drawbacks of the choice of the low-voltage MOSFET in the overall switching behavior are presented in this paper in terms of the proposed model, the experimental waveforms and efficiency measurements.

The boost converter was selected to carry out the experimental comparison between the two chosen configurations. The reason for choosing this converter is mainly its simplicity and the minimum number of elements that it comprises, reducing the influence of other elements in the converter on the switching process under study. A SiC diode was used as the output rectifier of the boost converter in order to reduce the reverse recovery current of this element and achieve fast switching transitions. To verify the conclusions drawn from the theoretical analysis, several tests were carried out with the converter operating in Continuous Conduction Mode (CCM) and Discontinuous Conduction Mode (DCM) at 600 W output power.

The paper is organized as follows in line with the aforementioned research plan. Section II presents the theoretical analysis of the cascode configuration in both switching transitions, highlighting the main differences with respect to traditional normally-on JFET transitions. Section III describes the performance of the two configurations under test in a boost converter operating in CCM. The section is divided into four subsections related to the converter specifications and its components, the time domain waveforms, the switching energies of the different configurations and the efficiency results. Section IV provides the same analysis as Section III, but with the converter operating in DCM in order to highlight the advantages of the cascode configuration compared to the normally-on JFET. Finally, Section V. presents the conclusions of the paper.

II. SWITCHING ANALYSIS OF THE SiC JFET/Si MOSFET CASCODE CONFIGURATION

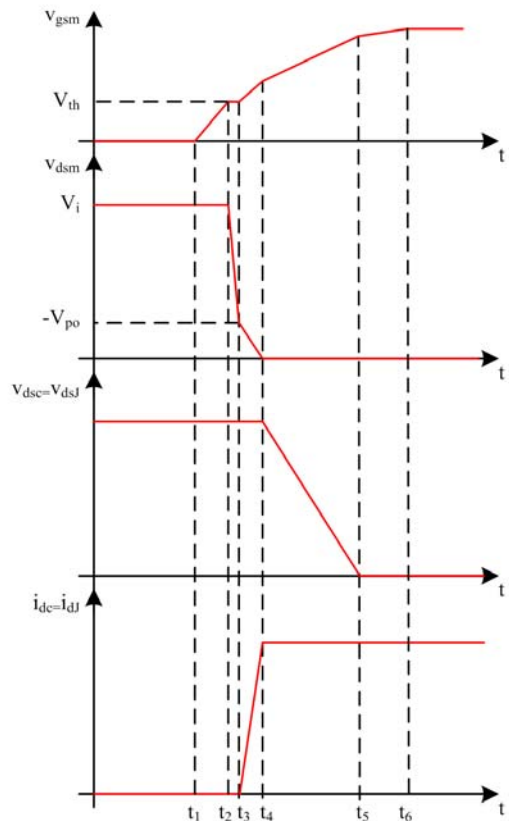The main aim of this section is to analyze the turn-on and

Fig. 1: Main waveforms of the turn-on transition of the cascode configuration.

turn-off switching transitions of the SiC JFET/Si MOSFET cascode configuration. The second objective is to highlight the differences with respect to normally-on JFET switching transitions. For this purpose, a theoretical model based on equivalent circuits for the turn-on and turn-off transitions will be presented. Moreover, the conclusions of this theoretical analysis will show the benefits and drawbacks of the choice of the low-voltage MOSFET in terms of its main features.

A. Switching behavior at turn-on

Figure 1 shows the turn-on waveforms of the cascode configuration over an inductive load circuit. All the transitions of these waveforms in each interval will be properly explained over the equivalent circuit shown in Fig 2. As some of these transitions are well known, the explanation will be descriptive. However, there are key transitions during the turn-on of the cascode configuration which define different behaviors compared to the normally-on JFET which will be explained in detail.

1) Interval [t_1, t_2]

Prior to t_1, the output voltage of the driver is zero, the low-voltage MOSFET is off and its drain-to-source voltage (v_{dsm}) is defined by the leakage drain current that the JFET allows (V_i). Moreover, this voltage is applied between the gate and the source of the JFET (v_{gsJ}=-v_{dsm}), and thus the JFET is also
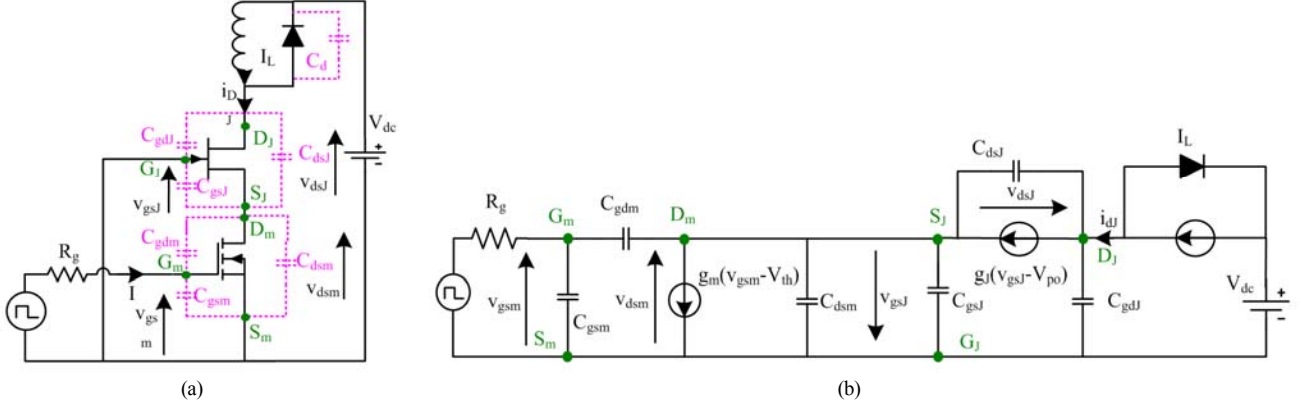
Fig. 2. a) Inductive switching circuit; b) Proposed equivalent circuit to analyze the turn-on transition of a cascode configuration.
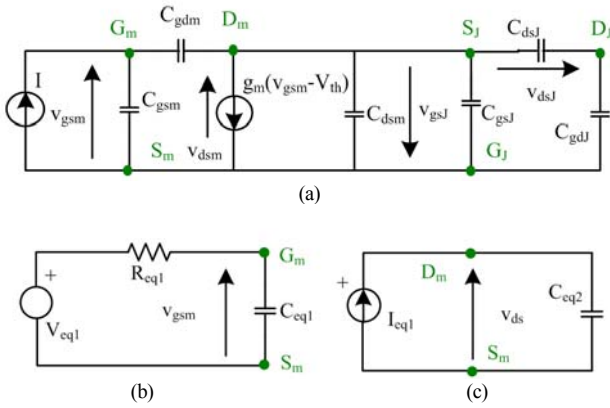

Fig 3. a) Equivalent circuit during the interval [t_2, t_3]. b) Equivalent circuit to calculate v_{gsm} during the interval [t_2, t_3]. c) Equivalent circuit to calculate v_{dsm} during the interval [t_2, t_3].

off due to the fact that v_{gsJ} is lower than the pinch-off voltage of the normally-on JFET (V_{po}). At t_1, the output voltage of the driver rises to its high level value. At this point, the gate-to-source voltage of the MOSFET (v_{gsm}) is known to increase as shown Fig. 1. In the real world, the evolution of v_{gsm} will be an exponential waveform due to the gate resistance of the MOSFET. This transition is completed at t_2 when the threshold voltage of the MOSFET (V_{th}) is reached.

2)   Interval [t_2, t_3]

From t_2, the current through the drain of the MOSFET (i_{dm}) increases due to the fact that v_{gsm} is greater than its threshold voltage (i.e. $i_{dm}=g_m(v_{gsm}-V_{th})$, where g_m is the trasconductance of the MOSFET). However, the JFET is still off and no current flows from the inductor through the cascode configuration ($i_{dJ}=0$, where i_{dJ} is the drain current of the JFET). The drain current of the MOSFET discharges its drain-to-source capacitance (C_{dsm}), so v_{dsm} decreases and therefore v_{gsJ} increases until V_{po}. During this interval, a "small" Miller effect occurs due to the gate-to-drain capacitance of the MOSFET (C_{gdm}) and is highlighted in v_{gsm} (Fig. 1). Bearing in mind the above considerations, the proposed equivalent circuit to study this interval is shown in Fig. 3a. As can be seen, the driver source has been modeled as a current source due to the fact that a Miller effect occurs

and constant current (I) is injected through the gate of the MOSFET. As i_{dJ} is zero, the current source which models the current channel of JFET is eliminated (i.e. $g_J(v_{gsJ}-V_{po})$ current source of Fig. 2b is eliminated).

In order to analyze the evolution of the v_{gsm} voltage, the equivalent circuit in Fig. 3b can be obtained from the circuit in Fig. 3a. As can be seen, a RC circuit performs of the fuction of v_{gsm}, where:

$$V_{eq1} = I \cdot \left(\frac{C_{dsm} + C_{gdm}}{C_{gdm}} \right) \cdot \frac{1}{g_m} + V_{th}, \tag{1}$$

$$C_{eq1} = \left(\frac{\left(\left(\frac{C_{dsJ} \cdot C_{gdJ}}{C_{dsJ} + C_{gdJ}} \right) + C_{gsJ} + C_{dsm} \right) \cdot C_{gdm}}{C_{gdm} + \left(\left(\frac{C_{dsJ} \cdot C_{gdJ}}{C_{dsJ} + C_{gdJ}} \right) + C_{gsJ} + C_{dsm} \right)} \right) + C_{gsm}, \tag{2}$$

$$R_{eq1} = \left(\frac{\left(\left(\frac{C_{dsJ} \cdot C_{gdJ}}{C_{dsJ} + C_{gdJ}} \right) + C_{gsJ} + C_{dsm} \right) + C_{gdm}}{C_{gdm}} \right) \cdot \frac{1}{g_m}. \tag{3}$$

Likewise, analyzing the evolution of the v_{dsm} voltage in the circuit in Fig. 3a, we obtain the simplified circuit in Fig. 3c, where:

$$I_{eq1} = I \cdot \left(\frac{C_{gdm}}{C_{dsm} + C_{gdm}} \right) - g_m \left(v_{gsm} - V_{th} \right), \tag{4}$$

$$C_{eq2} = \left(\frac{C_{gsm} \cdot C_{gdm}}{C_{gdm} + C_{gsm}} \right) + \left(\frac{C_{dsJ} \cdot C_{gdJ}}{C_{dsJ} + C_{gdJ}} \right) + C_{gsJ} + C_{dsm} \tag{5}$$

Figure 4a shows the evolution of v_{gsm} for different driver currents in line with the aforementioned circuit (Fig. 3b) with

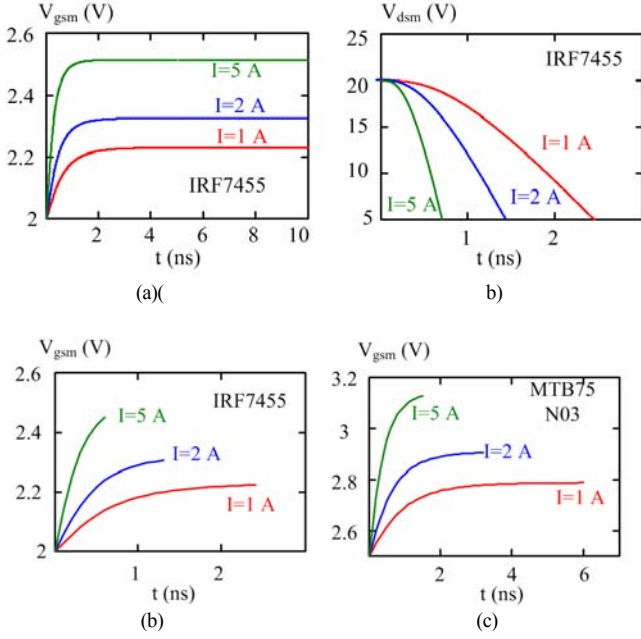|	Normally-On SiC JFET (SJDP120R085)		Low-voltage Si MOSFET (IRF7455)		Low-voltage Si MOSFET (MTB75N03)	
Manufacturer	SemiSouth		International Rectifier		Motorola	
$V_{dsbreakdown}$ (V)	1200		30		25	
I_{dmax} (A)	27		15		75	
R_{DSon_max} (mΩ)	85		7.5		9	
V_{GS_max}/V_{th} (V)/ V_{po}(V)	+15, -15 / -5		+12, -12 / 2		+15, -15 / 2	
g(S)	10		44		32	
C_{iss} (pF)	255	V_{DS}=100 V	3480	V_{DS}=25 V	4025	@
C_{oss} (pF)	80	f=1 MHz	870	f=1 MHz	1353	V_{DS}=25 V
C_{rss} (pF)	80		100		307	f=1 MHz

Fig 4. a) Evolution of v_{gsm} defining a Miller plateau with data from real components (SJDP120R085/IRF7455). b) Evolution of v_{dsm} with data from real components (SJDP120R085/IRF7455). c) Actual evolution of v_{gsm} with data from real components (SJDP120R085/IRF7455). d) Actual evolution of v_{gsm} with data from real components (SJDP120R085/MTB75N03).

data from a real SiC JFET (SJDP120R085) as well as from a real Si low-voltage MOSFET (IRF7455). In this case, the transconductance of the MOSFET has been parameterized from the datasheet. The main data from both devices is summarized in Table I. As can be seen in Fig. 4a, a Miller effect occurs in this transition, as previously deduced. However, the time spent in this transition is defined by the decrease of v_{dsm} until reaching V_{po} (this voltage decrease is more or less between 10 V to 15 V). Figure 4b shows the evolution of v_{dsm}. The discharge of C_{eq2} due to the action of I_{eq1} defines a $[t_2, t_3]$ interval of between 1 ns and 3 ns. The actual evolution of v_{gsm} is thus shown in Fig. 4c. In fact, a Miller effect occurs during this interval. However, as the interval is so short, the effect is almost unappreciable in the evolution of v_{gsm} (Fig. 1).

At this point, a comparison with a normally-on JFET must be established, as it is known that the Miller effect is appreciable at its gate-to-source voltage. It is well known that the interval of duration of the Miller plateau is defined by the

discharge of the drain-to-source parasitic capacitance due to the action of the driver discharging the Miller capacitance. Therefore, the time taken by the driver to discharge the Miller capacitance to zero is greater because its initial voltage is much higher (in the proposed case, it is a hundredth of a volt).The Miller effect is accordingly appreciable at the gate-to-source voltage of a JFET operating alone (not in the cascode configuration).

Returning to the cascode configuration, it should be noted that there is no coexistence between the drain-to-source voltage in the JFET (v_{dsJ}) and i_{dJ} in this interval. This contrasts with the transition in the case of the JFET operating alone, during which the Miller effect occurs (i.e. in the case of the JFET, this interval defines a high level of turn-on power losses due to the coexistence of voltage and current at its output). In the case of the cascode configuration, however, power is dissipated when the C_{dsm} is discharged through the MOSFET channel. It should be noted that these power losses are lower than those introduced during subsequent intervals of the turn-on. It is obvious that the shorter this interval, the lower the losses will be. Taking into account (4) and (5), when chosinng the low-voltage MOSFET, g_m should be as high as possible and all the capacitances of the power MOSFET should be as low as possible. A sensitivity analysis of C_{eq2} was carried out varying each MOSFET capacitance from the values expressed in Table I (from 0.5C to 2C, C being the value of the chosen capacitance, the remaining capacitances being kept constant). The results of this study highlight the influence of C_{dsm} on C_{eq2}. Finally, Figure 4d shows the evolution of v_{gsm} (during the interval $[t_2, t_3]$) choosing an actual low-voltage MOSFET (MTB75N03, see Table 1) with higher parasitic capacitances. As can be seen, the choice of a low-voltage MOSFET with higher parasitic capacitances extends this interval in comparison with Fig. 4c.

3) Interval $[t_3, t_4]$

The gate-to-source voltage of the MOSFET increases again due to the driver current through the gate resistor as an exponential waveform. Furthermore, v_{gsJ} increases above V_{po} in this case, while C_{dsm} is fully discharged. At this point, as the current begins to flow through the JFET, i_{dJ} increases (Fig. 1). The channel of the MOSFET was created at t_2, whereas the channel of the JFET is starting to be created at the beginning of this interval. It therefore seems evident that v_{gsJ} and the transconductance of the JFET (g_J) control the start-up process of the current through the cascode configuration due to the fact that $g_J(v_{gsJ}-V_{po}) \ll g_m(v_{gsm}-V_{th})$ during this interval. In other
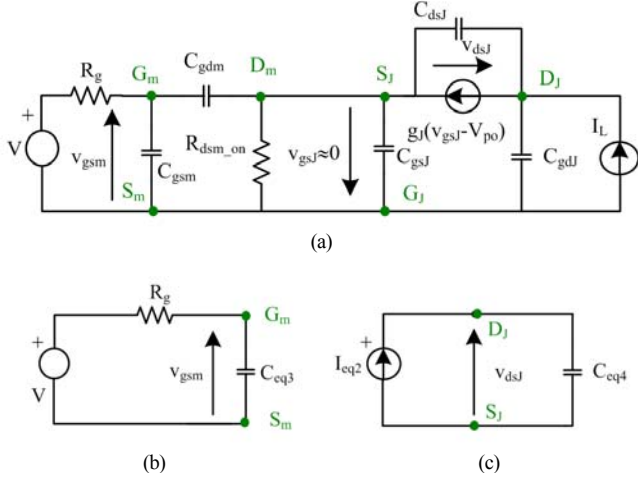
Fig 5. a) Equivalent circuit during the interval [t₄,t₅]. b) Equivalent circuit to calculate v_gsm during the interval [t₄,t₅]. c) Equivalent circuit to calculate v_dsJ during the interval [t₄,t₅].

words, the level of i_{dJ} that the JFET can manage for high values of v_{dsJ} is much lower than the current that the MOSFET can manage when v_{dsm} is close to zero. For the reasons outlined previously, the transconductance of the low voltage MOSFET has no effect on the coexistence between i_{dJ} and v_{dsJ} in this interval in terms of power losses. However, C_{dsm} is not fully discharged at the beginning of this interval, but is subsequently fully discharged during this interval (Fig. 1) from V_{po} to zero. Higher C_{dsm} values therefore prolong the time it takes to fully discharge and hence introduce higher power losses, a fact which is important when choosing the low-voltage MOSFET. It should also be remembered that the parasitic capacitances of the MOSFET at low voltages are higher than at high voltage levels, accentuating this effect.

4) Interval [t₄, t₅]

At the beginning of this interval, both the JFET and the MOSFET manage the inductor current I_L. Furthermore, v_{dsm} is almost zero. The equivalent circuit of this interval is shown in Fig. 5. During this interval, v_{gsm} increases as an exponential waveform and v_{dsJ} decreases linearly. As can be seen, the effect of the JFET does not affect the behavior of the MOSFET and *vice versa*, due to the fact that v_{dsm} is almost zero and it behaves as a resistor. Therefore, the input to the cascode (i.e. v_{gsm}) and the output from the cascode (i.e. v_{dsJ}) can be independently analyzed as shown in the equivalent circuits in Fig. 5b and Fig. 5c, where:

$$C_{eq3} = C_{gdm} + C_{gsm},$$ (7)

$$I_{eq2} = I_L + g_J V_{po},$$ (8)

$$C_{eq4} = C_{gdJ} + C_{dsJ}.$$ (9)

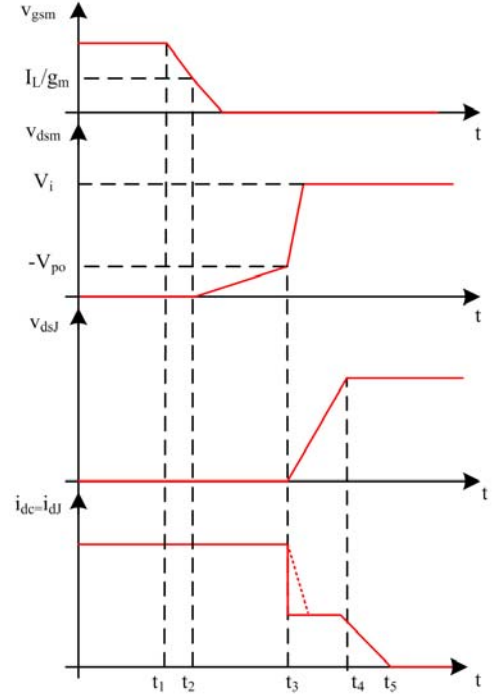In this interval, C_{dsJ} is discharged by the action of the

Fig. 6. Main waveforms of the turn-off transition of the cascode configuration..

$g_J(v_{gdJ}-V_{po})$ current source (see Fig. 5; in this analysis, $V_{po}<0$). Thus, the MOSFET and its driver do not affect the discharge of C_{dsJ}. Therefore, the choice of the low-voltage MOSFET and its driver does not affect the losses corresponding to this interval. However, the evolution of v_{gsm} determines the on-resistance of the power MOSFET (R_{dsm_on}), and hence the conduction losses. Therefore, when choosing the low-voltage MOSFET, C_{gsm} should be as low as possible and the diver current (I) as high as possible.

At this point, it should be stated that the discharge of C_{dsJ} in the case of a normally-on JFET working alone (without a MOSFET in cascode configuration) is different to that described previously for the reason that it depends on the driver current and the Miller capacitance. Thus, the coexistence of v_{dsJ} and i_{dJ} strongly depends on the driver current (I) and the Miller capacitance in this case.

5) Interval [t₅, t₆]

Once v_{dsJ} has reached zero, v_{gsm} increases in order to reduce R_{dsm_on} (Fig. 1).

B. Switching behavior at turn-off

The turn-off process of the cascode configuration will now be studied following the same procedure described previously for the turn-on. Figure 6 shows the turn-off waveforms of the cascode over an inductive load circuit. All the transitions of the waveforms in each interval will be properly explained over the equivalent circuit shown in Fig 2b.

1) Interval [t₁,t₂]

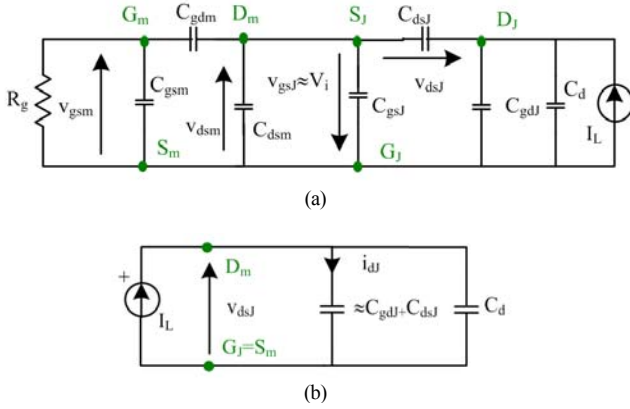Prior to t_1, the output voltage of the driver is at its

(a)

(b)

Fig 7. a) Equivalent circuit during the interval [t_3, t_4]. b) Equivalent circuit to calculate v_{dsJ} during the interval [t_3, t_4].

maximum value and the low-voltage MOSFET is on; so v_{dsm} is zero. This voltage is applied between the gate and the source of the JFET ($v_{gdJ}=-v_{dsm}$). Therefore, the JFET is also on due to the fact that v_{gsJ} is higher than V_{po} (e.g. $v_{gsJ}\approx0$, while $V_{po}=-5$ V). This interval starts at t_1, when v_{gsm} decreases, and ends at t_2, when v_{gsm} reaches the value I_L/g_m (Fig. 6).

2) Interval [t_2,t_3]

From t_2 on, the MOSFET is being turned-off and therefore v_{dsm} begins to increase due to the action of the inductor current (I_L) which is flowing through the JFET charging C_{dsm}. Note that the v_{dsm} level is very low in this interval. The value of C_{dsm} at this v_{dsm} level (remember C_{dsm} decreases as its voltage increases) is very high in comparison to its value at higher v_{dsm} levels. A dead time thus appears between the decrease of v_{gsm} and the increase of v_{dsm}. Furthermore, v_{gsm} reaches zero during this interval.

In this interval, coexistence appears between I_L and v_{dsm} in the output of the low-voltage MOSFET. The dead time is defined by the C_{dsm} charge. As C_{gsm} is high, the charge process is slow. Therefore, low C_{gsm} at low voltages should be chosen in order to decrease the power losses in this transition when chossing the low-voltage MOSFET

Moreover, v_{dsm} is applied between the gate and the source of the JFET ($v_{gsJ}=-v_{dsm}$) and this interval ends when v_{gsJ} decreases until V_{po}. Note that this transition does not appear in the turn-off of a normally-on JFET used alone.

3) Interval [t_3, t_4]

At the beginning of this interval, v_{dsm} continues to increase and is clamped to a voltage defined by the leakage current of the JFET when it is off (V_i). Note that this transition is very short due to the fact that the C_{dsm} values at this v_{dsm} level are much lower than in the previous interval. In this case, the same considerations regarding C_{dsm} as in the previous interval cannot be taken into account from the point of view of power losses because there is no coexistence of voltage and current at the output of the MOSFET due to the fact that $v_{gsm}<V_{th}$.

Furthermore, at the beginning of this interval, both the

JFET and the diode are off. The equivalent circuit of this interval is shown in Fig. 7. In this case, a current divider is created between the JFET capacitances (C_{dsJ} and C_{gdJ}) and the Schottky diode capacitance (C_d), as shown Fig.7b. At this point, a step in i_{dJ} should take place because the current (I_L) must not only charge C_{dsJ} and C_{gdJ}, but also discharge C_d (Fig. 6). In the real world, however, parasitic impedances (inductances and capacitances between the source of the MOSFET and the ground of the circuit) cause a softer transition, as shown in Fig. 6, in the evolution of i_{dJ} (dotted line).

The end of this interval is defined by both the total discharge of C_d and the total charge of ($C_{dsm}+C_{dsm}$), as shown in Fig. 6 (which is equivalent to the charge of both $C_{dsm}+C_{dsm}$ and the discharge of C_d). This interval is defined by the coexistence of i_{dJ} and v_{dsJ} in the turn-off transition.

Note that this effect (i.e. the current divider with C_d) will be due to the fact that a Schottky diode is used in the circuit as a freewheeling diode. This effect may also appear in the turn-off transition of a JFET working alone.

4) Interval [t_4,t_5]

In this interval, the diode is on and I_L is completely conducted by the diode just at the end of this interval (Fig. 6).

III. CONTINUOUS CONDUCTION MODE OPERATION

The purpose of this section is to analyze both switching transitions for the single JFET and the cascode configuration experimentally and compare the previously presented switching model of the cascode configuration with the well-known model corresponding to the JFET working alone. To achieve this goal, a boost converter operating in CCM was tested. It should be noted that this mode of operation generates losses in both transitions and hence information on the switching process in both turn-on and turn-off is available. In the case of the cascode configuration, two different low-voltage Si MOSFETs with different parasitic capacitances were tested to test all the key points regarding the influence of the MOSFET features on the model previously developed for the cascode configuration.

A. Converter specifications and components.

As described previously, the converter chosen to carry out the comparison in switching behavior between the different configurations was the boost converter. Several features, such as the simplicity and the low number of components of this converter, make it a good solution for comparing the devices under test. The schematic design of the boost converter is presented in Fig. 8.

The converter operates at an input voltage of 150 V_{dc} and an output voltage of 400 V_{dc}. The chosen output power for this analysis was 600 W and, as the main goal was to study both switching transitions of the main switch, CCM was chosen initially. The switching frequencies in this conduction mode ranged from 100 kHz to 200 kHz in order to keep the
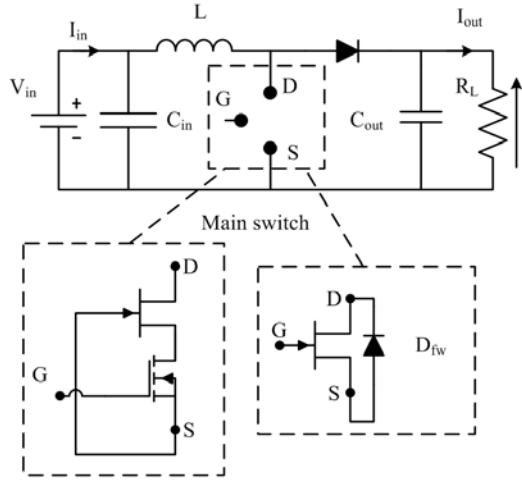
Fig. 8. Schematic design of the boost converter.

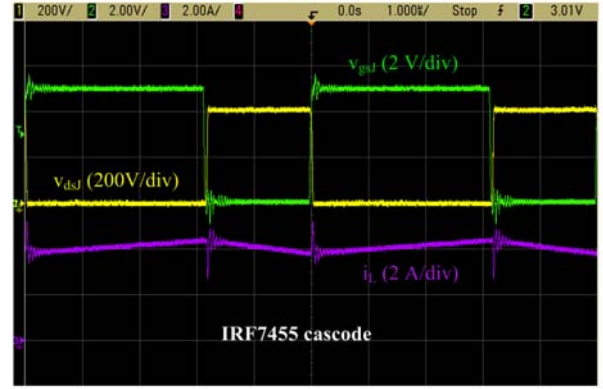TABLE II. MOST RELEVANT FEATURES OF C3D10060A

	SiC Schottky diode (C3D10060A)
Manufacturer	Cree
$V_{breakdown}$ (V)	600
I_{max} (A)	10
$V_{forward}$ (V)	2.4
C_d (pF)	
V_R= 0 V, T_J= 25 ºC, f = 1 MHz	480
V_R= 200 V, T_J= 25 ºC, f = 1 MHz	50
V_R= 400 V, T_J= 25 ºC, f = 1 MHz	42

(a)

(b)

Fig. 9. Main waveforms of the boost converter at 200 kHz, 600 W and CCM for: a) IRF7455 cascode, and b) JFET.

switching losses below a reasonable value, as the switching losses would become unmanageable at higher frequencies, bearing in mind that forced cooling was not used in this prototype.
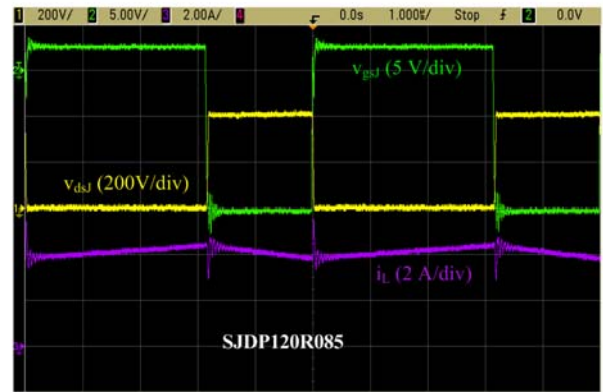
The output rectifier of the boost converter is a SiC-Schottky diode with a maximum breakdown voltage of 600 V (Table II). The reason for choosing this diode was to avoid the high reverse recovery current of a Si diode that would excessively influence the turn-on losses of the main switch, which is the device under test. Although the SiC diode also has some reverse recovery losses, the peak value and the time during which the negative current of this diode exists are much lower than in the case of an ultrafast Si diode.

The devices under test were a 1200 V normally-on SiC JFET and the cascode, composed of the aforementioned SiC JFET and a low-voltage Si MOSFET connected as shown in Fig. 2a and Fig. 8. In both cases, the devices act as the main switches of the boost converter. The most important features of the devices used in the converter (including the two different low-voltage MOSFETs for the cascode configuration) are listed in Table I.

In the case of the cascode configuration, a commercial driver was used to switch the device due to the fact that the controlled device is a standard low-voltage MOSFET. However, the normally-on feature of the SiC JFET means

that it is necessary to implement a new driver to control this device properly. This new driver has to be able to supply -15 V to turn off the device and a voltage of between 0 and 2 V during the on-state (values directly recommended by the manufacturer). The reason for applying 2 V instead of 0 V to turn on the JFET is to improve the on-resistance of this device, thereby slightly reducing conduction losses. Taking all these considerations into account, a new driver was developed for the SiC JFET as can be seen in [16]. Note that this driver's capability to supply current is provided by an IC EL7156 manufactured by INTERSIL® (i.e. 3.5 A peak).

Finally, the boost converter inductor for this conduction mode was designed to have a peak-to-peak current ripple of 20% of the mean value of the current. In the case of a switching frequency of 100 kHz, an inductance of 1.1 mH was chosen. The same inductor was used for the switching frequency of 200 kHz, reducing the current ripple to only 10 % of its mean value. The inductors were optimized to have the minimum losses, thereby avoiding their influence on the analysis of switching losses in terms of the efficiency of the converter, as will be described below.

Figure 9 shows the inductor current (i_L), the gate-source
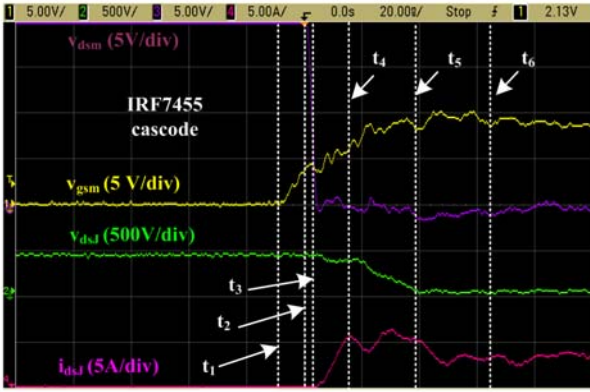
(a)
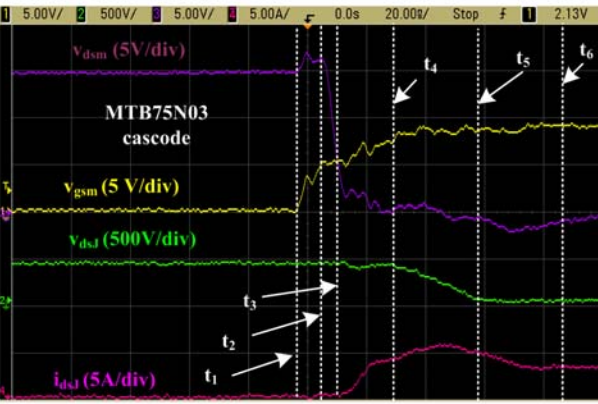
(b)

Fig.10. a) Experimental results of the turn-on transition of the SJDP120R085/IRF7544 cascode. b) Experimental results of the turn-on transition of the SJDP120R085/MTB75N03 cascode.
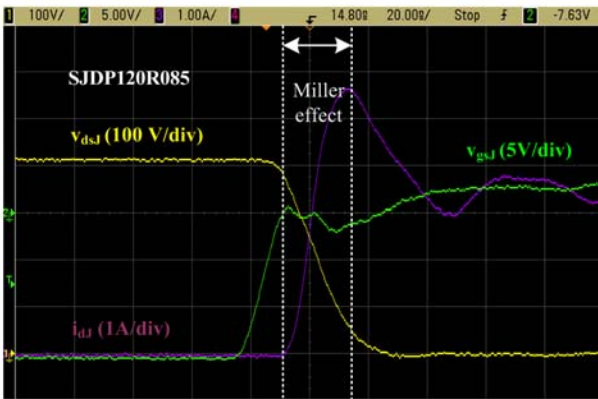

Fig. 11. Experimental results of the turn-on transition of the SJDP120R085 JFET.

voltage and the output voltage of the main switch of the boost converter operating in CCM at a frequency of 200 kHz for the cascode with the IRF7455 and the single JFET. The waveforms for the cascode with the MTB75N03 are very similar to the configuration with the IRF7455. The duty cycle

under these conditions to boost the voltage from 150 V at the input to 400 V at the output was d = 0.625.

B.   Switching behavior.

In order to verify the proposed analysis for the cascode configuration (Section II) and to determine the differences in the switching process between the single JFET and the cascode configuration, the boost converter operates initially in CCM with hard switching conditions at a frequency of 100 kHz. Thus, neither turn-on nor turn-off losses can be neglected. The switching losses are calculated from the waveform data of the drain current of the transistors and their drain-source voltage obtained using an oscilloscope (Fig. 10, Fig. 11, Fig. 12 and Fig. 13).

Figure 10a shows the drain current, the gate-source voltage and the output voltage of the SJDP120R085/IRF7455 cascode. The drain to source voltage of the low-voltage MOSFET was also measured. Figure 10b shows the same waveforms for the SJDP120R085/MTB75N03 cascode. The waveforms for both cascodes are very similar. Furthermore, all the transitions described in the previous study are highlighted on the plots (in white). As can be seen, the experimental results match the proposed intervals of the turn-on: the charge of v_{gsm} [t_1, t_2], the "small" Miller effect with the v_{dsm} discharge [t_2, t_3], the increase of i_{dJ} [t_3, t_4] and the decrease of v_{dsJ} [t_4, t_5].

However, some real effects appear in the waveforms which have not been previously explained. For example, in the interval [t_3, t_4], the decrease of v_{gdm} is reflected in v_{dsJ}. This is due to the parasitic inductance in the connection between the cascode drain and the anode of the Schottky diode. Moreover, some ringing is appreciated in real waveforms, which was neglected in the theoretical analysis.

Figure 11 shows the same waveforms for the turn-on of the SJDP120R085 JFET when working alone. As previously stated, the switching transition is different. In this case, a Miller plateau appears in v_{gsJ} when the drain-to-source voltage of the JFET decreases to zero. Furthermore, the time of this interval is defined by the C_{gsJ} and the driver current.

The experimental results of the turn-off are presented next. Figure 12a shows the drain current, the gate-source voltage and the output voltage of the SJDP120R085/IRF7455 cascode. In this case, the drain-to-source voltage of the MOSFET was also measured. Figure 12b shows the same waveforms for the SJDP120R085/MTB75N03 cascode. All the transitions described in the previous study are highlighted on the plots (in white). As can be seen, the experimental results match the proposed intervals of the turn-off: the decrease of v_{gsm} [t_1, t_2], the discharge of C_{dsm} which introduces a delay [t_2, t_3], the decrease of i_{dJ} and the increase of v_{dsm} imposed by the current divisor formed by C_d and C_{dsJ} [t_3, t_4] and the current passing through the diode [t_4, t_5]. As in the case of the turn-on, the experimental results match the proposed intervals defined in the theoretical analysis of the turn-off. In this case, the waveforms for both cascodes are
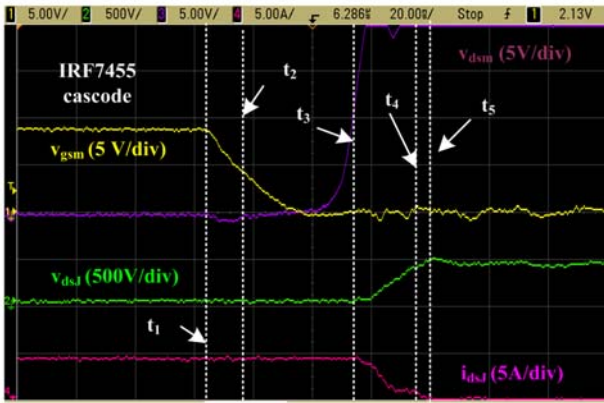
(a)
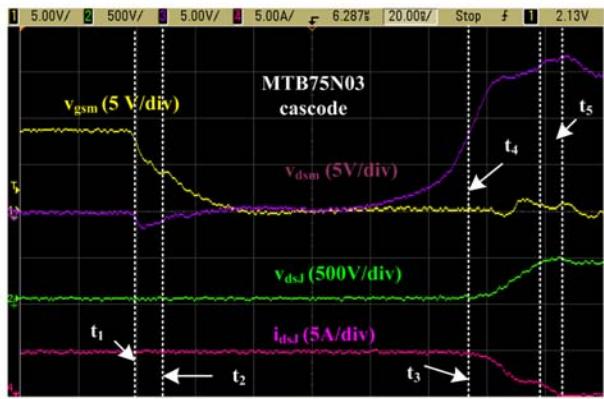
(b)

Fig. 12. a) Experimental results of the turn-off transition of the SJDP120R085/IRF7544 cascode. b) Experimental results of the turn-off transition of the SJDP120R085/MTB75N03 cascode.
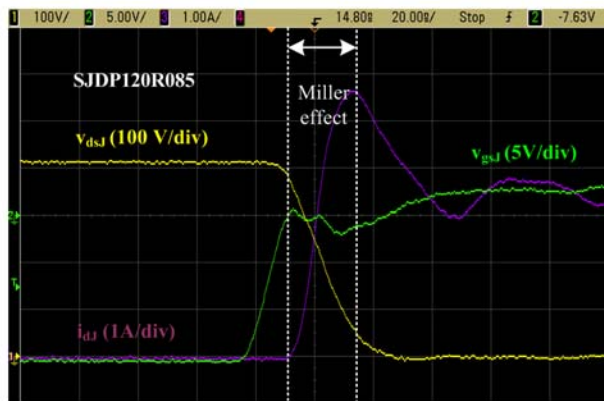

Fig. 13. Experimental results of the turn-off transition of the SJDP120R085 JFET.

different due to the delay imposed by the C_{dsm} capacitance (i.e. $C_{dsmIRF7544} < C_{dsm\ MTB75N03}$) in the interval $[t_2, t_3]$. Furthermore, the effect of the parasitic inductance between the source of the MOSFET and ground of the setup can be seen in i_{dJ}.

In this case, some real effects also appear due to parasitic inductances in the experimental results. Some kind of Miller effect appears in v_{gsm} due to parasitic inductance between the source of the MOSFET and the ground of the setup when v_{dsm} starts to increase (the interval $[t_1-t_2]$).

Figure 13 shows the same waveforms for the turn-off of the SJDP120R085 JFET. No delay appears due to C_{dsm}. In other words, when v_{gsJ} reaches V_{po}, v_{dsJ} then begins to decrease with no major delay due to the C_{dsm} of the low-voltage MOSFET. In this case, a Miller plateau appears when v_{dsJ} decreases. Finally, the coexistence of i_{dJ} and v_{dsJ} determines the power losses of the turn-off transition in the JFET and the energy stored mainly in C_{dsJ} and C_{dgJ}. As can be seen, the coexistence of v_{dsJ} and i_{dJ} is more or less similar to that of the cascodes

C. Switching energies.

The switching energies of both transitions were calculated from the experimental data of the waveforms shown in Fig. 10, Fig. 11, Fig. 12 and Fig. 13 by multiplying of i_{dJ} by v_{dsJ} and integrating the result. This process is carried out using MATLAB® in order to increase the accuracy obtained on the oscilloscope. To carry out the measurements, the probes were previously calibrated to avoid possible delays between them and errors in gain, thus increasing precision. The experimental setup does allow characterization of the devices under test in terms of providing a precise value of the switching losses, although it is perfectly valid to compare the different devices. Furthermore, the purpose of this paper is not to provide a precise model for obtaining these losses, but to estimate the differences in the switching process of the two SiC-based solutions.

Figure 14 shows the instantaneous switching power and the switching energies for the three tested devices (i.e. single JFET, IRF7455 cascode and MTB75N03 cascode) at a switching frequency of 100 kHz and an output power of 600 W. From this figure, the difference between the switching energies (total area of the depicted instantaneous power represented in Fig. 14c) in the turn-off of the JFET and the cascode with two different low-voltage MOSFETs can be seen to be almost imperceptible. There is, however, a marked variation in the turn-on energy between these three set-ups, the JFET being seen to be the main switch that performs best in this transition. This is because the driver used (i.e. an IC EL7156 from INTERSIL®; 3.5 A peak) discharges the Miller capacitance of the JFET faster than the product of g_m and $(v_{gsm}-V_{th})$ which defines the same discharge in the cascode configuration. Obviously, the behavior of the cascode is markedly worse when a low-voltage MOSFET with both higher parasitic capacitances and lower g_m is used in $[t_2, t_3]$ and $[t_4, t_5]$, as was deduced in the theoretical analysis. However, this effect is only noticeable in the turn-on process at this switching frequency.
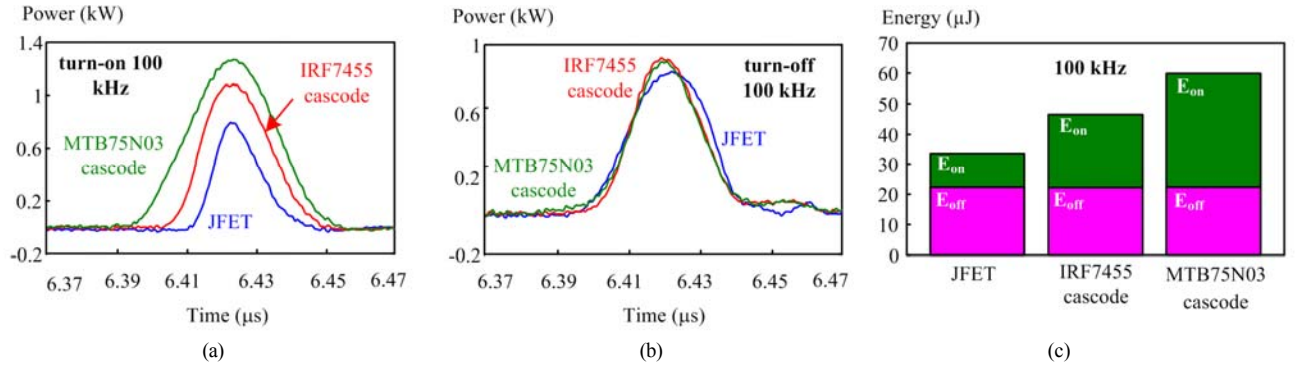
(a)   (b)   (c)

Fig. 14. Instantaneous switching power of the main switch at 100 kHz, 600 W and CCM in: a) Turn-on, and b) Turn-off. c) Switching energies.
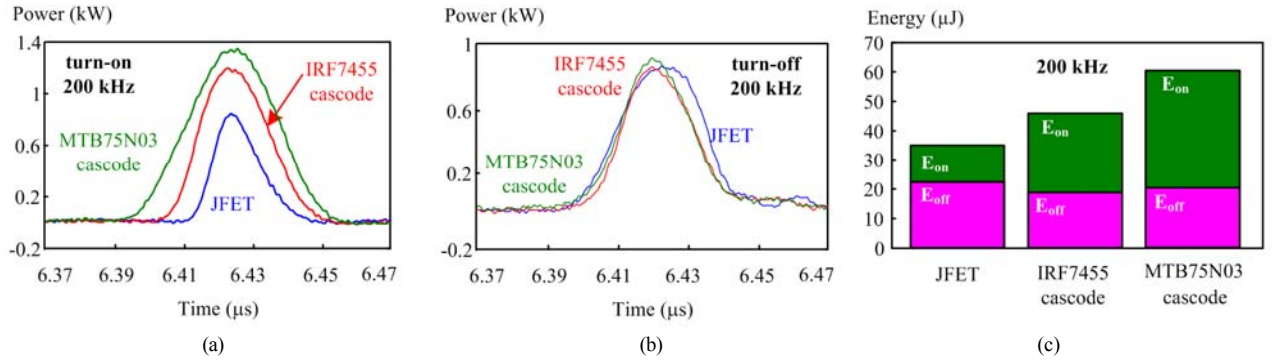

(a)   (b)   (c)

Fig. 15. Instantaneous switching power of the main switch at 200 kHz, 600 W and CCM in: a) Turn-on, and b) Turn-off. c) Switching energies.

The same waveforms, though with the converter operating at a switching frequency of 200 kHz in this case, are shown in Fig. 15. These waveforms are similar to those in Fig. 14, although some slight differences can be noted. For example, real differences can be seen in the detail of the instantaneous power at turn-off (Fig. 15b) between the different devices under test. This is more noticeable in the chart in Fig. 15c, where the cascode configuration has a lower turn-off energy than the single JFET. The conclusions drawn from the turn-on energies are the same as in the case in which the converter operates at a switching frequency of 100 kHz and verify that the turn-off transition of the cascode configuration is better than that of the JFET configuration. Furthermore, the effect of the C_{dsm} delay appears in the cascode configuration energy results, making the transition of the SJDP120R085/MTB75N03 cascode worse due to its greater C_{dsm}.

D. Efficiency results.

This subsection presents the efficiency results of the boost converter operating in CCM at 600 W for the aforementioned configurations (i.e. IRF7455 cascode, MTB75N03 cascode and single JFET). Furthermore, a number of conclusions are drawn from these results making certain simplifications that will be explained below. These conclusions will allow us to verify the theoretical analysis of the switching transitions for both single JFET and cascode configuration.

As stated in subsection A. , all the components of the boost converter are the same for the different configurations

under test, with the exception of the main switch. As the output power is also the same, the capacitor losses, inductor losses and output diode losses can be considered equal. Moreover, the R_{dsm} of the two low-voltage MOSFETs used in the cascode configuration is ten times smaller than that of the JFET (Table I). This difference in the R_{dsm} between the cascode and the JFET working alone yields a theoretical variation of 0.08 W in the conduction losses for a power of 600 W, allowing us to consider losses of this type as constant. Having made these simplifications, the efficiency of the converter may be considered a suitable magnitude to compare the switching losses of the devices under test. As the converter operates in CCM, the efficiency only points out the difference in the overall switching losses (turn-on plus turn-off) between the different configurations, but does not allow comparison between the turn-on and turn-off losses of the devices under test.

The measured efficiency as a function of the switching frequency for the different configurations of the main switch in the boost converter operating in CCM at 600 W is given in Fig. 16. In this conduction mode, the JFET shows the best results in terms of efficiency at 100 kHz, followed by the IRF7455 cascode and the MTB75N03 cascode, mainly due to the difference in the turn-on energies described previously (the turn-off energies at 100 kHz are roughly the same). At 200 kHz, the turn-off energies of the two different cascodes are slightly lower than those of the JFET, as can be appreciated in Fig. 15c. However, this difference is much smaller than the improvement in the turn-on energy of the
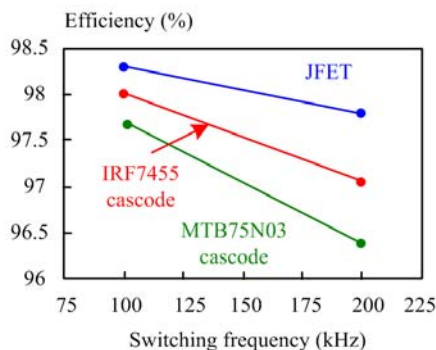
Fig. 16. Schematic design of the boost converter.

(a)

(b)

Fig. 17. Main waveforms of the boost converter at 1 MHz, 600 W and DCM for: a) IRF7455 cascode and b) JFET.for: a) IRF7455 cascode, and b) JFET.

JFET with respect to both cascode configurations, which means that the total switching energy in the JFET presents the lowest value. This explains why the difference in efficiency is greater between the tested configurations for higher frequencies. All these results point to the single JFET as the best option in CCM in terms of efficiency.

It should be noted that all the energy involved in the turn-off when the converter is operating in CCM is totally dissipated, one part in the turn-off process itself and another part during the turn-on process. Although these results show the better overall switching behavior of the single JFET, the efficiency results do not allow us to distinguish between the two switching losses terms of the devices under test. In order to compare only one term of the switching losses directly and verify the theoretical conclusions drawn in Section II, the boost converter was tested in DCM. In this conduction mode, the turn-on losses can be eliminated by achieving Zero Voltage Switching (ZVS) in the main switch [17-19]. Moreover, as opposed to CCM, part of the energy involved in the turn-off (that stored in the device output capacitor) is recovered in this mode of operation. Therefore, the switching energies calculated in this case are not equivalent to switching losses. The differences in turn-off losses can hence be analyzed with more accuracy.

## IV. DISCONTINUOUS CONDUCTION MODE OPERATION

DCM operation was also employed in the boost converter to study the turn-off switching process of the main switch for two reasons. First, employing this conduction mode, ZVS can be achieved at turn-on of the main switch and hence turn-on losses can be neglected and only the turn-off losses of this switch have to be taken into account. Second, as the overall switching losses of the main switch are significantly reduced, the switching frequency can be increased, making the differences in the turn-off energies of the different configurations more noticeable in terms of efficiency. Only the single JFET and the IRF7455 cascode will be tested in this conduction mode.

A. Converter specifications and components.

The specifications of the boost converter for this
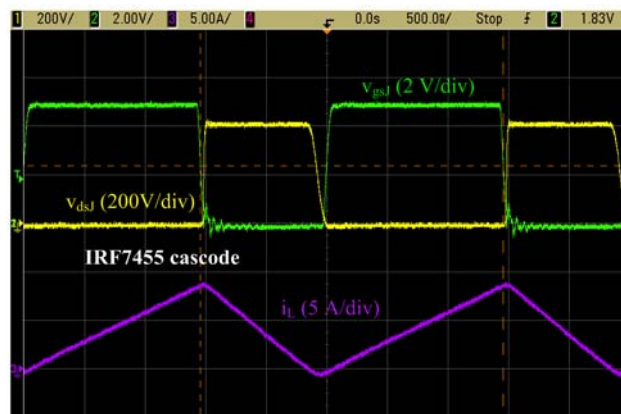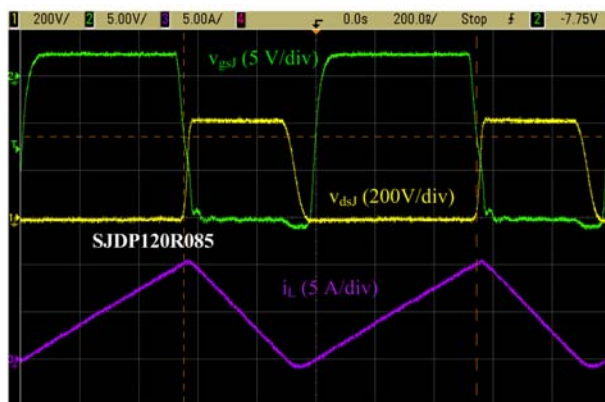
conduction mode are the same as in CCM (i.e. input and output voltages of 150 V and 400 V, respectively, and an output power of 600 W), with the exception of the frequency, which, as the overall switching losses are significantly reduced by achieving ZVS, was allowed to range from 100 kHz up to 1 MHz. Note that the performance of the SiC Schottky diode is better than that of the Si Ultrafast diode, even if ZVS is achieved in the turn-on of the diode [19]. Accordingly, the SiC Schottky diode was also used in DCM.

The components of the boost converter are also the same as in CCM, with the exception of the inductor. In this conduction mode, ZVS is achieved by discharging the output capacitance of the transistor completely before turning it on. Obviously, the equivalent output capacitance of the cascode and the JFET working alone are different because of the addition of the low-voltage MOSFET. Therefore, slight modifications were made in the value of the converter inductor (by changing the gap in the inductor) in order to achieve ZVS.

To better understand this particular DCM operation, Fig. 17 shows the gate and output voltage of the main switch and the inductor current of the boost converter for a switching
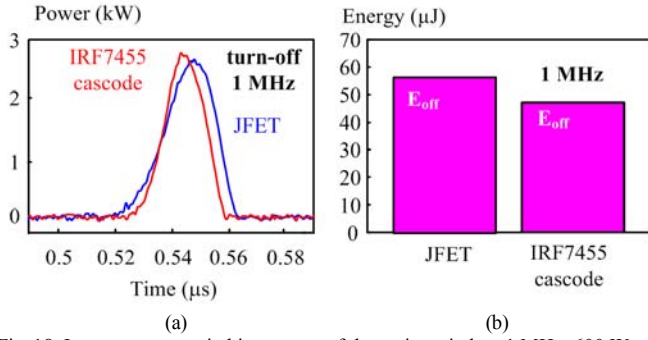
Fig. 18. Instantaneous switching power of the main switch at 1 MHz, 600 W and DCM in: a) Turn-off, b) Switching energies.
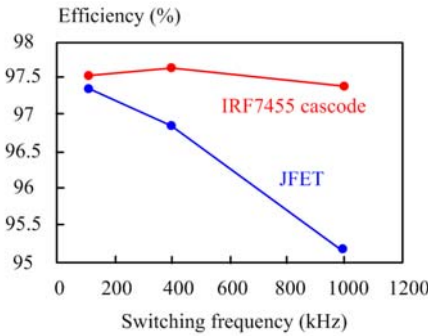

Fig. 19. Efficiency of the boost converter in CCM and an output power of 600 W.

frequency of 1 MHz when using the single JFET and the cascode. It can be seen that the slightly negative current of the inductor is used to discharge the output capacitance of the main switch. This switch is turned on once its drain-source voltage has reached zero, thus achieving ZVS. As the JFET does not have a parasitic diode between the drain-source, a SiC diode (the same diode as used at the output of the boost converter) was placed in parallel with this device to drive the negative current once the output capacitor has been completely discharged. In the case of the cascode, an external diode is not needed as this current can flow through the parasitic diode of the low-voltage MOSFET and the channel of the JFET due to its normally-on structure.

B. Switching energies.

In this particular DCM operation, ZVS is achieved in the turn-on of the main switch as previously described. Figure 18 shows the instantaneous power and switching energies at turn-on of the main switch when the boost converter operates at 600 W, DCM and 1 MHz switching frequency. Both figures show the substantial difference between the single JFET and the IRF7455 cascode in terms of the switching energies in the turn-off transition. This difference was not deduced in the theoretical analysis because no accessible data on the two devices (SJDP120R085 and IRF7544) can be obtained from their datasheets in order to determine a difference. Nonetheless, it was deduced that the delay imposed by C_{dsm} in the cascode configuration enables a better scenario at the coexistence of v_{dJ}

and i_{dJ} in this configuration, reducing the turn-off energies with respect to the JFET working alone.

As stated at the end of Section III.D, it should be noted that not all the energy involved in the turn-off process is dissipated into the semiconductor devices during turn-off, neither in the cascode configuration nor in the case of the JFET working alone. A considerable part of this energy (95% of the total turn-off energy of the cascode configuration and about 70% of that energy in the case of the JFET working alone) is stored in parasitic capacitances and is eventually recovered in the turn-on process.

Another important point to bear in mind is that the turn-off switching energies for this conduction mode are higher than the same term of switching energy in the case of CCM even for the same output voltage and power processed by the converter. The reason for this is that the current ripple in the inductance is much higher in DCM than in the case of CCM for the same power. Comparatively speaking, when the main switch turns off in DCM, the current through it is therefore much higher than in CCM, leading to higher energies in this transition.

C. Efficiency results.

This subsection presents the efficiency results for the single JFET and the IRF7455 cascode configuration in the boost converter operating in DCM at an output power of 600 W.

As previously described, although the inductor is the same in both configurations, slight modifications have to be made in the value of the inductance to achieve ZVS due to the different output capacitance of the single JFET and the IRF7455 cascode configuration. However, these variations are minimal and the losses in inductance can be considered the same for both configurations at the same switching frequency. Employing this simplification and the others described in the previous section (i.e. same capacitor losses, same output diode losses and same conduction losses in the devices under test for both configurations), the efficiency can be considered as a comparative way to assess the turn-off losses of the main switch when the converter operates in this particular DCM.

The measured efficiency of the boost converter operating in DCM at an output power of 600 W for the two different configurations under test is given in Fig. 19. The turn-off losses at 100 kHz are practically identical in the case of the IRF7455 cascode and the JFET to those presented in Section III.C. Hence, the measured efficiency is almost the same at this frequency. As the switching frequency increases, however, slight differences in the turn-off energy of the main switch represent a large part of the switching losses, with the consequent major impact on efficiency. The graph shows an improvement of 0.5% in the case of the cascode at 400 kHz and 2% at 1 MHz, making this configuration the most suitable one for high switching frequencies in DCM when ZVS is achieved.

At low frequency, DCM presents a lower efficiency than CCM mainly due to the fact that the conduction losses in all the components are greater because of the higher current ripple, which leads to higher rms values. However, when the frequency increases and the switching losses become more substantial, DCM provides higher efficiency values.

V. CONCLUSIONS

The switching performance of two of the most widespread solutions using SiC high-voltage devices (i.e. a SiC normally-on JFET and a SiC JFET/Si MOSFET cascode configuration) has been studied and compared in this paper. First, a theoretical analysis of the cascode configuration in both switching transitions has been presented. The main differences with respect to traditional normally-on JFET transitions have been highlighted in this study. Conclusions regarding both the transitions of cascode configuration and the influence of their components on its switching behavior have likewise been presented. To verify the theoretical results, a number of tests were carried out in CCM to obtain information on the performance in both switching transitions. The chosen topology to test the different configurations was a 600-W boost converter due to its simplicity and low number of components, which reduce uncertainty in the measurements.

The study carried out in this paper confirms that the overall switching losses of the JFET in CCM are lower, making it more suitable for operating in this mode in terms of overall converter efficiency. However, the lower turn-off losses of the cascode point to this device as the most appropriate one for DCM when ZVS is achieved at the turn-on of the main switch.

REFERENCES

[1] J.A. Cooper, A. Agarwal, "SiC power-switching devices. The second electronics revolution?". Proceedings of the IEEE, vol. 90, n. 6, pp. 956-968. June 2006.

[2] A. Elasser, P. Chow, "Silicon carbide benefits and advantages for power electronics circuits and systems". Proceedings of the IEEE, vol. 90, n. 6, pp. 969-986. June 2002.

[3] J. Millán, "Wide band-gap power semiconductor devices". IET Circuits Devices and Systems, vol. 1, n. 5, pp. 372-379. 2007.

[4] Application Note AN-SS1, "SiC Enhancement-Mode Junction Field Effect Transistor & Recommendations for Use", SemiSouth.

[5] K. Mino, S. Herold, J. W. Kolar, "A Gate Drive Circuit for Silicon Carbide JFET", Industrial Electronics Society, Annual Conference of the IEEE, vol. 2, pp. 1162-1166, 2003.

[6] S. Round, M. Heldwein, J. Kolar, I. Hofsajer, and P. Friedrichs, "A SiC JFET driver for a 5 kW, 150 kHz three-phase PWM converter", Industry Applications Conference, IAS Annual Meeting, vol. 1, pp. 410-416, 2005.

[7] T. Friedli, S.D. Round, D. Hassler, J.W. Kolar, "Design and Performance of a 200-kHz All-SiC JFET Current DC-Link Back-to-Back Converter". IEEE Transactions on Industry Applications, vol. 45, no. 5, pp. 1868-1878. Sept.-oct. 2009.

[8] Lai Rixin, Wang Fei, R. Burgos, D. Boroyevich, Zhang Di, Ning Puqi, "A Shoot-Through Protection Scheme for Converters Built With SiC JFETs". IEEE Transactions on Industry Applications, vol. 46, no. 6, pp. 2495-2500. Nov.-Dec. 2010.

[9] C. Bernal, P.M. Gaudo, A. Gallego, A. Otin, J.M. Burdio, "Half-bridge resonant inverter for domestic induction heating based on silicon carbide technology". 2012 Twenty-Seventh Annual IEEE Applied Power Electronics Conference and Exposition (APEC), pp. 2218-2222. 5-9 Feb. 2012.

[10] A. Mihaila, F. Udrea, R. Azar, G. Brezeanu, "Analysis of static and dynamic behaviour of SiC and Si devices connected in cascode configuration". Semiconductor Conference (CAS) 2001, vol. 2, pp. 333-336, 2001.

[11] Aggeler, D.; Biela, J.; Kolar, J.W., "Controllable dυ/dt behaviour of the SiC MOSFET/JFET cascode an alternative hard commutated switch for telecom applications," Applied Power Electronics Conference and Exposition (APEC), 2010 Twenty-Fifth Annual IEEE , vol., no., pp.1584,1590, 21-25 Feb. 2010

[12] Huang, Xiucheng; Liu, Zhengyang; Li, Qiang; Lee, Fred.C., "Evaluation and application of 600V GaN HEMT in cascode structure," Applied Power Electronics Conference and Exposition (APEC), 2013 Twenty-Eighth Annual IEEE , vol., no., pp.1279,1286, 17-21 March 2013.

[13] Pittini, R.; Zhe Zhang; Andersen, M.A.E., "SiC JFET cascode loss dependency on the MOSFET output capacitance and performance comparison with Trench IGBTs," Applied Power Electronics Conference and Exposition (APEC), 2013 Twenty-Eighth Annual IEEE , vol., no., pp.1287,1293, 17-21 March 2013.

[14] Wu, Y.-F., "Paralleling high-speed GaN power HEMTs for quadrupled power output," Applied Power Electronics Conference and Exposition (APEC), 2013 Twenty-Eighth Annual IEEE , vol., no., pp.211,214, 17-21 March 2013.

[15] S.K. Singh, F. Guedon, R. McMahon, "Comparative switching behaviour of silicon transistors and practical silicon carbide transistors". International Conference on Power Electronics and Drive Systems (PEDS) 2009, pp. 585-590, 2009.

[16] Rodriguez, A.; Fernandez, M.; Vazquez, A.; Lamar, D.G.; Arias, M.; Sebastian, J., "Optimizing the efficiency of a dc-dc boost converter over 98% by using commercial SiC transistors with switching frequencies from 100 kHz to 1MHz," Applied Power Electronics Conference and Exposition (APEC), 2013 Twenty-Eighth Annual IEEE , vol., no., pp.641,648, 17-21 March 2013

[17] Yifeng Wu; Jacob-Mitos, M.; Moore, M.L.; Heikman, S., "A 97.8% Efficient GaN HEMT Boost Converter With 300-W Output Power at 1 MHz," Electron Device Letters, IEEE , vol.29, no.8, pp.824,826, Aug. 2008

[18] Zhang Junhong, Lai Jih-Sheng, Kim Rae-Young, Yu Wensong, "High-power density design of a soft-switching high-power bidirectional dc-dc converter". IEEE Transactions on Power Electronics, vol. 22, issue 4, pp. 1145-1153, 2007.

[19] Daniel Costinett, Dragan Maksimovic, Regan Zane, Alberto Rodríguez, "Comparison of Reverse Recovery Behavior of Silicon and Wide Band Gap Diodes in High Frequency Power Converters", In Proc. IEEE Workshop Contr. Modl. (COMPEL)., june, 2013.

Alberto Rodríguez-Alonso (S'07) was born in Oviedo, Spain, in 1981. He received the M.S. degree in telecommunication engineering in 2006 from the University of Oviedo, Gijón, Spain, and the Ph. D. degree in the same university in 2013.

In 2006, he has been a Telecommunications Engineer with the Government of the Principality of Asturias and an Assistant Professor with the Department of Electrical Engineering, University of Oviedo. Since 2007 he has been working in University of Oviedo at full time.

His research interests are focused on multiple ports power supply systems, bidirectional DC-DC power converters and wide band gap semiconductors.

Diego G. Lamar (M'08) was born in Zaragoza, Spain, in 1974. He received the M.Sc. degree, and the Ph.D. degree in Electrical Engineering from the University of Oviedo, Spain, in 2003 and 2008, respectively.

In 2003 and 2005 he became a Research Engineer and an Assistant Professor respectively at the University of Oviedo. Since September 2011, he has been an Associate Professor.

His research interests are focused in switching-mode power supplies, converter modelling, and power-factor-correction converters.

Marcos Fernández Díaz (S'11) was born in Avilés, Spain, in 1986. He obtained the degree in Telecomunications Engineering in 2011 in the University of Oviedo, Gijón, Spain.

He has been working in the Department of Electrical and Electronical Engineering, Computers and Systems, University of Oviedo, for the Power Supply System Group since 2011. His research interests include power factor corrector ac-dc converters for LED lighting.
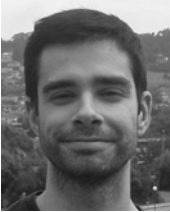
Manuel Arias Pérez de Azpeitia (M'10) was born in Oviedo, Spain, in 1980. He received the M. Sc. degree in electrical engineering from the University of Oviedo, Spain, in 2005 and the Ph. D. degree from the same university in 2010.

Since February 2007 until June 2011, he was an Assistant Professor of the Department of Electrical and Electronic Engineering, University of Oviedo. Since June 2011, he has been a researcher of Sistemas Electrónicos de Alimentación Group. His research interests include ac-dc and dc-dc converters, UPS and LED-based lighting.

Marta M. Hernando (M'94-SM'11) was born in Gijón, Spain, in 1964. She received the M.S. and Ph.D. degrees in electrical engineering from the University of Oviedo, Gijón, Spain, in 1988 and 1992, respectively. She is currently a Professor at the University of Oviedo. Her main interests include switching-mode power supplies and high-power factor rectifiers.

Javier Sebastián (M'87-SM'11) as born in Madrid, Spain, in 1958. He received the M.Sc. degree from the Polytechnic University of Madrid, and the Ph.D. degree from the University of Oviedo, Spain, in 1981 and 1985, respectively. He was an Assistant Professor and an Associate Professor at both the Polytechnic University of Madrid and at the University of Oviedo, in Spain. Since 1992, he has been with the University of Oviedo, where he is currently a Professor. His research interests are switching-mode power supplies, modelling of dc-to-dc converters, low output voltage dc-to-dc converters, high power factor rectifiers, dc-to-dc converters for envelope tracking techniques and the use of wide bandgap semiconductors in power supplies..