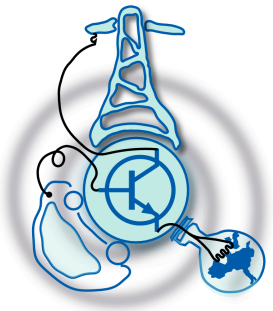
# Hybrid Reactive Power Compensation System for Low Voltage Applications

by

UMER MUSHTAQ



Submitted to the Department of Electrical Engineering, Electronics, Computers and Systems
in partial fulfillment of the requirements for the degree of

Erasmus Mundus Master Course in Sustainable Transportation and Electrical Power Systems

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Author .....

Certified by .....
JOSE MANUEL CANO RODRIGUEZ
Associate Professor
Thesis Supervisor

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## Abstract

This Master thesis presents a three phase hybrid STATCOM (Static synchronous compensator) that provide reactive power (*var*) for power factor correction in low voltage distribution system. The system consist of capacitor banks and an inverter, based on a voltage sourced inverter (VSI) configuration, which allows the reactive current injection in leading and lagging to the utility voltage. This system also have master controller that controls the reactive power reference of inverter and switching of power capacitors with capability to reduce capacitors switching events to increase the life of power components.
The system used phase lock loop (PLL) to synchronization with grid even with significant voltage harmonics. Vector control method is used to generate direct and quadrature components of the grid voltage in a simple and computationally efficient manner in order to generate a synchronized reference signal for the current control loop. The main goal of this project is to study and implement the control system of a grid-tied inverter with LCL filter and its performance with capacitor switching. The objectives of the project are divided in three parts: theoretical, simulation study and experimental work. The theoretical part discuss the harmonics mitigation, inverter topology and control, filter topology and the performance of overall system. Simulation is performed on Matlab/Simulink platform, for experimental verification a prototype is also developed in the lab to prove the effectiveness of the designed filter, controllers and grid synchronization method. The Opal RT-lab hardware in the loop (HIL) is used for hardware testing, which provides a good solution for analysis of design and laboratory prototype implementation.

Thesis Supervisor: JOSE MANUEL CANO RODRIGUEZ
Title: Associate Professor

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I would never forget to pay gratitude to my professors from ISEC Coimbra and University of Nottingham for providing me basics and advance knowledge to develop this research.

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# Glossary

| | |
|---|---|
| **VSI** | Voltage source inverter. |
| **PLL** | Phase lock loop. |
| **STATCOM** | Static synchronous compensator. |
| **HIL** | Hardware in the loop. |
| **PI** | Proportional and integral. |
| **PWM** | Pulse width modulation. |
| **DSOGI** | Dual second order generalized integrator. |
| **QSG** | Quadrature signal generator. |
| **PSC** | Positive sequence calculator. |
| **ISC** | Instantaneous symmetrical components. |
| **IGBT** | Insulated gate bipolar transistor . |
| **SVPWM** | Space vector PWM. |
| **LCL** | Inductor capacitor inductor. |
| **THD** | Total harmonic distortion. |
| **PCB** | Printed circuit board. |
| **ADC** | Analogue to digital converter. |
| **LEMUR** | Laboratory for enhanced microgrid unbalance Research. |
| **TCP/IP** | Transmission control protocol/Internet protocol. |
| **FPGA** | Field-programmable gate array. |
| $\boldsymbol{T_s}$ | Sampling time. |
| $\boldsymbol{T_{sw}}$ | Switching time. |
| $\boldsymbol{P}$ | Active power. |
| $\boldsymbol{Q}$ | Reactive power. |
| $\boldsymbol{V_g}$ | Grid voltage. |
| $\boldsymbol{f_g}$ | Grid frequency. |
| $\boldsymbol{f_{sw}}$ | Switching frequency. |
| $\boldsymbol{P_n}$ | Rated power. |
| $\boldsymbol{V_{dc}}$ | DC bus voltage. |
| $\boldsymbol{L_1}$ | Inverter inductor. |
| $\boldsymbol{L_2}$ | Grid inductor. |
| $\boldsymbol{C_f}$ | Filter capacitor. |

# Chapter 1

# Introduction

## 1.1 Objective

This thesis deals with design and implementation of hybrid STATCOM (Static synchronous compensator), which is connected to low voltage distribution grid to provide reactive power and compensate for low power factor on customer side. The hybrid STATCOM consist of a voltage source inverter(VSI) of power rating $5kvar$ and capacitor banks, both are controlled by master reactive power controller. This controller decides the source of reactive power compensation. As VSI is capable to provide $5kvar$ both leading and lagging reactive power, therefore master controller can reduce the switching of capacitor banks by fine reactive power control in both direction from VSI.

The main focus of this thesis is to implement harmonic filter for inverter and study grid synchronized inverter operation with capacitor switching.

## 1.2 Motivation

In most of buildings and industries heavy electrical load (pumps and fans) and electronic devices are connected at low voltage distribution network, the reactive power demand of these loads is very high which reduce the overall power factor of facility. Therefore, utility grid companies impose penalties for low power factor customers,

that increase the cost of energy.

The situation become worst when these loads overload the low voltage distribution cables (during starting) and cause extensive voltage drop in power network, most of cases voltage sensitive electrical appliances are connected close to heavy electrical loads. Therefore hybrid STATCOM is offered to provide cheap and easy implementable solution. It minimize the power factor penalties and also control voltage dip in low voltage network. The hybrid STATCOM concept investigated in this project consist of an inverter and capacitor banks (see Fig.1-1) which provide power factor compensation and voltage dip due to switching of heavy loads is compensated by fast injection of reactive current by STATCOM inverter.

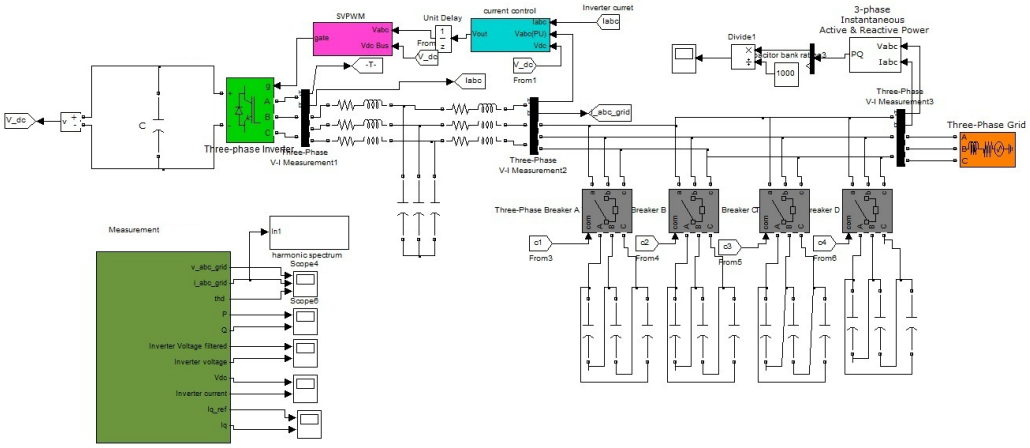



Figure 1-1: Schematic diagram of STATCOM.

## 1.3 Literature review

This section presents the literature review of the inverter control and grid synchronization techniques.

### 1.3.1 Inverter control

The control of stand alone inverter is mainly consist of two current control loops, one is a fast control loop which control current dynamics, active and reactive current with feed-forward components while other slow current control loop maintain constant DC

bus voltage. The fast current control loop is responsible for current protection, power quality, current harmonics control and dynamic performance of the inverter. The DC voltage controller is designed to balance the power flow between grid and inverter. Following are different techniques to implement VSI control with respect to different reference frames[9].

### Synchronous reference frame

Synchronous reference control also called *dq* control use *abc* to *dq* transformation(A.1.1). The sinusoidal signals, i.e grid currents and voltages are converted into DC values for easy filtering and control by transforming them in to the reference frame that is synchronized with grid voltage. The schematic of *dq* control is shown in Fig.(1-2). The DC bus voltage is controlled by adjusting $i_d$ current that depends on the active

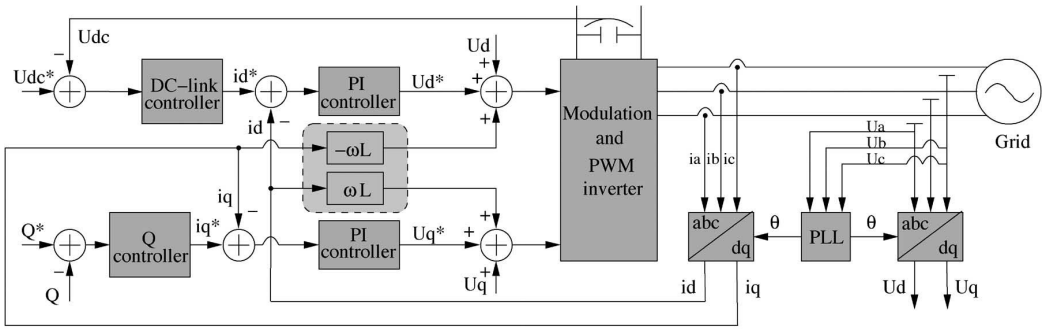



Figure 1-2: Structure of synchronous rotating frame control.
[25]

power exchange in the system. The reference for active power is usually set to zero, if active power is not required. If reactive power has to be controlled the reactive power reference is given to $Q$ controller to generate reference $i_q$ current.

The control system has three PI controllers, one for DC link voltage control , two for $i_q$ current control and $i_d$ current control. The gains of PI controllers are calculated according to the required dynamics performance of inverter.

The phase angle needed by *abc* to *dq* transformation block is extracted from grid voltage, as output voltage need to be in phase with grid voltage. There are different techniques to extract the grid voltage phase angle, arctangent function or phase lock

loop(PLL). However, the voltage feed-forward and cross coupling terms are used to improve the response of the PI controller[25].

### Stationary reference frame

In stationary reference frame currents and voltages are transformed into stationary reference frame using *abc* to $\alpha\beta$ transformation (A.1.3) as shown in Fig.(1-3). In this control scheme the transformed currents are not constant they are sinusoidal, therefore it is hard to remove steady state error from the system using simple PI controllers. Therefore, a proportional resonant controller is implemented to control grid tied inverter. The advantage of this controller is that it can achieve very high gain around the resonant frequency and is able to remove steady state error between the controlled and reference signals[4]. In theory infinite gain can be achieved at resonance frequency but practically this is not feasible, therefore predictive model resonant controller is used. However, the performance of a PR controller is not good for variable frequency operations for inverters connected to weak grids[27].

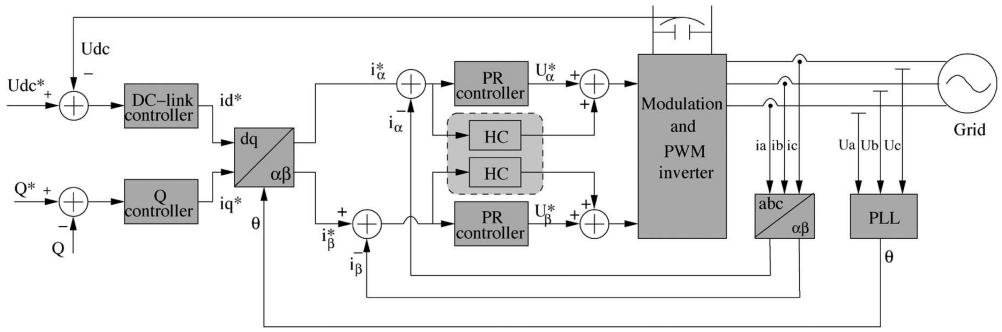



Figure 1-3: Structure for Stationary rotating frame control.
[25]

### Natural reference frame

Natural reference frame control also called *abc* control use individual controller for every phase current, however the configuration of the controller varies with different three phase circuit configuration. If the system has 3 wire connection (it is isolated from the neutral conductor) only two controllers are required as the third current is

derive from other two currents using Kirchoff's current law[9]. The controllers implemented in such control are dead-beat or hysteresis type.

In *abc* control scheme, the controllers are non-linear and have fast dynamic performance. The hysteresis type control is very famous in *abc* control scheme, because it is easy to implement and offers fast transient response, limit peak currents and it is insensitive to DC bus ripples that leads to low filter capacitors. However, this controller generate variable switching frequency for PWM within the given band that produce non-optimized current ripples. Moreover, the dead beat controller has bandwidth limitations due to plant delays[21].

In natural reference frame control scheme, DC link controller and $Q$ controller gives

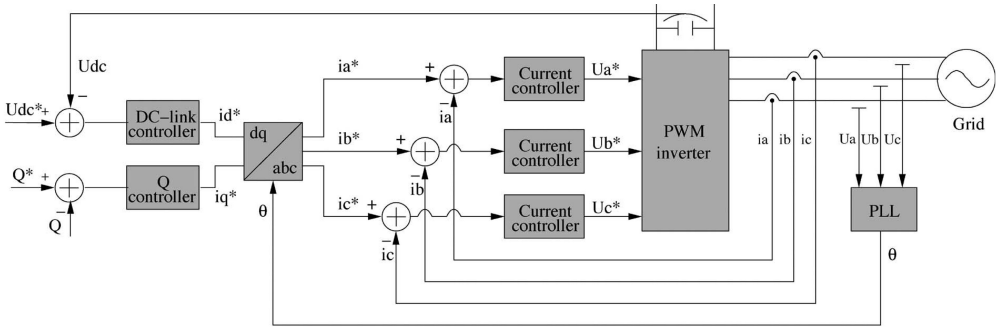



Figure 1-4: Structure for Natural reference frame control.
[25]

$I_d$ and $I_q$ reference currents respectively. These reference currents are transformed into sinusoidal reference currents using *dq* to *abc* (A.1.2) and grid voltage angle from PLL. Each of these current reference is compared with the measured current and the error is feed to the corresponding current controller. The current controllers output is feed to a variable switching frequency PWM generation block to control transistors as shown in Fig.(1-4).

Modulation is not required if dead-beat or hysteresis control is employed in current controllers, modulation is only required to generate duty cycle, if PR or PI controllers are employed in control.

### 1.3.2 Thesis scope

The research work done to support this thesis is to design and implement a hybrid STATCOM for low voltage application. Following are the main attributes of this thesis:

1. Design of a reactive power controller, which minimize the switching events of capacitor bank contactors and generate reactive power reference for the inverter. The controller is designed to compensate power factor grid codes.
2. Comprehensive LCL filter design procedure for grid connected inverter.
3. The system dynamic and steady state stability is studied.
4. Design and hardware implementation of current and voltage sensors for low voltage application.
5. Analysis and design of current controllers for grid connected inverter. Verify the required dynamic response of inverter with current THDs according to IEEE standard.
6. Study of applicability of RT-Lab platform and verify the design through real time simulation with laboratory prototype.

### 1.3.3 Project outline

This thesis is structured in six chapters:
Chapter 1: Describes the motivation, backgrounds and goals of this thesis.
Chapter 2: Deals with the design of STATCOM, theoretical and mathematical analysis of the inverter control and LCL filter parameter is conducted.
Chapter 3: Presents the MATLAB Simulation studies of STATCOM with different operation scenarios and test results.
Chapter 4: Gives detailed information about the hardware used in testing and verification proposed design.

Chapter 5: Explains hardware result and compare them with simulation results.

Chapter 6: Conclude the project with future work scope.

# Chapter 2

# Mathematical and Engineering Analysis of STATCOM

## 2.1 Introduction

This chapter presents reactive power control of STATCOM, grid synchronization, PLL, Design of LCL filter, design of inverter control and inverter switching techniques. The schematic diagram of the inverter system is shown in Fig.(2-1). Grid voltage is

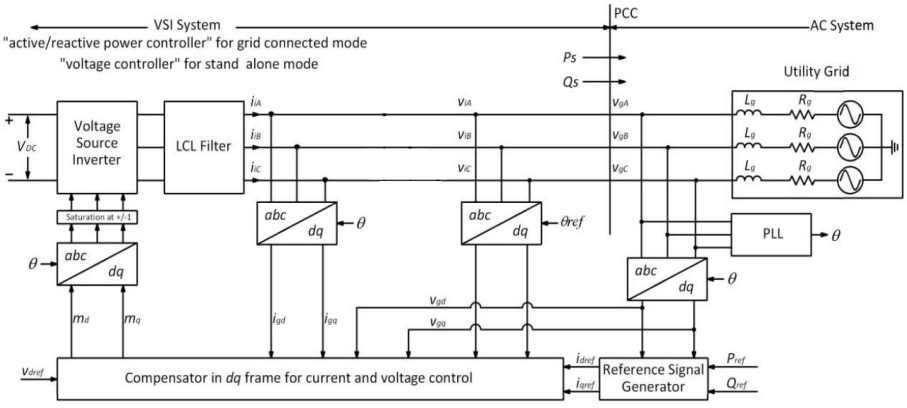



Figure 2-1: Schematic of grid tied inverter with LCL filter[25].

sensed and used by the PLL block to estimate the grid angle, which is required for grid synchronization of the inverter. The inverter currents are transformed into $dq$ reference frame(A.1.1) and these currents are oriented along the $V_d$ component of

grid voltage, that the reason this control is called voltage oriented control. Grid frequency and voltage is needed to control the inverter dynamics. The grid voltage is also transformed into $dq$ reference frame(A.1.1) to be added in the control loop as feed-forward term. The reactive and active power reference generate the $I_d$ and $I_q$ reference current by putting $V_d$ and $V_q$ in equation 3.1 and 3.2. The inverter control generate the reference voltage signal in synchronous reference frame and feed into PWM generator block after transformation from $dq$ to $abc$ using the same grid angle(A.1.2). This block calculates the required switching states to generate the desire output inverter voltage.

## 2.2 PLL and grid synchronization

Phase Lock Loop (PLL) is defined as the internally generated signal that is programmed to track the external signal and keep in synchronism. PLL is used in many application like electrical motors, radio, telecommunication and power electronics applications. PLL system can work with wide rage of frequency spectrum, from few hertz to gigahertz. There are mainly three types of PLL. (i) stationary reference frame (ii) zero crossing (iii) synchronous rotating reference frame. In grid voltage application synchronous rotating reference frame PLL is most commonly used.

### 2.2.1 Phase Lock Loop (PLL)

The PLL configuration is shown in Fig.(2-2). The phase voltages are sensed using grid voltage sensors. These sinusoidal voltages are transformed to $V_\alpha$ and $V_\beta$ voltage using $\alpha\beta$ transformation(A.1.3). These voltage then further transformed into the $dq$ reference frame the angle used in these transformations is calculated by integrating a frequency signal and the initial value of the angle should be carefully selected in initial condition of integrator. The next input to the PLL is the fundamental frequency of grid, If this frequency is set properly, the voltages $V_d$ and $V_q$ appears as DC values with some fluctuation due to grid harmonics.

The transformation of a sinusoidal signal into DC value ($dq$ reference frame) decreases

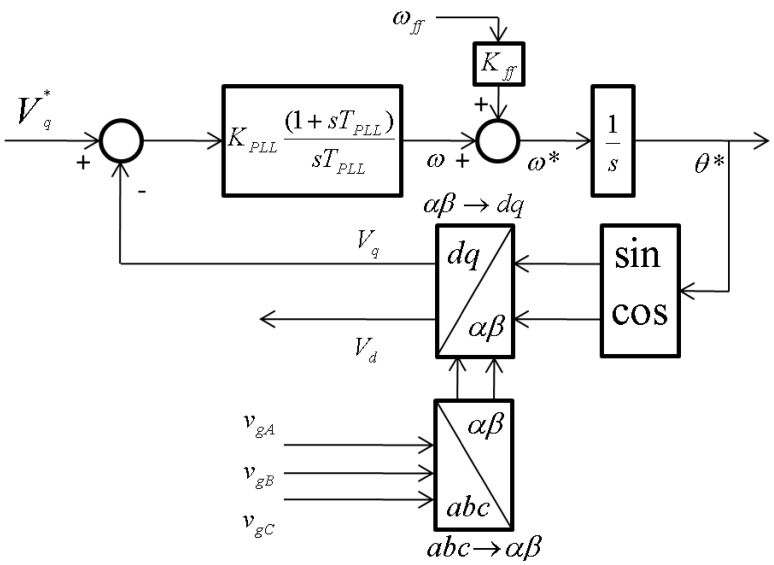



Figure 2-2: Schematic of phase lock loop[25].

the complexity of the control. However, input signals are in time domain therefore, removing the steady state error required specially tuned PI controller[3].

### 2.2.2 Phase deviation

Phase deviation is the problem in using simple PLL scheme described above. Normally the grid frequency is constant and phase error is zero but in the case of frequency variation phase error tends to increase and the PI regulator brings the phase error to the zero. The $w_{ff}$ term fed through $K_{ff}$ facilitates it in large extend. If the frequency variation is not predictable then additional integral term may be use to within the PI controller to achieve desire response from PLL[10].

### 2.2.3 Positive sequence detection and grid synchronization

In AC power systems applications, the grid voltage is not pure fundamental waveform as expected. It contains harmonics and unbalance. Which produce negative sequence component that rotate in the opposite direction to the positive sequence component. Therefore, the applications that required synchronization to the grid, must have a system to reject negative sequence component of grid voltage and detect

only positive sequence component. Many algorithms are proposed to detect positive sequence component of grid voltage, Which work on different mathematical models. Fortescue presented symmetrical component method in 1918. which use frequency domain approach. Most of positive sequence detection algorithms are based on this method. However, there are algorithm that use voltage peak detection or time domain adjustment of the Fortescue decomposition. If algorithm is derived assuming purely sinusoidal voltages, do not work properly if grid voltage has harmonics. Some techniques also propose filtering the measured voltages in order to identify the fundamental component and then, calculate the positive sequence[20], but in case real time application filtering delay cause a problem in grid synchronism[25].

In grid synchronization positive sequence component detection is very important in case of distorted and unbalance grid. The fast detection of this component under grid fault is important for power exchange and prevent inverter protection from tripping. The well know technique used to detect positive sequence component use dual second order generalized integrator (DSOGI) to implement quadrature signal generator(QSG)[20]. The scheme shown in Fig.2-3 present a new frequency-adaptive

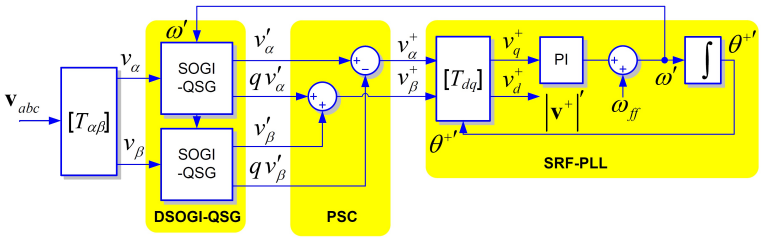



Figure 2-3: Improved dual SOGI-PLL for positive sequence detection[20].

positive sequence detection technique, called the Dual Second Order Generalized Integrator PLL (DSOGI-PLL). This technique convert the three phase voltage from the *abc* to $\alpha\beta$ reference frame. The 90 degree shift version of $\alpha\beta$ voltages is obtain by dual SOGI based quadrature signals generator (QSG). These signals act as inputs to the positive sequence calculator (PSC) which lies on the instantaneous symmetrical components (ISC) method on the $\alpha\beta$ domain. At the end positive-sequence $\alpha\beta$ voltages are transform to the *dq* synchronous reference frame and a PLL (SRF-PLL) is

employed to make the system frequency adaptive. To get precise result under grid frequency variations the close-loop system is implemented which allows proper adaptation of the DSOGI-QSG resonance frequency to the actual network frequency as shown in Fig.2-3. The SOGI is the important block of the QSG and block harmonics of the grid and make system more robust. The ISC method on the $\alpha\beta$ reference frame provides an effective mechanism to easily calculate the positive sequence voltage component. The combine action of these techniques converts the DSOGI-PLL to a high performance detection system which allows fast and precise detection of the positive-sequence voltage component even under distorted grid conditions[20].

### 2.2.4 Transfer function of PLL

As the PLL system is working with sampled data therefore, the sampling delay should be considered. The transfer function of PLL shown in Fig2-2 is a integral element and time lag.

$$G_{plant} = (\frac{1}{1+sT_s})(\frac{1}{s}) \tag{2.1}$$

In equation 2.1 $T_s$ is the sampling time. The overall open loop transfer function of system is:

$$G_{ol} = (K_{PLL}\frac{1+sT_{PLL}}{sT_{PLL}})(\frac{1}{1+sT_s})(\frac{V_m}{s}) \tag{2.2}$$

Therefore the close loop transfer function become:

$$G_{cl} = \frac{G_{ol}}{1+G_{ol}} \tag{2.3}$$

## 2.3 Pulse Width Modulation(PWM)

### 2.3.1 Principle of Space Vector PWM (SVPWM)

The schematic of a three phase voltage source PWM inverter is shown in Fig.2-4. S1 to S6 are the six power IGBTs that generate the output voltage, which are controlled by the switching signals a, a', b, b', c and c'. When an upper IGBT is switched ON

the lower IGBT in same arm is switched OFF to prevent short circuit. Therefore, only three IGBTs states are required to determine the switching states i.e S1, S3 and S5[14].

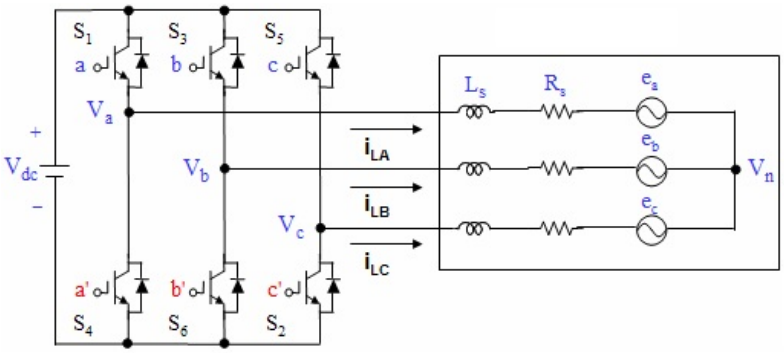



Figure 2-4: Three-phase voltage source PWM Inverter.

The relationship between the line to line voltage vector $[Vab \quad Vbc \quad Vca]^t$ and switching variable vector $[a, b, c]^t$ is shown below.

$$\begin{bmatrix} V_{ab} \\ V_{bc} \\ V_{ca} \end{bmatrix} = V_{dc} \begin{bmatrix} 1 & -1 & 0 \\ 0 & 1 & -1 \\ -1 & 0 & 1 \end{bmatrix} \begin{bmatrix} a \\ b \\ c \end{bmatrix} \tag{2.4}$$

The relationship between the phase voltage vector $[Va \quad Vb \quad Vc]^t$ and switching variable vector $[a, b, c]^t$ is shown below.

$$\begin{bmatrix} V_{an} \\ V_{bn} \\ V_{cn} \end{bmatrix} = \frac{V_{dc}}{3} \begin{bmatrix} 2 & -1 & -1 \\ -1 & 1 & -1 \\ -1 & -1 & 2 \end{bmatrix} \begin{bmatrix} a \\ b \\ c \end{bmatrix} \tag{2.5}$$

As show in Fig.2-4, there are eight possible combinations of "ON" and "OFF" patterns for six IGBTs. The ON and OFF states of the lower IGBT are complementary to the upper one, therefore once the states of the upper IGBTs are determined according to equation 2.5 lower IGBTS position can be determined.

The eight switching vectors, output phase voltage and output line to line voltages in

terms of DC-link VDC are given in Table.2.1 and the eight inverter voltage vectors (V0 to V7) are show in Fig.2-5

Table 2.1: Switching table

| Voltage Vectors | Switching Vectors | | | Line to neutral voltage | | | Line to line voltage | | |
|---|---|---|---|---|---|---|---|---|---|
| | a | b | c | $V_{an}$ | $V_{bn}$ | $V_{cn}$ | $V_{ab}$ | $V_{bc}$ | $V_{ca}$ |
| $V_0$ | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| $V_1$ | 1 | 0 | 0 | 2/3 | -1/3 | -1/3 | 1 | 0 | -1 |
| $V_2$ | 1 | 1 | 0 | 1/3 | 1/3 | -2/3 | 0 | 1 | -1 |
| $V_3$ | 0 | 1 | 0 | -1/3 | 2/3 | -1/3 | -1 | 1 | 0 |
| $V_4$ | 0 | 1 | 1 | -2/3 | 1/3 | 1/3 | -1 | 0 | 1 |
| $V_5$ | 0 | 0 | 1 | -1/3 | -1/3 | 2/3 | 0 | -1 | 1 |
| $V_6$ | 1 | 0 | 1 | 1/3 | -2/3 | 1/3 | 1 | -1 | 0 |
| $V_7$ | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |

The SVPWM is the special transistor switching technique used in the phase inverters, it give better utilization of DC bus voltage and produce less harmonics in current and voltage. The modulation limit for sine PWM is $\frac{1}{2}V_{dc}$, while SVPWM reference voltage can be reach up to $\frac{1}{\sqrt{3}}V_{dc}$ shown in Fig.2-6. In space vector PWM, the sinusoidal voltages in the *abc* reference frame are transformed into the stationary *dq* reference frame, which contain two components one along horizontal (d) axis and other along vertical (q) axes. This transformation is equivalent to an orthogonal projection of $[a, b, c]^t$ onto the two-dimensional perpendicular to the vector $[1, 1, 1]^t$(the equivalent d-q plane) in a three-dimensional coordinate system. Therefore, two zero vectors and six non zero vectors are possible.

The six non-zero vectors (V1 - V6) shape the axes of a hexagonal as shown in Fig.2-7, and switch the transistor to produce three phase voltage. The angle between any adjacent two non-zero vectors is 60 degrees. However, two zero vectors (V0 and V7)

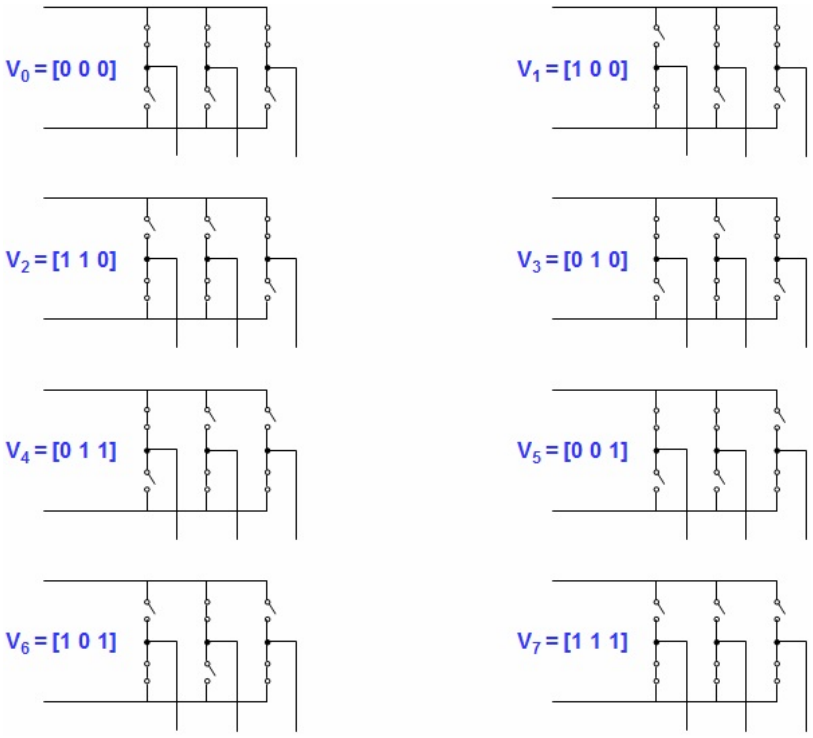



Figure 2-5: Inverter voltage vectors

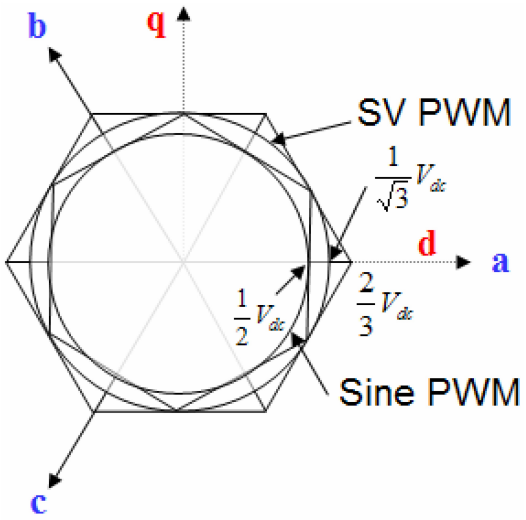



Figure 2-6: Comparison of modulation index in Sine PWM and SVPWM.

are at the origin and apply zero voltage. The eight vectors are the basic space vectors and are denoted by V0, V1, V2, V3, V4 V5, V6, and V7. The same transformation can be applied to the desired output voltage to get the required reference voltage vector $V_{ref}$ in the $dq$ plane[14].

The space vector PWM use eight switching vector to approximate the reference

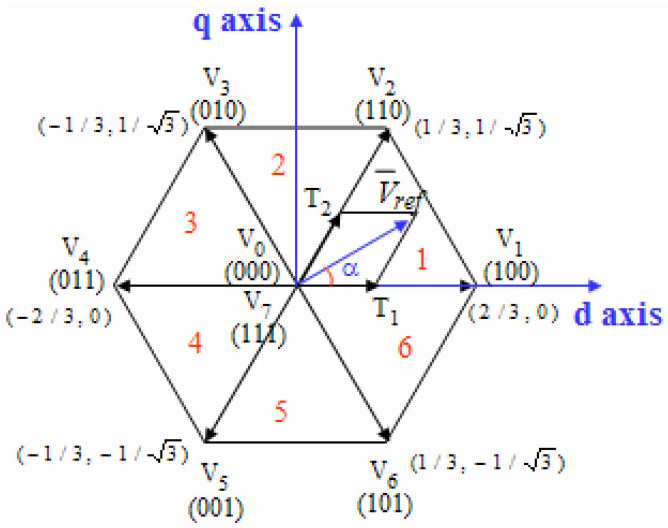



Figure 2-7: SVPWM switching vectors and sectors.

voltage vector $V_{ref}$. One simple method of approximation is to generate the average output of the inverter in a small period, T to be the same as that of $V_{ref}$ in the same period. Therefore, space vector PWM can be implemented by the following steps:[14]

Step 1. Determine $V_{ref}$ , $V_q$, $V_d$, and angle $\alpha$

Step 2. Determine time duration $T_2$, $T_1$, $T_0$

Step 3. Determine the switching time of each transistor (S1 to S6)

## 2.4 Control of VSI

There are two different approaches used to control the VSI. The voltage control and current control. Voltage control is very simple technique mostly utilized in high voltage application i.e FACTS. In this technique the $P$ and $Q$ are directly controlled through the inverter voltage magnitude and phase angle with respect to grid voltage. However, a second technique that involves inverter current sensing is move complex, but provides inverter current protection in case of grid fault.

### 2.4.1 VSI current control

The VSI current control is implemented in synchronous reference, ss this technique provide decoupled control of active and reactive power, moreover all control parameters are DC values that makes PI controller design very easy. In this control technique VSI AC side currents are sensed and controlled by implementing PI controllers. The phase angle and the amplitude of the VSI line current with respect to the phase voltage is used to control real and reactive power of the inverter. As inverter current is continuously sensed and controlled therefore, the VSI is protected from overloading and this technique also shows robustness to variation in grid parameters. If grid voltage varies the VSI current is adjusted accordingly, to get desired reactive and active power from the VSI.

Current control in a two signal reference frame, $\alpha\beta$ or $dq$, reduce the complexity of controller. The number of plants are reduced from three to two and decoupled control of active and reactive power is possible. However, $dq$ reference frame control gives further advantages, as all control variables are DC quantities at steady state condition, which make the PI controller design pretty easier. As shown in Fig.1-2,the $P$ and $Q$ are controlled by grid current $i_d$ and $i_q$ respectively.

### 2.4.2 PI current controller

Proportional and integral(PI) controller is the most common controller used in industrial applications. The block diagram of a PI controller is shown in Fig.2-8

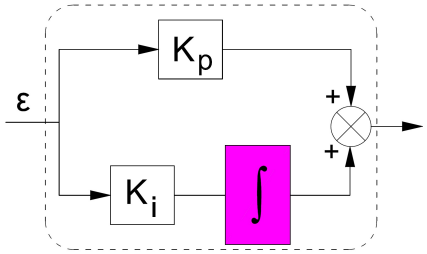



Figure 2-8: Block diagram of PI regulator.

The transfer function of PI controller is depicted in equation 2.6.

$$G_{PI}(s) = K_p + \frac{K_i}{s} \tag{2.6}$$

The design of the PI controller in $dq$ reference frame, both currents have the same dynamic therefore, PI controller parameter tuning is done only for $d$ current and the same parameters are used for $q$ current PI controller. While designing current control loop controller parameter (Fig.2-9) voltage feed-forward and decoupling terms are consider as disturbance therefore, they are neglected in controller design.

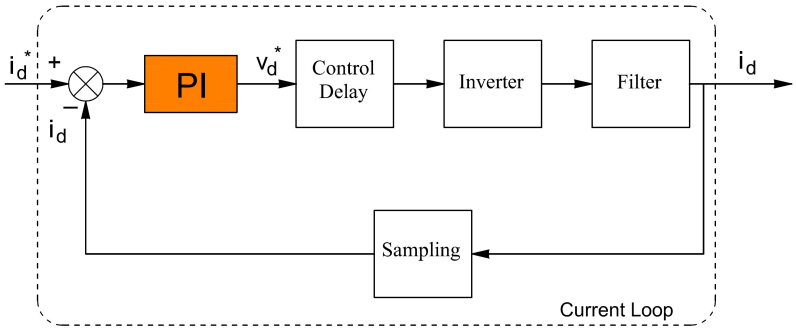



Figure 2-9: PI current controller block diagram.

For digital system the controller diagram is re-draw in Fig.2-10.

Fig.2-10 includes following functions:

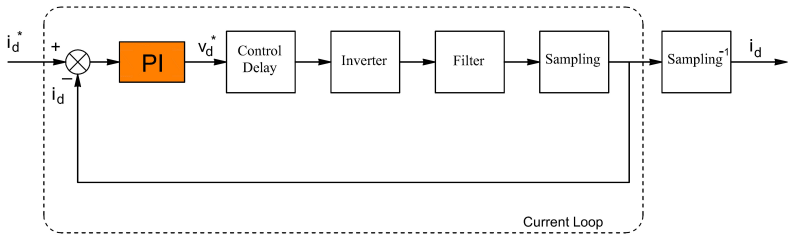



Figure 2-10: PI current controller block diagram with sampling block.

∗ Transfer function of PI controller

$$G_{PI}(s) = K_p + \frac{K_i}{s} \tag{2.7}$$

* Transfer function control delay.

$$G_{control}(s) = \frac{1}{1 + sT_s} \tag{2.8}$$

where $f_s = 10kHz$ and $T_s = \frac{1}{f_s}$

* Transfer function of inverter.

$$G_{inverter}(s) = \frac{1}{1 + s.0.5T_{sw}} \tag{2.9}$$

where $f_{sw} = 10kHz$, (nominal switching of inverter) and $T_{sw} = \frac{1}{f_{sw}}$

* In simulation LCL filter (see Fig.2-15) is used but for simplicity of control design, capacitor is neglected and only filters inductances and their parasitic resistances are considered.

$$G_{filter}(s) = \frac{1}{Ls + R} \tag{2.10}$$

Where $L = L_i + L_g$ and $R = R_i + R_g$

* Transfer function of sampling block.

$$G_{sampling} = \frac{1}{1 + s.0.5T_s} \tag{2.11}$$

The overall transfer function of current loop is :

$$G_{crt} = G_{PI}.G_{control}.G_{inverter}.G_{filter}.G_{sampling} \tag{2.12}$$

Using equation. 2.7, 2.8, 2.9, 2.10 and 2.11 the transfer function become:

$$G_{crt} = \frac{K_{Pcrt}s + K_{icrt}}{s} \frac{1}{1 + sT_{\sum 1}} \frac{K_e}{sT_e + 1} \tag{2.13}$$

where $T_e = \frac{L}{R}$ , $K_e = \frac{1}{R}$ and $T_{\sum 1} = T_s + 0.5T_{sw} + 0.5T_s$.
After optimizing the equation 2.13.

$$G_{crt} = \frac{1}{2sT_{\sum 1}(1 + sT_{\sum 1})} \tag{2.14}$$

After comparing the equation 2.13 and 2.14 PI controller constants are

$$K_{pcrt} = \frac{T_e}{2K_e T_{\sum 1}} = 15 \tag{2.15}$$

$$K_{icrt} = \frac{K_{pcrt}}{T_e} = 250 \tag{2.16}$$

The values calculated in equation 2.15 and 2.16 are used to optimize the controller parameters using Sisotool, MATLAB toolbox. The following are the controller design requirement imposed:[25]

∗ The minimum band with of control is $500Hz$ to get good transient response of the inverter current control.

∗ The current loop with gain margin larger than $6dB$ and phase margin larger than 45°.

The proportionality gain is selected in such away that dominant poles have damping factor higher the 0.8. The Bode plot and zero pole map of open loop current control transfer function is generated using design parameters from table.2.2. The plot is shown in Fig.2-11.

It is also shown in Fig.2-11 that gain margin is $13.5dB$ and phase margin is 57.3°

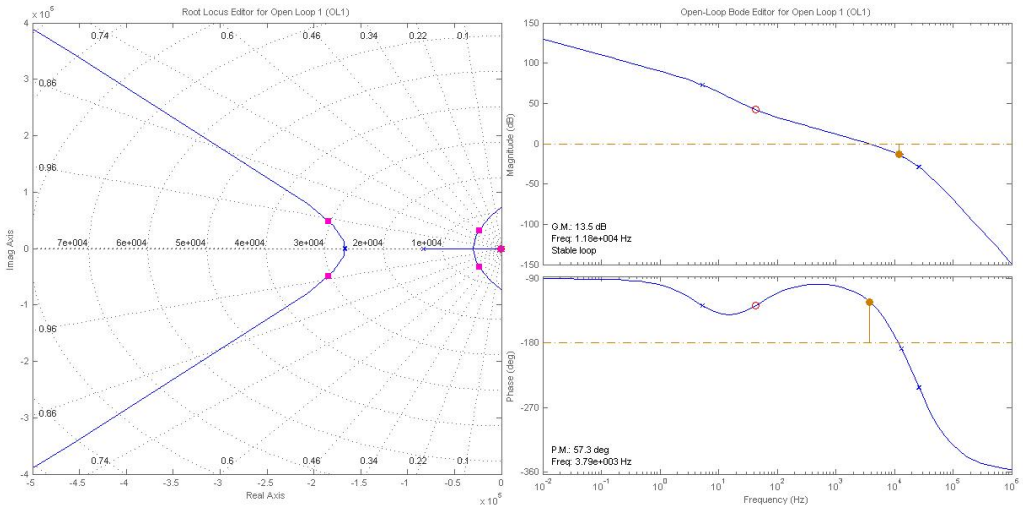



Figure 2-11: Bode plot and zero pole map open loop current control.

and control loop is stable.

The step response of controller is depicted in Fig.2-12 with settling time $0.001s$.

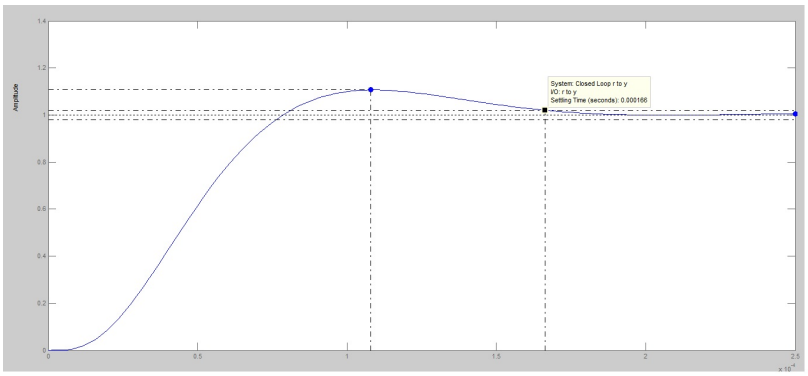



Figure 2-12: Step response of system.

### 2.4.3 DC bus voltage controller

The DC link voltage control is achieve by controlling the active power exchange between the grid and the inverter. The voltage control loop is the outer current loop and slower than inner current loop by 5 to 20 times and both loop are consider as decoupled and while designing the voltage loop controller the actual grid current can be consider equal to reference current. The bock diagram of control loop is shown in Fig. 2-13.

The value of DC link capacitor is $1100uF$. According to optimum symmetrical

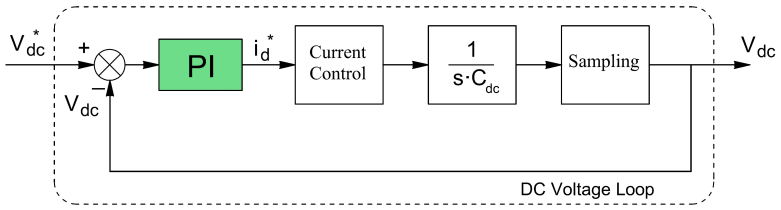



Figure 2-13: DC voltage loop block diagram.

method[15] first phase margin 45° is impose to calculate the PI controller parameters.

$$a = \frac{1 + cos\psi}{sin\psi} \tag{2.17}$$

MATLAB Sisotool block is used to perform the discrete analysis. The settling time of $0.05s$, $K_p = 1.7$ proportional gain, gain margin $18.5dB$ and phase margin of $59°$ is obtain as shown in Fig. 2-14.

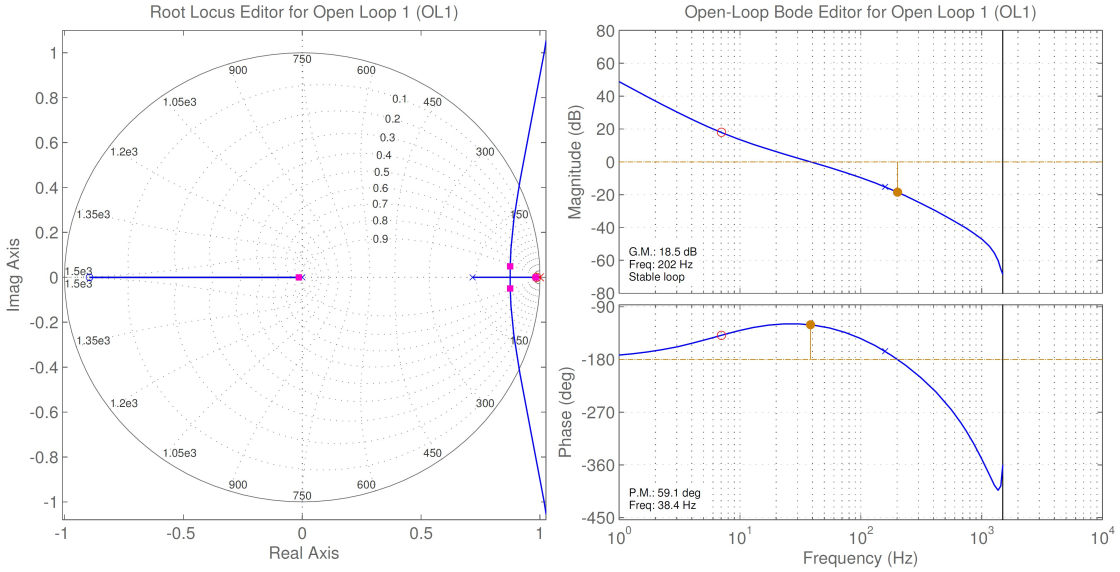



Figure 2-14: Bode plot and zero pole map of open loop voltage control

## 2.5 LCL filter design and modeling

Grid connected inverters produce harmonics in output current due to switching, therefore to limit these harmonics according to international industrial standards harmonic damping filters are connected after inverters. Single inductor filter was used in past electronic applications, but this technique increase the size and cost of the system. Therefore, in modern inverter application which operate at higher switching frequency, LCL filters are introduced that reduce the size and cost of the filtering unit and provide suitable harmonics damping. The most important constraints in designing the LCL filters are, switching ripples and reactive power variation seen by grid due to capacitor of LCL filter. All these constraints are precisely design to fulfill system required specification and stable inverter operation.

The LCL filter per-phase model is shown in Fig.2-15. Where $L_1$ is the inverter side

inductance, $L_2$ is the grid side inductance, $C_f$ is the filter capacitor, $R_f$ is the damping resistance, $R_1$ and $R_2$ are inductor stray resistances. The $i_c$, $i_g$ and $i_i$ are capacitor, inverter and grid currents respectively.

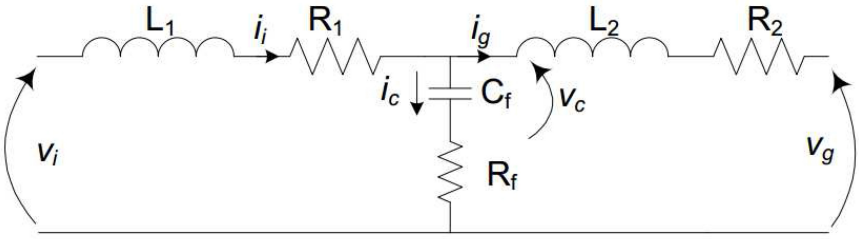



Figure 2-15: Per phase model of the LCL filter.

### 2.5.1 Transfer function of the LCL filter

The transfer function of the LCL filter is derived from the differential equations of model shown in Fig.2-15, while inductor resistances are neglected as these resistance increase the stability of the filter. The transfer function $H_{LCL} = \frac{i_g}{v_i}$ is written considering the grid voltage as ideal source and for harmonic analysis it is considered as short-circuit and for filter analysis it is considered to be zero. The transfer function of the LCL filter without damping is:

$$H_{LCL}(s) = \frac{1}{L_1 C_f L_2 s^3 + (L_1 + L_2)s} \tag{2.18}$$

Transfer function with damping resistor $R_f$.

$$H_{LCL}(s) = \frac{C_f R_f s + 1}{L_1 C_f L_2 s^3 + C_f (L_1 + L_2) R_f s^2 + (L_1 + L_2)s} \tag{2.19}$$

### 2.5.2 LCL filter design

The step by step approach of LCL filter design procedure is presented in this section. The resonance frequency selection and grid inductance variation are most important parameters while designing the LCL filter because the variation in these parameters can make the system unstable.

Following are the parameters required for the filter design, grid rated line to line rms voltage $V_{LL}$, inverter power rating $P_n$, Grid frequency $f_g$, inverter DC bus voltage $V_{DC}$ and switching frequency $f_{sw}$. The LCL filter design algorithm is shown in Fig.2-16.

Filter inductance and capacitor values are referred as the percentage of base values,

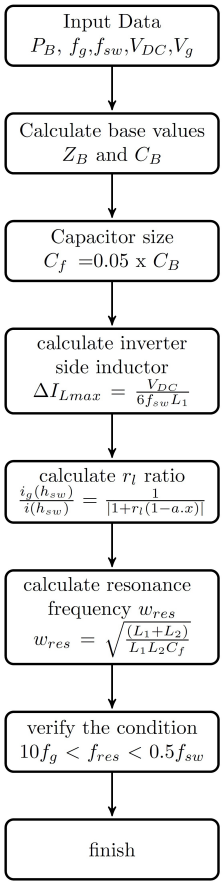



Figure 2-16: LCL filter design algorithm [18], [22] & [19].

therefore base value for impedance $Z_b$ and capacitance $C_b$ can be calculated using equation 2.20 and 2.21.

$$Z_b = \frac{V_{LL}^2}{P_n} \tag{2.20}$$

$$C_b = \frac{1}{w_n Z_b} \tag{2.21}$$

The power factor seen by the grid is different from the actual power factor of the inverter, because of the reactive current produced by the filter capacitor. Therefore, in selecting the capacitor for LCL filter these variation of power factor is limit to $x = 5\%$[18]. The value higher then 5% can be used but the influence on the system power factor would be decreased.

$$C_f = xC_b \tag{2.22}$$

According to average current model of voltage source inverter, VSC output maximum current ripple can be calculated as[22]:

$$\Delta I_{Lmax} = \frac{2V_{DC}}{3L_1}(1-m)mT_{sw} \tag{2.23}$$

Where, m is the modulation and the maximum current peak ripples happened when $m = 0.5$, therefore putting value of $m$ in equation 2.23:

$$\Delta I_{Lmax} = \frac{V_{DC}}{6f_{sw}L_1} \tag{2.24}$$

For 5% ripple of inverter rated current $I_{max}$:

$$\Delta I_{Lmax} = 0.05I_{max} \tag{2.25}$$

where $I_{max}$

$$I_{max} = \frac{P_n\sqrt{2}}{3V_{ph}} \tag{2.26}$$

Therefore,

$$L_1 = \frac{V_{DC}}{6f_{sw}\Delta I_{Lmax}} \tag{2.27}$$

The constant $r_l$ is the ratio between grid side inductance $L_2$ and inverter side inductance $L_1$ of the LCL filter.

$$L_2 = r_l L_1 \tag{2.28}$$

The value of $r_l$ is selected to have peak to peak harmonic current in 10% to 20% rated current range of the inverter. The desired output ripple reduction can be used to estimate the value of $r_l$, while neglecting losses and damping of LCL filter, using equation. 2.29 [19].

$$\frac{i_g(h_{sw})}{i(h_{sw})} = \frac{1}{|1 + r_l(1 - a.x)|} \tag{2.29}$$

Where $a = L_1 C_b w_{sw}^2$ and $x = 0.05$.

The value of $r_l$ is used to calculate the $L_2$ using equation 2.28. Therefore Filter resonance frequency is obtained as:

$$w_{res} = \sqrt{\frac{(L_1 + L_2)}{L_1 L_2 C_f}} \tag{2.30}$$

The resonance frequency should satisfy the equation 2.31, therefore it cannot interfere with the control bandwidth of control system.

$$10 f_g < f_{res} < 0.5 f_{sw} \tag{2.31}$$

If equation 2.31 is not satisfied, parameter should be re-chosen.

Step by Step filter design procedure is shown in Fig.2-16 and filter capacitors are connected in Wye configuration. Following data is used to calculate filter parameters: $V_{LL} = 230\sqrt{3}V$, $P_B = 5kW$ rated power, $V_{DC} = 650V$ DC bus voltage, $f_n = 50Hz$ grid frequency, $f_{sw} = 10kHz$ switching frequency, maximum reactive power variation seen by grid $x = 0.05$, total attenuation of harmonics 30%.

1. The impedance and capacitance base value are calculated $Z_b = 32$ and $C_b = 9.94\text{x}10^{-5}$ using equations 2.20 and 2.21.

2. The inverter inductance $L_1 = 2mH$ is calculated using 5% ripple value in equation 2.27.

3. The capacitance $C_f = 5uF$ is calculated using $x = 5\%$ in equation 2.22.

4. The value of $L_2 = 4mH$ is calculated by setting harmonics attenuation to 30% using equations 2.28 and 2.29.

5. By putting the above calculated values in equation 2.30. The resonance frequency $f_{res} = 1.95kHz$ is calculated.

System parameters are summarized in table2.2.

Table 2.2: Parameters summary.

| | | |
|---|---|---|
| $f_g$ | Grid frequency | $50Hz$ |
| $f_{sw}$ | Switching frequency | $10kHz$ |
| $P_n$ | Rated Power | $5kVA$ |
| $V_g$ | Grid Voltage(L-L) | $400V$ |
| $V_{dc}$ | DC Bus Voltage | $650V$ |
| $L_1$ | Inverter inductor | $2mH$ |
| $L_2$ | Grid inductor | $4mH$ |
| $C_f$ | Filter capacitor | $5uF$ |

## 2.6 Resonance damping technique for LCL filter

The LCL filter provides compact as low cost solution for harmonics control of inverters, but inductors and capacitor of LCL filter cause resonance in close loop current control which make control unstable[13]. The most common and simple method to resolve this resonance effect is to deploy a passive element, a resistor in series with capacitor branch of LCL filter. This approach cause power losses and reduce the efficiency of the system[24].

The resonance damping technique used in this report to control the resonance is called active damping. In this technique a virtual resistor is added to damp the resonance effect of the LCL filter. Active damping can be implemented in different ways, the feedback loop with grid current derivation[16], capacitor voltage feedback, capacitor current feedback[12],[6], capacitor current feedback using lead-lag network[5],[7],[17] and implement notch filter at filter output voltage with self commission procedure in case of grid parameter variation[23],[11].

### 2.6.1 Active damping method

The active damping method used for LCL filter current control in this report, is the capacitor current feedback shown in Fig.2-17. In this approach capacitor current is measured and feed into the control loop after multiplying with a damping factor. This approach simulates a virtual resistor to damp the capacitor current without having power losses in the system. In active damping methods, the ratio $r_f = f_{sw}/f_{res}$ between the switching frequency and the resonance frequency has a crucial importance. If the designer want that resonance should not interfere with the current control loop then $f_{res}$ should be from halfway between $f_{bw}$ (the current control bandwidth) and $f_{sw}$. Therefore, the approximate ratio between $f_{bw}$ and $f_{sw}$ is $r_f = 4.5$. However, if $r_f < 6$, active damping method is not necessary to achieve stability in grid current control[26].

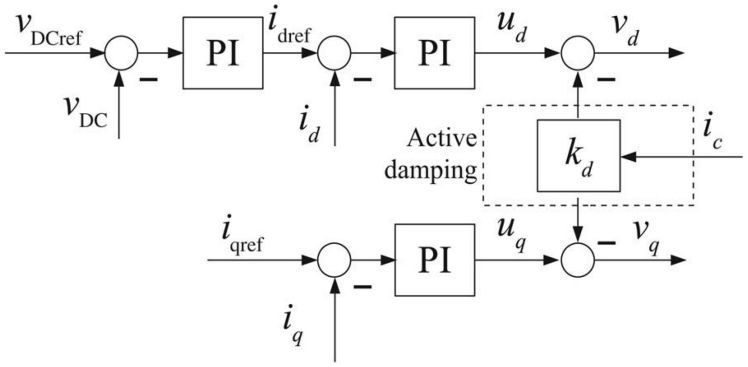



Figure 2-17: Control schematic of the grid converter with active damping capacitor current feedback.

The resonance frequency $f_{res}$ of LCL filter is:

$$f_{res} = \frac{f_{sw}}{r_f} = \frac{1}{2\pi}\sqrt{\frac{1}{C_f}(\frac{1}{L_1} + \frac{1}{L_2})} \tag{2.32}$$

For the capacitor current feedback as depicted in Fig. 2-18 the transfer function

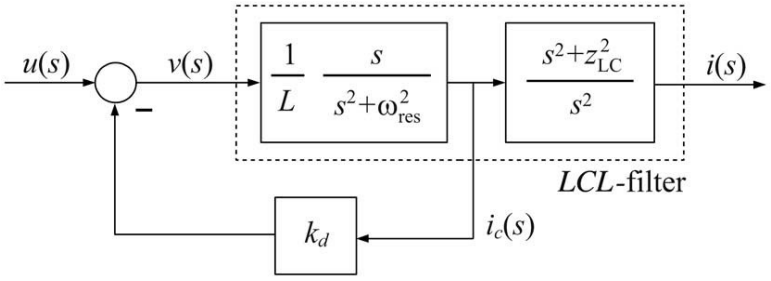



Figure 2-18: Transfer function blocks of grid converter with active damping capacitor current feedback.

between inverter current $i_i$ and inverter voltage $v_i$ is[26]:

$$G_{inv}(s) = \frac{i_i(s)}{v_i(s)} = \frac{1}{L_1 s} \frac{s^2 + z_{LC}^2}{s^2 + 2[\frac{k_d}{2L_1 w_{res}}] w_{res} s + w_{res}^2} \tag{2.33}$$

Where $\frac{k_d}{2L_1 w_{res}}$ is active damping, and $z_{LC}^2 = [L_2 C_f]^{-1}$.
The equation 2.33 shows that damping depends on the feedback gain $k_d$. After considering the ratios $r_l$ and $r_f$ the minimum damping constant for achieving stability is calculated. Therefore, the minimum damping $\zeta_{min}$ for stable close loop poles is [26]:

$$\zeta_{min} = \frac{1}{12\pi} r_f \frac{r_l}{\sqrt{1 + r_l}} \tag{2.34}$$

The implementation of capacitor current feed-back active damping control in digital domain causes the phase delay due to computation and PWM delay (Fig.2-19). Therefore, in controller design one sample delay is incorporated to compensate this delay. The value and polarity of $k_d$ can be estimated by the procedure given in[24].

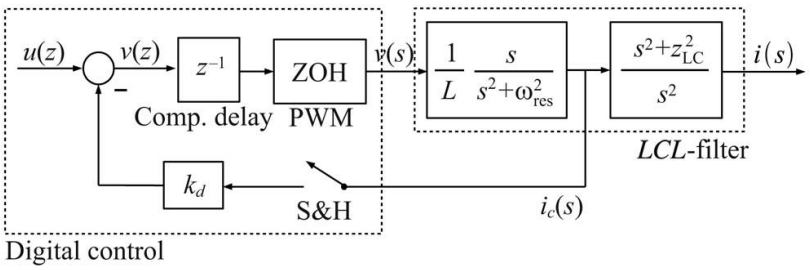



Figure 2-19: Digital control of the grid converter with active damping capacitor current feedback.

According to that article the computational delay transfer function at $w_{res}$ is given by equation 2.35.

$$G_d(jw_{res}) = e^{T_s jw_{res}} \frac{1 - e^{-T_s jw_{res}}}{jT_s w_{res}} \tag{2.35}$$

Where $w_{res} = \frac{2\pi}{3T_s}$.

At resonance frequency the computational and PWM delay is considered as zero. which makes equation 2.35 simplified and damping can be calculated by putting the solution of equation 2.35 in equation 2.34.

The conditions for $k_d$ can be calculated from equation 2.36 by putting value of $r_l$.

$$k_d G_d(jw_{res}) = k_d sinc(\frac{T_s}{2} w_{res})[cos(-\frac{3T_s}{2} w_{res}) + jsin(-\frac{3T_s}{2} w_{res})] \tag{2.36}$$

As we know only real part of equation. 2.36 produce active damping, which is in phase with capacitor current at resonance frequency[24].

$$k_d \Re G_d(jw_{res}) = k_d sinc(\pi/r_f) cos(3\pi/r_f) > 0 \tag{2.37}$$

It is clear from the equation 2.37 that the condition on real part of equation 2.36 can only be fulfilled, if $k_d$ is negative for $r_f = 6$. While for $r_f > 6$ the value of $k_d$ should be positive[24].

The zero and pole plot of current close loop in z plane is shown in Fig.2-20 while varying the value of $k_d$.

## 2.7 Grid current THD estimation

In this section grid current THDs are estimated by using the same approach presented in passive damping of the LCL filter[8]. First upper and lower rms bound values of capacitor current is calculated while neglecting the capacitor branch impedance. Capacitor current lower limit $i_c^{low}$ is given in equation 2.38 and capacitor current upper limit $i_c^{up}$ is given in equation 2.39 [24].

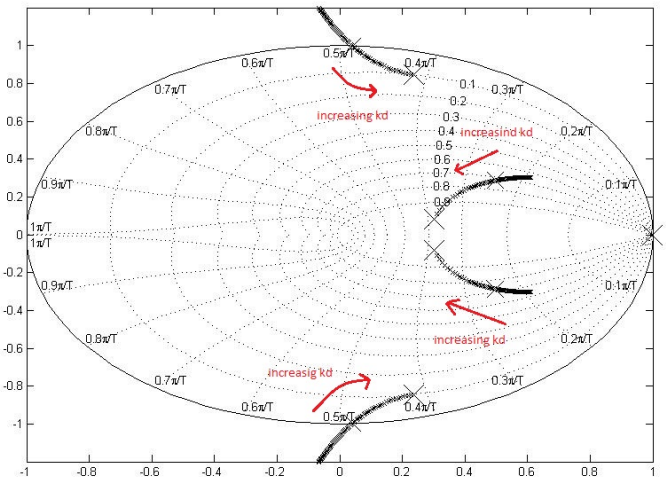



Figure 2-20: Zero and pole plot of current close loop in $z$ plane.

$$i_c^{low} = \frac{1}{2\sqrt{3}} \frac{1}{\sqrt{48}} \frac{v_{dc}}{f_{sw} L_1} \sqrt{\frac{3}{2} m^2 - \frac{3\sqrt{3}}{\pi} + \frac{9}{8}(\frac{3}{2} - \frac{9}{8}\frac{\sqrt{3}}{\pi} m^4)} \tag{2.38}$$

$$i_c^{up} = i_c^{low} | \frac{s^2}{s^2 + w_{res}^2} |_{s=j[(m_f-6)w_n]} \tag{2.39}$$

Where $m$ is the modulation index, $m_f$ is the frequency modulation ratio $m_f = f_{sw}/f_n$. The transfer function that relate $i_g$ and $i_c$ of LCL filter (shown in equation 2.40) is used to calculate the upper limit of grid rms current at $m_f - 6$ order, while harmonics in current are assumed to be negligible for this order.

$$i_g^{up} = i_c^{up} | \frac{j_g(s)}{i_c(s)} |_{s=j[(m_f-6)w_n]} = i_c^{up} \frac{z_{LC}^2}{[(m_f - 6)w_n]^2} \tag{2.40}$$

The grid rms current calculated in equation 2.40 is very optimistic estimation, as grid voltage harmonics, losses in IGBTs and fluctuation in DC bus voltage are not considered. The approximate THD in grid current is estimated by dividing the product of equation 2.40 and equation 2.38 by the rated fundamental harmonic current (THDs are below 5%).

## 2.8 STATCOM reactive power control

The hybrid STATCOM consist of one inverter rated at $5kva$ and four capacitor banks rated at $7.5kvar$, with $50uF$ capacitors connected in delta. The schematic of the system is shown in Fig.2-21. The power factor of customer facility is measured and given

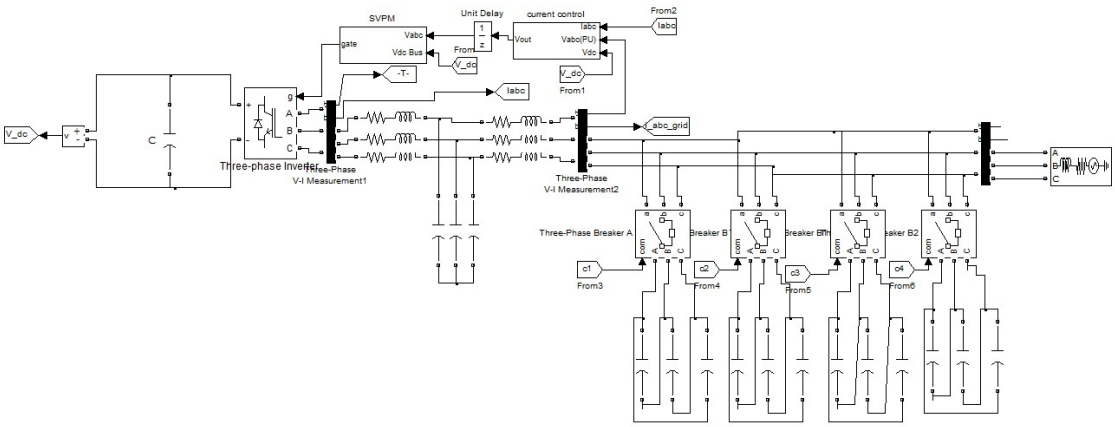



Figure 2-21: Schematic diagram of STATCOM.

to the power factor controller, which generate reactive reference for the STATCOM. The STATCOM inject required reactive power into the low voltage distribution network to keep power factor in specified range.

As inverter in STATCOM can operate $\pm$ $5kvar$ therefore, the reactive power controller can minimize the capacitor banks switching, that would increase the life of capacitor bank and power contactors without scarifying the dynamic performance of STATCOM. The small variations in reactive power are compensated by inverter, while large reactive power demand is satisfied by capacitor banks. The flow chart of reactive power controller algorithm and C code are shown in Fig.2-22 and Fig.A-4, respectively.

The operation of reactive power controller can be explained by these two scenarios. If reactive power controller estimate the reactive power reference of $18kvar$, it will switch ON two capacitor banks to provide $15kvar$ and the rest, $3kvar$ is compensated by inverter. The selection of reactive power source is also depend on previous state of STATCOM capacitor banks, if before $18kvar$ reactive power reference given to con-

troller, three capacitor banks are already switched ON and providing $22.5kvar$ into the grid. As reactive power controller is design to minimized the capacitor switching therefore, rather then switching one capacitor bank OFF, it will keep three capacitor banks switched ON and start operation inverter at $-4.5kvar$.

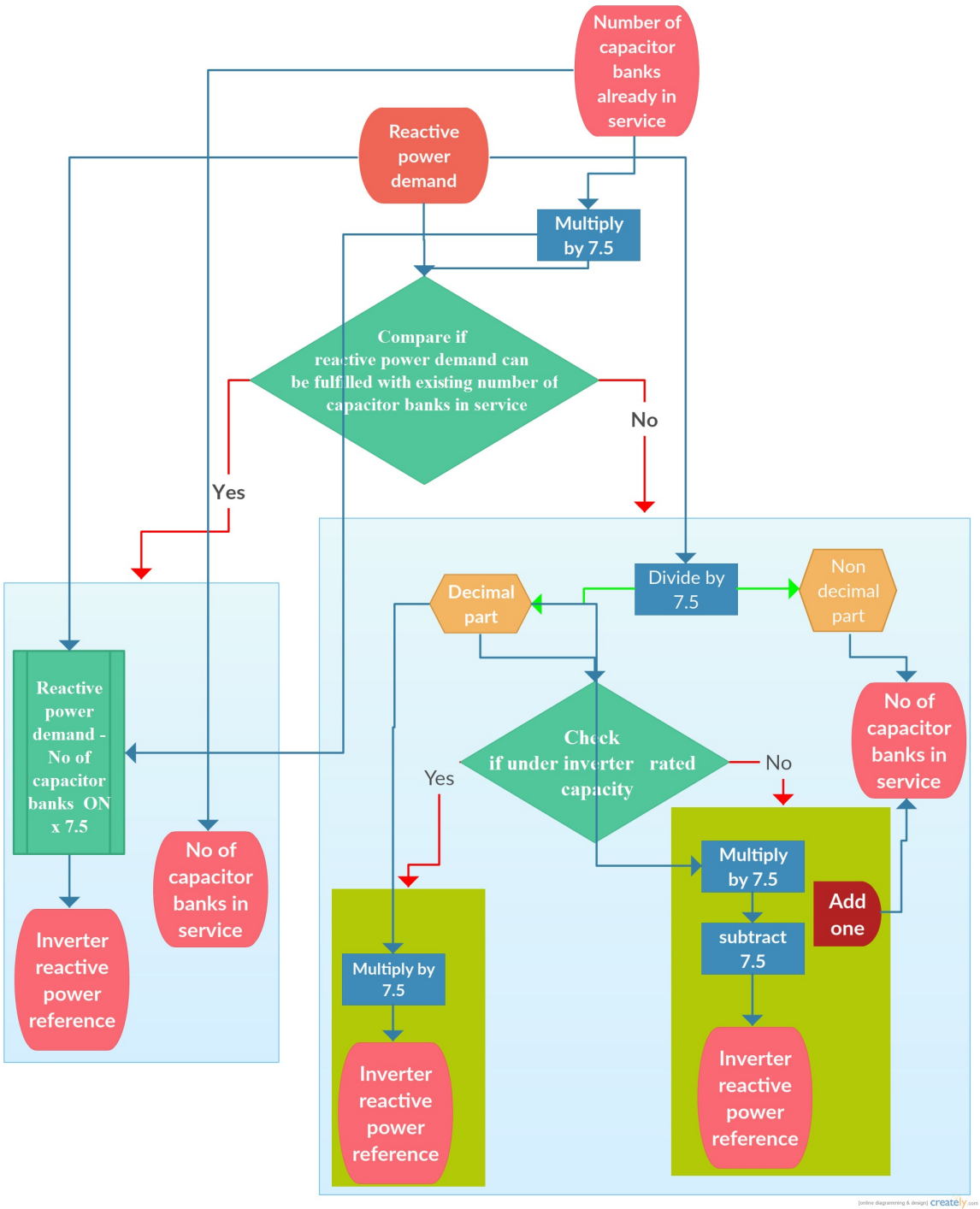



Figure 2-22: Reactive power controller algorithm flow chart.

# Chapter 3

# Simulation Studies

## 3.1 Objective

In this chapter simulation studies of the STATCOM is conducted in MATLAB Simulink platform. Different operational scenarios are discussed with their simulation results to support the design objective of the system. The first part of this chapter defines the key parts of the simulation model and the second part deals with simulation results.

## 3.2 STATCOM simulink model

The STATCOM simulink model is shown in Fig.3-1, which includes following main blocks:

- Three phase inverter.
- LCL filter.
- Inverter voltage and current control.(Fig.A-1)
- SVPWM block.(Fig.A-2)
- Measurement and reactive power controller.(Fig.A-3 & A-4)
- Delta connected capacitor banks.

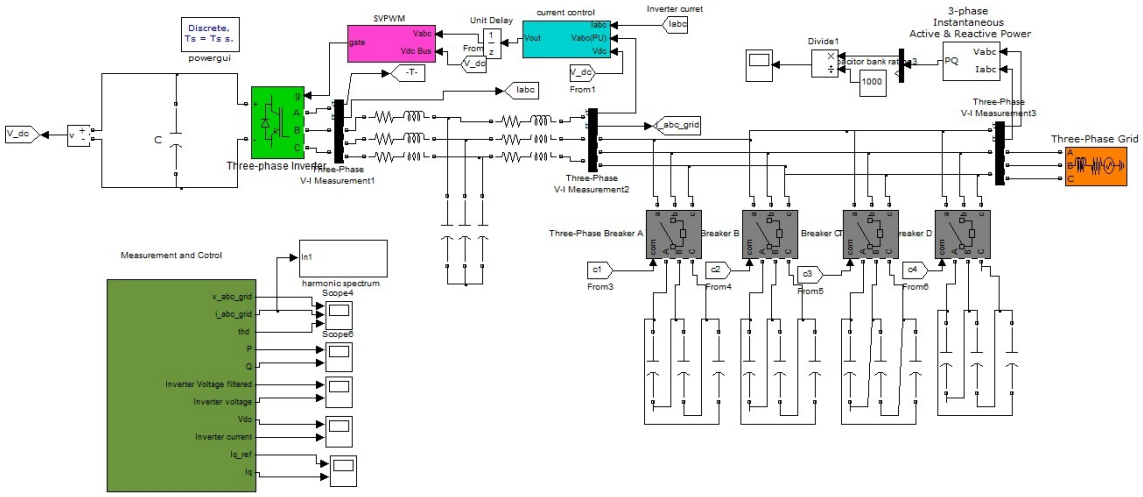
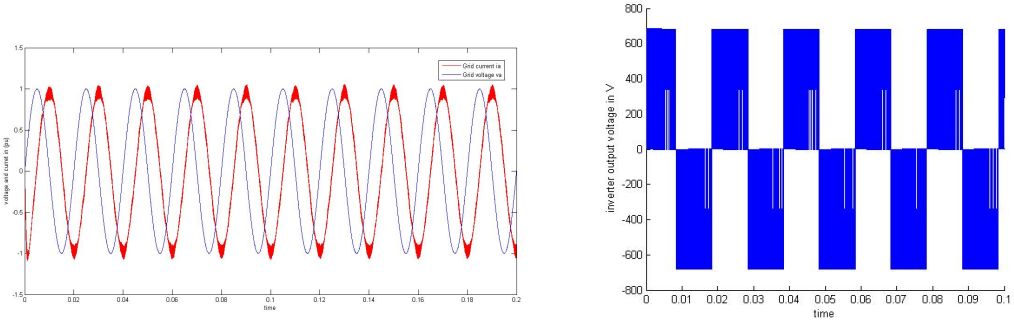



Figure 3-1: MATLAB simulink schematic diagram of STATCOM.

## 3.3 Simulation cases

### 3.3.1 Case 1 (reactive power to the grid)

In first case, $5kvar$ reactive power reference is given to the inverter and it will act like a capacitor bank of rating $5kvar$. The power reference is given in the form of stationary reference frame current $I_q$ and $I_d$. The external reference of $I_d$ is set to zero as no power transfer between grid and DC link is required, while the $I_d$ current is controlled by DC link voltage controller.




(a) $v_a$ and $i_a$. (b) inverter output voltage.

Figure 3-2: Inverter voltage and grid current.

The stationary reference frame currents references are calculated using equation.3.1 and 3.2.

$$p = u_d I_d + u_q I_q \tag{3.1}$$

$$q = u_d I_q - u_q I_d \tag{3.2}$$

The per-unit(pu) graph of grid phase voltage $v_a$ and line current $i_a$ is shown in Fig.3-2a. It is clear from the Fig.3-2a that the grid voltage $V_a$ lag the inverter output current $i_a$ by 90°.

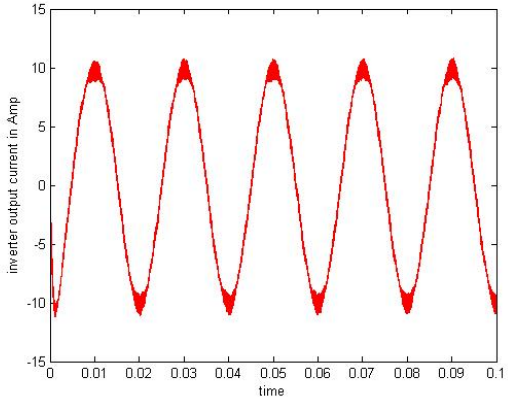
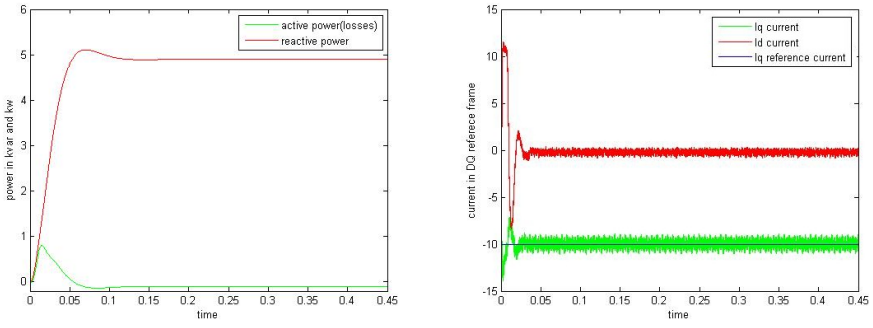



Figure 3-3: Inverter output current.

The DC bus voltage reference is set to $650VDC$ and DC bus voltage error is feed to DC voltage controller which control the $I_d$ current and keep the DC link voltage constant. Inverter output voltage is shown in Fig.3-2b which preset the switching of IGBTs.

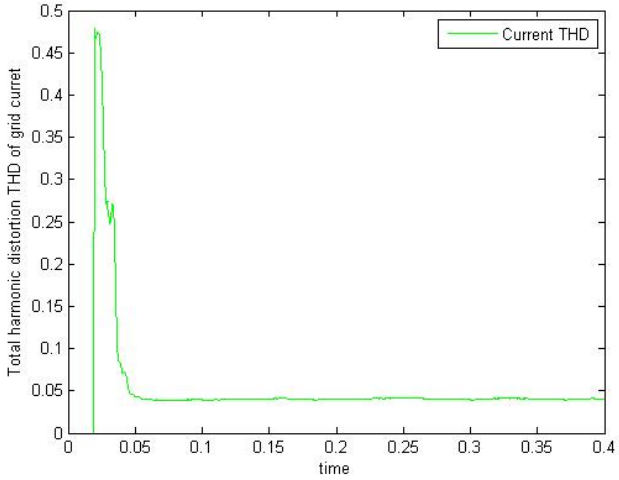



(a) Reactive and active power (b) $I_d$ and $I_q$ currents

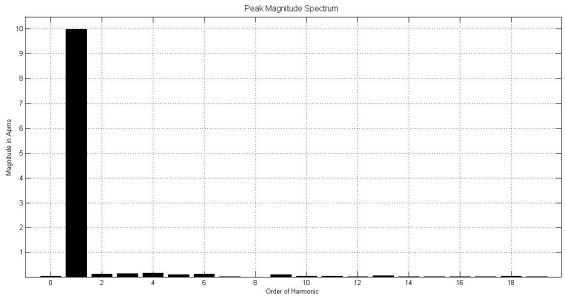
Figure 3-4: Reactive power & active power and $I_d$ & $I_q$ currents.

The inverter output line current ($10A$ peak) is shown in Fig.3-3, the current is sinusoidal and have some harmonics. The Fig.3-4 shows that power losses in LCL filter and IGBTs. The active power is negative, as power is transfer from grid to DC bus.

The Fig.3-5 shows the THD analysis of the inverter output current after LCL filter, performed by MATLAB simulink tool. THD of the current is less then 5%, which is IEEE standards limit for low voltage application. The bar graph of each harmonic order of inverter current is also depicted in Fig.3-5b.




(a) THDs of inverter output current.

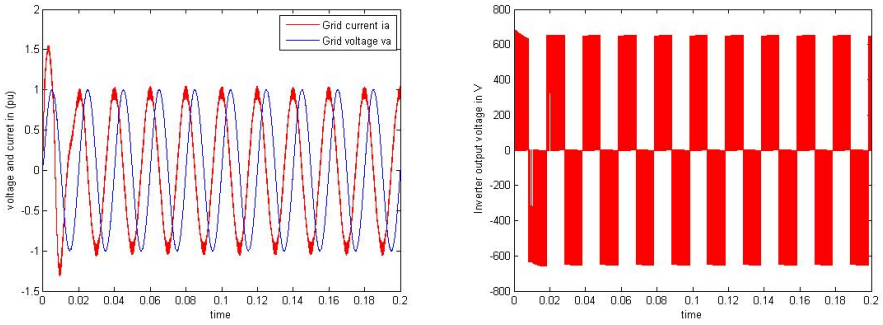



(b) Magnitude graph of each harmonic order.

Figure 3-5: Harmonic order and THDs of inverter current.

### 3.3.2 Case 2 (reactive power from the grid)

In second case, $5kvar$ reactive power reference is given to the inverter, it act like a inductive load of rating $5kvar$. The power reference is given in the form of stationary reference frame current $I_q$, and $I_d$. The external reference of $I_d$ is set to zero as no power transfer between grid and DC link is required, while the $I_d$ current is controlled by DC link voltage controller. The per-unit(pu) graph of the grid phase voltage $v_a$




(a) $v_a$ and $i_a$. (b) Inverter output voltage.

Figure 3-6: Inverter grid current and voltage graph

and the line current $i_a$ is shown in Fig.3-6a. The Fig.3-6a shows that grid voltage $v_a$ leads the inverter output current by 90°.

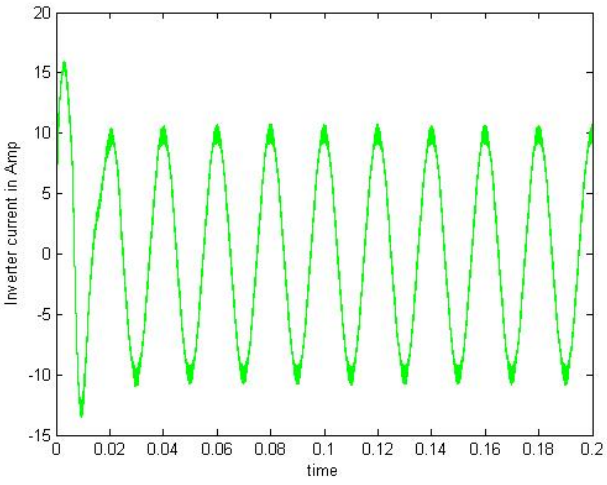
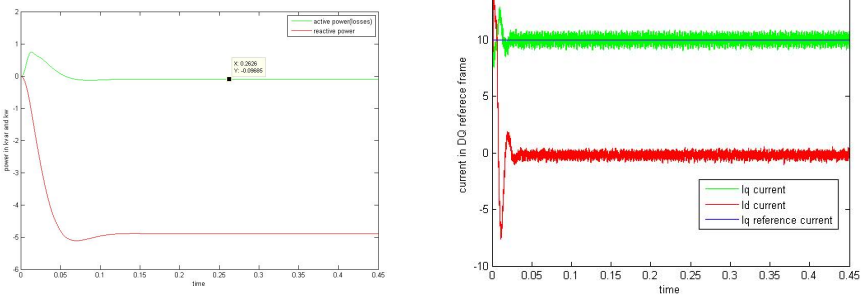



Figure 3-7: Inverter output line current.

The inverter output voltage is shown in Fig.3-6b.The Fig.3-7 shows the inverter

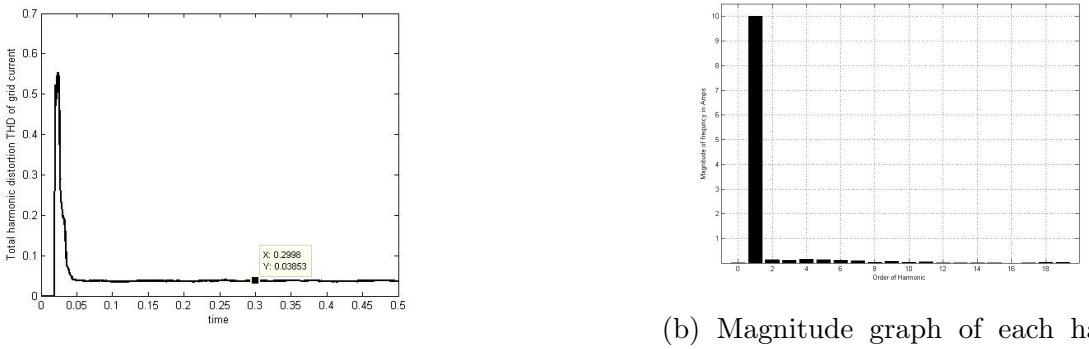
output current with peak amplitude $10A$. The Fig.3-8 shows that power losses in




(a) Reactive and active power. (b) $I_d$ and $I_q$ currents.

Figure 3-8: Reactive power & active power and $I_d$ & $I_q$ currents.

LCL filter and IGBT. The total power losses in the system are $90watt$, Therefore system efficiency is above 98%. The Fig.3-9 shows the THD analysis of inverter




(a) THDs of inverter output current.

(b) Magnitude graph of each harmonic order.

Figure 3-9: Harmonics and THDs of inverter output current.

output current. The THD in the current is 3.8%, which is less then IEEE standards limit (5%) for low voltage application. The bar graph of each harmonics order in inverter output current is depicted in Fig.3-9b.

### 3.3.3 Case 3 (step change in reactive power demand)

The reactive power reference is changed from $2.5kvar$ to $5kvar$ at time $t = 2.5s$. The reference step change is performed in zero time to verify the dynamic response and robustness of the current control for abrupt reactive power demand variations. The

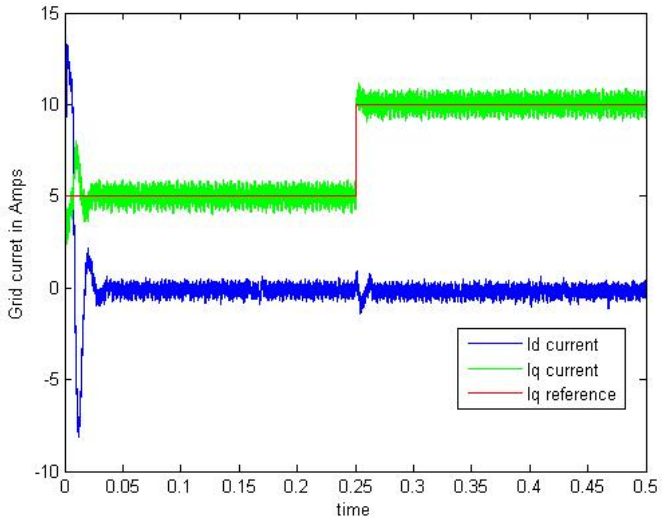



Figure 3-10: $I_d$ and $I_q$ current.

Fig.3-10 shows that $I_q$ follows the reference current without significant time delay, while there is a small transient in $I_d$ that is stabilized in $0.02s$.

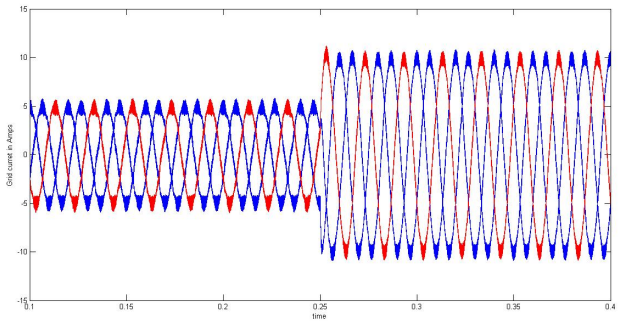


Figure 3-11: Inverter output line current $i_a$.

The inverter output current moved from $5A$ peak to $10A$ without losing synchronism with the grid and without phase fluctuation.(see Fig.3-11)

### 3.3.4 Case 4 (step change from rated leading *kvar* to rated lagging *kvar* )

In this test, the inverter control is verified at worst possible condition. The reactive power reference is changed from rated leading to rated lagging reactive power demand

in approximately zero time.

Fig.3-13a shows that reference current $I_q$ switched from $-10A$ to $10A$ (peak) at time

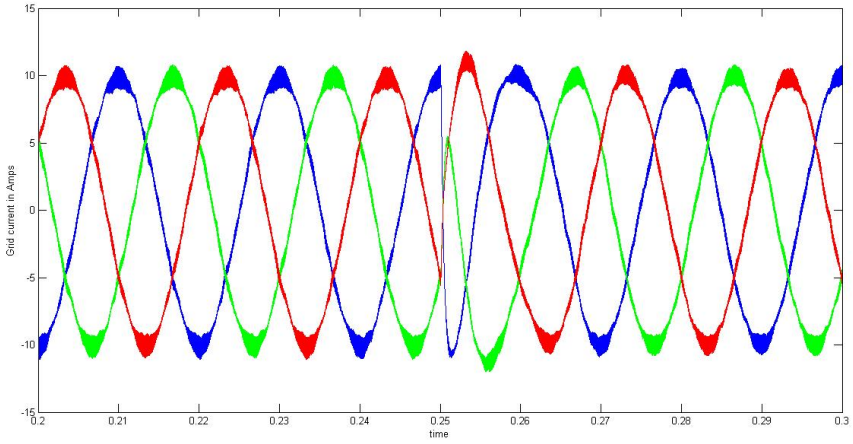
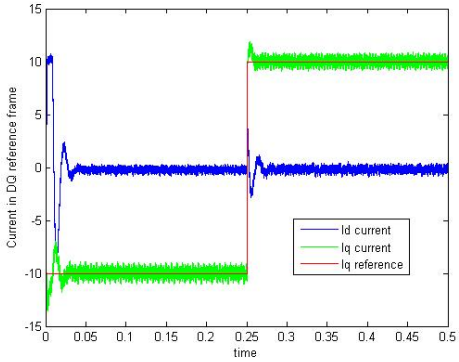


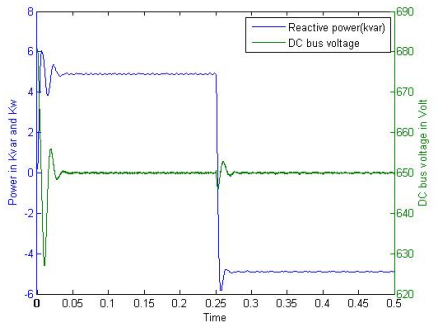

Figure 3-12: Inverter three phase output line current.

$t = 0.25s$. The inverter output currents changes their phase by 180 degree to provide new reactive power demands within $0.01s$ (see Fig. 3-12). The system settled to new reactive power demand within half the time cycle of fundamental frequency ($10ms$).

The Fig.3-13a shows that $I_q$ current change from $-10A$ to $10A$ with in $0.01s$, while




(a) $I_d$ and $I_q$ current.




(b) DC link voltage and reactive power.

Figure 3-13: Reactive power and stationary reference frame currents

there is very small overshot in $I_q$ before settling at new reference value. The second graph(3-13b) shows the effect on DC link voltage, A $1100uF$ capacitor is charged to $650VDC$ to provide energy during inverter transients. During the reactive power

changing from leading to lagging, the DC link voltage first drop down by $4V$ and then rise $4V$ from reference value during the transient time, although it stabilize to reference value ($650VDC$) with in $0.02s$.

## 3.4 Reactive power controller

The reactive power controller accept reactive power reference as input and decide how much reactive power should be delivered by the inverter and how many capacitor banks should be taken in the service with the aim of minimizing the switching events of capacitor banks power contactors.

### 3.4.1 Case 1(verification of reactive power controller functionality)

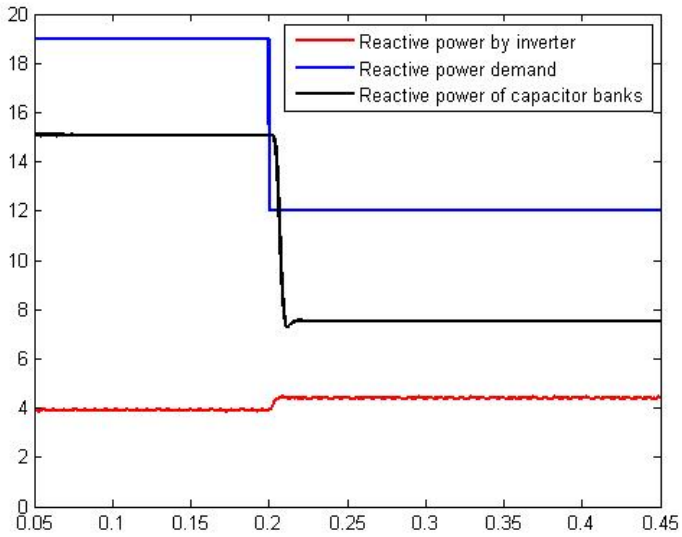



Figure 3-14: Reactive power form inverter and capacitor bank.

In this case, the basic function of reactive power controller is presented without its extended functionality of minimizing capacitor banks contactors switching. As shown in the Fig.3-14 at time $t = 0s$ when reactive power reference was $19kvar$, $4kvar$ are given by inverter and rest ($15kvar$) by two capacitor banks($7.5kvar$ each).

When reactive power reference changed to $12kvar$ at time $0.2s$ one capacitor bank is switched OFF (shown in Fig.3-15) and inverter start providing $4.5kvar$.

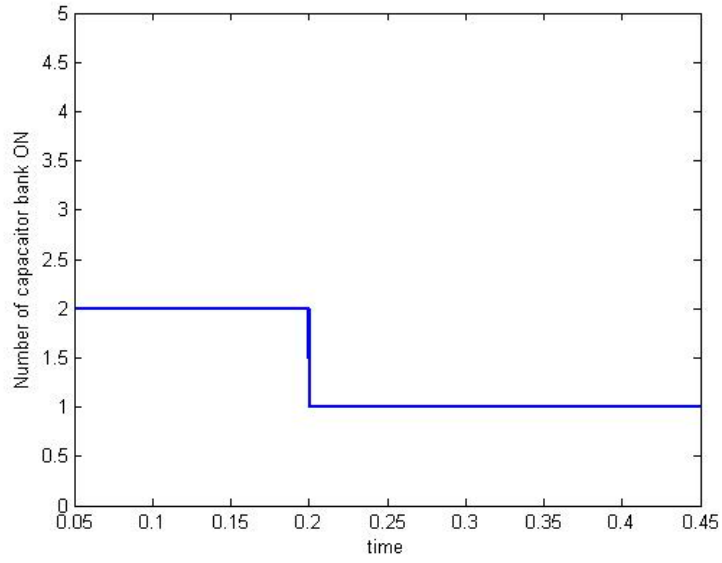


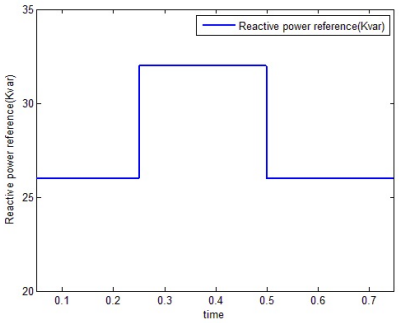

Figure 3-15: Status of capacitor banks.

### 3.4.2 Case 2 (Minimizing capacitor bank switching)

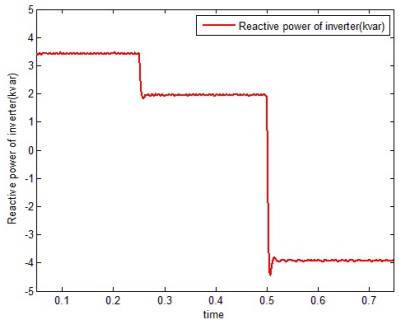
In this case the functionality of reactive power controller to minimize the capacitor bank switching is presented. First reactive power reference of $26kvar$ is applied at time $t = 0.00s$(see Fig.3-16a), the reactive power controller switch ON three capacitor banks(see Fig.3-16d) to provide $22.5kvar$ (see Fig.3-16c), the remaining reactive power ($3.5kvar$) is delivered by inverter(see Fig.3-16b).

At time $t = 0.25s$ reactive power reference is changed to $32kvar$ (see Fig.3-16a), the reactive power controller switch ON four capacitor banks(see Fig.3-16d) to provide $30kvar$ (see Fig.3-16c), the remaining reactive power ($2kvar$) is provided by inverter.

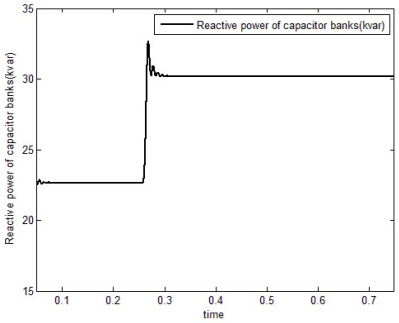
At third instant $t = 0.5s$, the reactive power reference again changed to $26kvar$ (see Fig.3-16a), according to previous calculation three capacitor bank should be switched ON, but reactive power controller verify the previous state of capacitor banks in service that was four, therefore to minimize the capacitor bank switching reactive power controller keep four capacitor banks in service to provides $30kvar$ (see Fig.3-16c) and



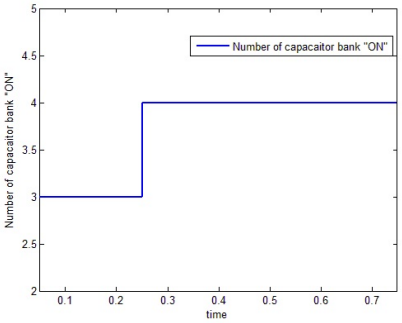

(a) *kvar* reference to reactive power controller.




(b) Reactive power delivered by inverter to grid.




(c) *kvar* delivered by capacitor banks.




(d) Number of capacitor banks in service.

Figure 3-16: Minimized capacitor bank switching.

inject lagging reactive power $-4kvar$ from inverter (see Fig.3-16b) to balance and achieve reactive power reference.

# Chapter 4

# Hardware Setup Detail

## 4.1 Objective

This chapter present the control hardware and electronic circuits used for the experimental evaluation of the hybrid STATCOM system. The system setup consist of a hardware in loop (HIL) RT-lab platform that work with MATLAB simulink based model with some extra libraries for RT-lab system integration. The main components include: a Semikron inverter, optical fiber communication PCBs, DC power sources, voltage and current sensor boards, RT-LAB Engineering Simulator, LCL filter, relay board, capacitor banks, monitoring computer (PC) with RT-LAB build-time tool and OPAl RT-lab platform.

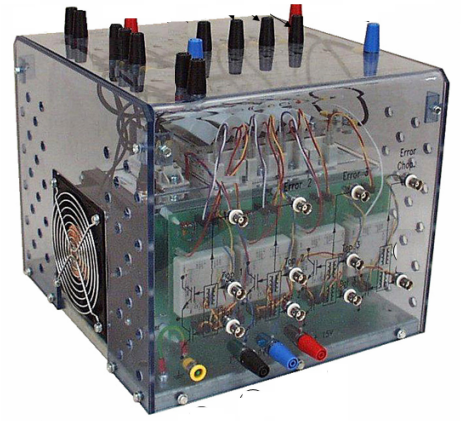
## 4.2 Three phase inverter

The three-phase inverter used in the experiment is power IGBT module of SEMIKRON Electronics Teaching System. This module consists of the following elements:

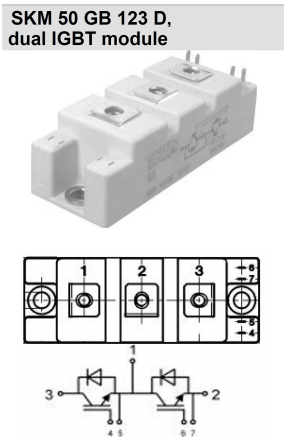
∗ Aluminum radiator fan (see Fig.4-1a) for heat dissipation of semiconductor components.

∗ Three drivers SKHI 22A SEMIKRON (See Fig.4-1a) to control the firing of IGBTs and protection of IGBTs and user module. These drivers are responsible for

input signals handling, adaptation & processing for ON & OFF of IGBTs, monitoring of possible errors in input firing signals, detect short-circuit and under-voltage in IGBT block and provide isolation between the input side signals & power section. Each one of these drivers are associated with one branch of the IGBTs and supplied with $15VDC$ source.



(a) Three-phase Inverter module[1].




(b) IGBT SKM 123 GB module[1].

Figure 4-1: Power IGBT module of SEMIKRON Electronics Teaching System.

∗ There are three IGBT SKM 123 GB 50 D modules in inverter (See Fig.4-1b)each of these modules is composed of two IGBTs with respective anti-parallel diodes. IGBTs are closed when a signal voltage of $15VDC$ is applied between gate and open emitter terminal and open when a signal of $-15VDC$ applied between these terminals.

∗ Two electrolytic capacitors of $2200uF/400V$ are connected in series equivalent to a DC link capacitor of $1100uF/800V$.

∗ There is a temperature sensor in the radiator to protect system from overheating, The power supply of the driver card is connected in series to the temperature sensor normally close relay contact. If temperature cross set limit, sensor relay contact automatically shut down inverter module power supply to save system from permanent damage.

∗ The inverter also include a three phase uncontrolled rectifier that is supplied

with three phase voltage from the grid, if variable frequency functionality is required. Although this rectifier is not required for this research project.

## 4.3 Programmable power source

The hardware prototype was first tested with a three phase programmable power source and the finally test is performed with low voltage grid supply. Following is the introduction of three phase programmable power source:
The Elgar SmartWave Model SW 5250A (see Fig.4-2)use transformer less, direct coupled amplifiers and work as a true arbitrary waveform generator. Three phase power waveform with different frequency and amplitude can be generated by this power source. This device support up to $320VAC$ single phase voltage. The system allows the user to set over-current and over-voltage rating of simulated power waveform. This unit is design to simulate low voltage grid to test system in harmonics free environment[2].

Figure 4-2: Elgar SmartWave Model SW 5250A[2] .

## 4.4 Auxiliary power and DC link charging circuit

### 4.4.1 DC link charging circuit

When inverter is connected directly to power grid the DC bus capacitors are charged in abrupt manner, it is similar to a short-circuit at capacitor terminals. This heavy inrush current can damage the DC bus capacitor or cause tripping of power protection device. Therefore, a charging circuit is recommended for control charging of DC link. DC link charging circuit comprises of following elements:

∗ Timer relay RE7ML SCHNEIDER ELECTRIC with auxiliary contact for ON delay & OFF delay. Timing associated with this relay determines the duration of DC link capacitor per-charge.

∗ A pre-charge resistor.

∗ Two contactors LC1D32 SCHNEIDER ELECTRIC. Contacts associated with these contactors are normally open. The first three-phase contactor connects the power source with inverter through precharge resistors. During that time, timer relay wait for preset time, and when time delay expires the second contactor connects the rectifier of inverter directly to power source bypassing the precharging resistors.


Figure 4-3: Auxiliary Power and DC link charging circuit.

### 4.4.2 Auxiliary power circuit

The auxiliary power supply includes following elements:

∗ A DC voltage source ($15VDC$, $4A$) is used to power optical fiber communication PCB and the inverter drivers card of SEMIKRON module.

* SEMIKRON module cooling fan is supplied with single phase AC power supply($230Vrms$, $50Hz$) through a power breaker.

* A DC voltage source ($\pm 15VDC$ MINI-PS-100-240AC / 2X15DC / 1 PHOENIX CONTACT) powered the signal conditioning card and voltage & current sensing PCBs.

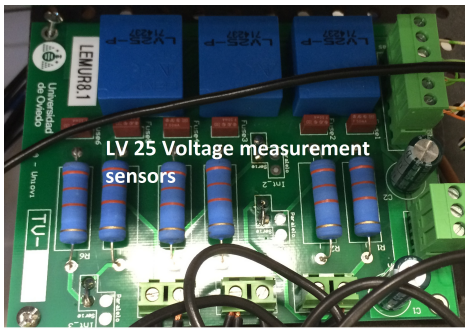
## 4.5 Sensors and optical fiber transmission system

The STATCOM control strategy discussed in this thesis require measurement of grid voltage, DC link voltage, grid currents and inverter currents. These measurement sensors are built using following components:

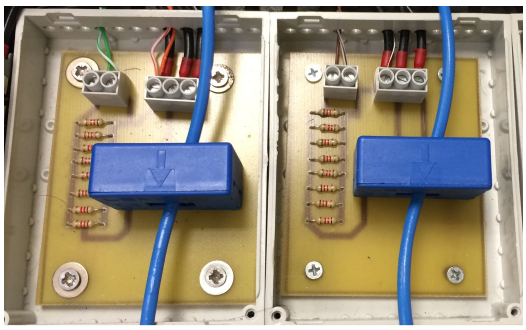
* Four voltage measuring sensors LEM LV25-P.

* Four current measuring sensors LEM LA55-P.

* Two PCBs for signal conditioning and communication using optical fiber.




(a) Grid voltage sensors.



(b) Current sensors.

Figure 4-4: Current sensor and voltage sensor.

Two current sensors are used to measure grid currents $I_{ga}$ and $I_{gb}$ (see Fig.4-4b) and other two current sensors are used to measure inverter currents $I_{ia}$ and $I_{ib}$, however the third grid ($I_{gc}$)and inverter current ($I_{ic}$) is estimated while supposing system is balanced and current through neural conductor is zero. Although, there are three voltage sensor that measure three phase grid voltages (see Fig.4-4a) and provide isolation between grid voltage and the analog to digital converter (ADC) inputs of the RT-lab cards. This voltage sensing card is designed by LEMUR research lab of

university of Oviedo and it was borrowed for this project prototype. One voltage sensor is used to measure the DC link voltage. The complete sensor board is shown in Fig.4-5.

Moreover, sending and receiving of digital signals from the control platform to the

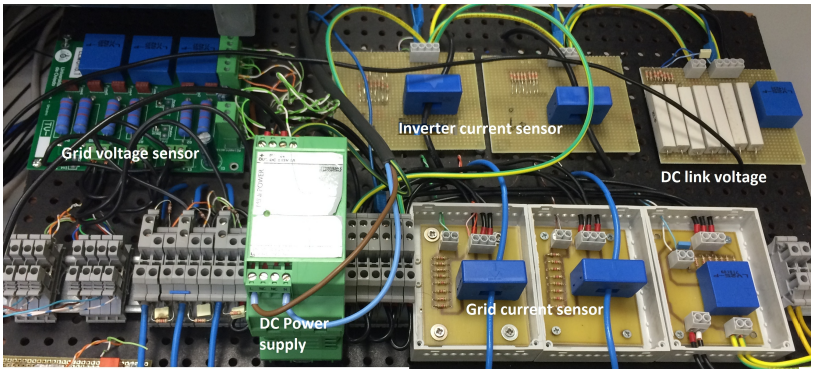
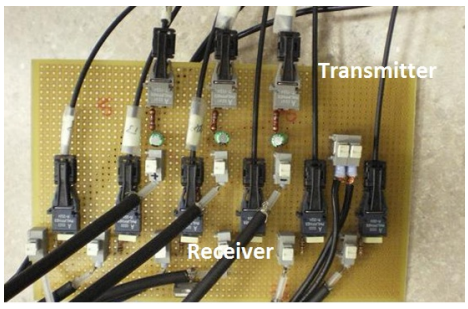
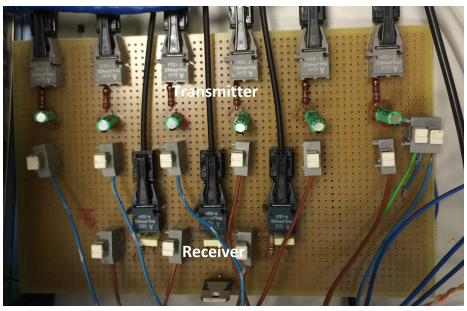



Figure 4-5: Complete sensor board.

inverter (the firing signals of IGBTs and error signals associated drivers of IGBTs) is performed through optical fiber transmission system. At the inverter side and control platform side, two printed circuit boards(PCBs) are used for digital signal conditioning and transmission. The inverter side PCB comprises of three transmitters T-1524 and six receivers R-2524 from AGILENT TECHNOLOGIES and control platform side PCB has six transmitters T-1524 and three receivers R-2524 (see Fig.4-6).




(a) Inverter side optical fiber interfacing PCB.




(b) Control platform side optical fiber interfacing PCB.

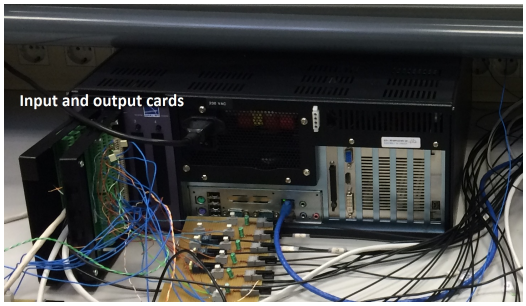
Figure 4-6: Signal conditioning and transmission PCBs through optical fiber.

## 4.6 OPAL RT-lab prototyping platform

The STATCOM components are controlled through OPAL-RT real-time simulation platform by RT-LAB TECHNOLOGIES (see Fig.4-7). The RT-Lab platform is actually a conventional CPU with WANDA 4U chassis and two cores of activated computer system operating with QNX v6.3. The platform used in the experimental trials of this thesis is in configuration called rapid control prototyping. The architecture of the rapid control prototyping system consist of two fundamental elements:

∗ A conventional computer or PC-console (Host PC) (see Fig.4-7b), to create and edit the control Simulink model and compiled to check its compatibility with the RT-Lab environment. On the other hand, the PC-console also allows the user to modify system parameters and observe simulation results in real time.

∗ The RT-Lab (Target-PC) (see Fig.4-7a) is the platform that load and run compiled model of the real-time control system. The platform also communicates with the PC-console via TCP / IP protocol and with two inputs and outputs modules(analog OP5340 and OP5330 , respectively) digital (OP5311 and OP5312, respectively) for interaction with inverter. The management of these modules is done via an FPGA.




(a) The RT-Lab (Target-PC)

(b) PC-console (Host PC)

Figure 4-7: RT-lab rapid prototyping control system

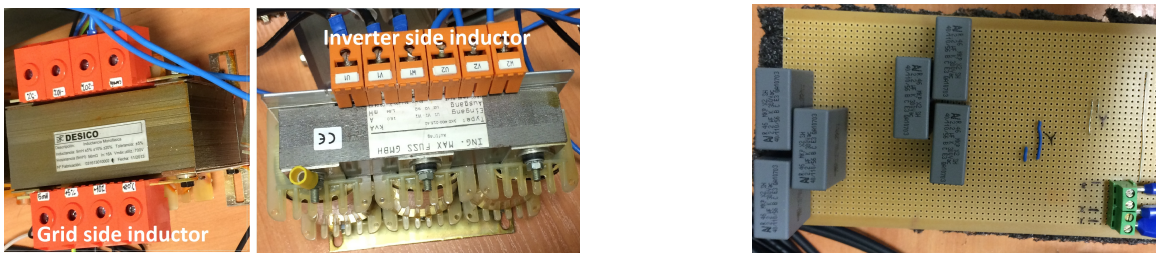
The simulation of the real time control system requires a fix sampling period to read the signals from input cards, perform necessary calculations and write the signals to output cards. The reduced sampling period increases the accuracy of the results, but this platform have hardware limit for the sampling rate selection. The minimum sampling step that can be selected in this system is $10us$.

## 4.7 LCL filter

The LCL filter used in this project is comprises of following parts:

### 4.7.1 Filter inductances

The LCL filter is implemented with inductors already available in the lab. The inverter side inductor is a three phase inductor with inductance value $1.85mH$ and current rating $16A$ (see Fig.4-8a). The grid side inductor is multi tapped single phase inductor with current rating $16A$ and nominal inductance $5mH$ ($\pm 20\%$ $\pm 10\%$ and $\pm 5\%$), therefore three set of these inductors are used with $-20\%$ tap to implement $4mH$ design inductance.(see Fig.4-8a)




(a) LCL filter inductances.

(b) LCL filter capacitor.

Figure 4-8: LCL filter

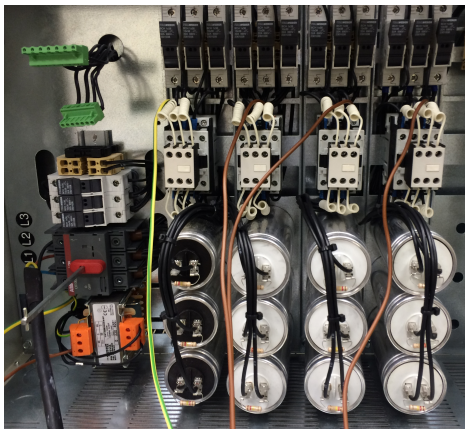
### 4.7.2 Filter capacitor

The design value of LCL filter capacitor is $5uF$ , therefore two $2.2uF$ capacitors connected in parallel for each phase to approximate the design value of capacitance (see Fig.4-8b).

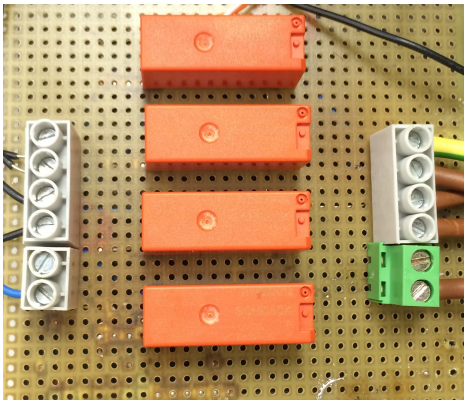
## 4.8 Capacitor bank

A low voltage switch capacitor reactive power compensation device is used as capacitor bank(see Fig.4-9a). Which comprises of four sets of capacitor banks that can individually switched ON and OFF through their power contactors, rated at $110VAC$. The power contactors are controlled by digital outputs of RT lab platform therefore,

a PCB is fabricated with four relays (closing coil $15VDC$)to control contactors of capacitor banks(see Fig.4-9b).



(a) Capacitor bank.



(b) Capacitor bank control relay board.

Figure 4-9: Capacitor bank and its control relay board.

# Chapter 5

# Laboratory Prototype and Results

## 5.1 RT-Lab simulation model

Laboratory prototype of STATCOM is built using hardware explained in chapter 4. The OPAL RT-lab platform is used to implement the control and extract simulation results. This platform enable users to export the MATLAB Simulink model to RT-lab workbench, but before compiling, model need to be customized according to specified requirement of RT-Lab workbench. The following blocks from RT-lab simulink libraries are induced in mode: the data communication block(console and master interfacing), digital input block, digital output block and analog inputs block. The complete RT-lab model is shown in Fig.A-5 appendix A. below are the important blocks of simulation model.

### 5.1.1 Console and master control block

RT-lab control system is divided into two main parts, the console and the master control block. The console block runs on host computer and provide access to different parameters for monitoring and modification during real time simulation. Console block use special RT-lab Opcom block to communicate with master control block (see Fig.5-1). Hardware control, signal import and export blocks are included in master control block that run on target computer.

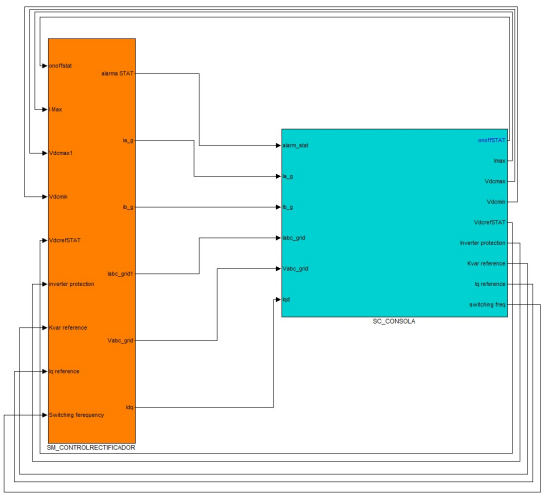



Figure 5-1: Console and master control block.

### 5.1.2 Current control block.

Current control block work in the same way as explained in chapter 2. Grid voltage angle is extracted from PLL block and this angle is used by *abc* to *dq* block to transform sinusoidal currents in to stationary reference frame. $d$ and $q$ axis current errors are input to PI controllers to generate $V_d$ and $V_q$ reference voltages. The feed-back and feed-forward terms are added to these signals before transforming them back in to sinusoidal reference voltage using $dq$ to $abc$ transformation. (see Fig.5-2) SVPWM generation block use these sinusoidal reference voltages as input to generate gate firing signals.

### 5.1.3 SVPWM generator

RTE SVPWM block from RT-lab library is included in model to generate PWM (see Fig.5-3). It is a field-programmable gate array(FPGA) based block that configure internal FPGA of RT-lab to generate PWM of specified switching frequency.The RTE SVPWM block generates square wave pulses at regular time intervals. The frequency and duty cycle input signals determine the shape of the output waveform. This approach increase the efficiency and speed of simulation. In this model PWM switching frequency is set to $10kHz$, RTE SVPWM block change the duty of output signal depending on normalized input signal.

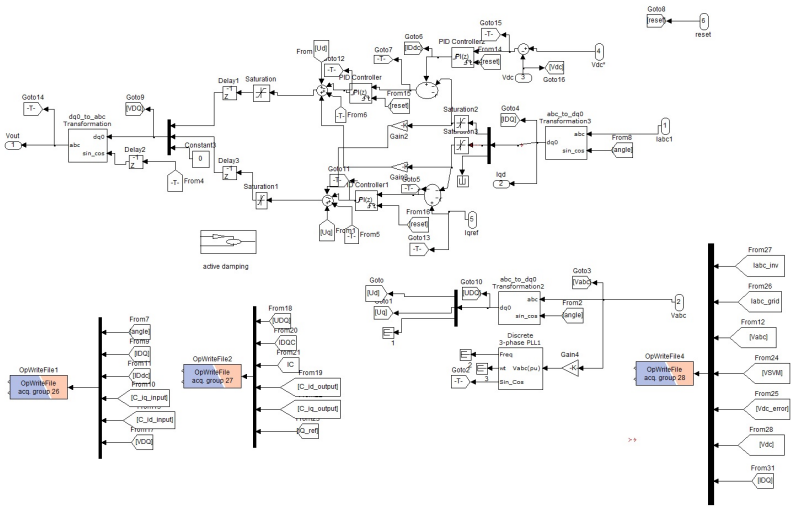



Figure 5-2: Current control block.

The output gate pulses from RTE SVPWM block are converted to suitable data type by RTE conversion block (FPGA based) and terminated o digital output card of RT lab event generator block.(see Fig.5-4)

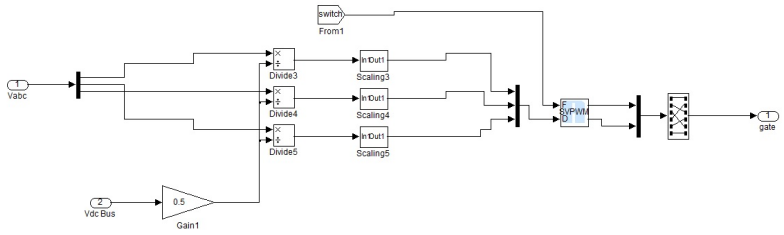



Figure 5-3: SVPWM generation block.

### 5.1.4 Inverter protection block

Hardware protection is one of the most important block during testing of system. The software based protection block is used in this prototype (see Fig.5-5). The protection block continuously monitor DC link voltage, the inverter phase currents, temperature of inverter heat sink and driver error signals of three IGBT modules. If any of these monitoring parameter cross the predefine limits, the protection block stop the gate signal to the inverter and display the information on console fault motioner.(see Fig.A-6 appendix A)

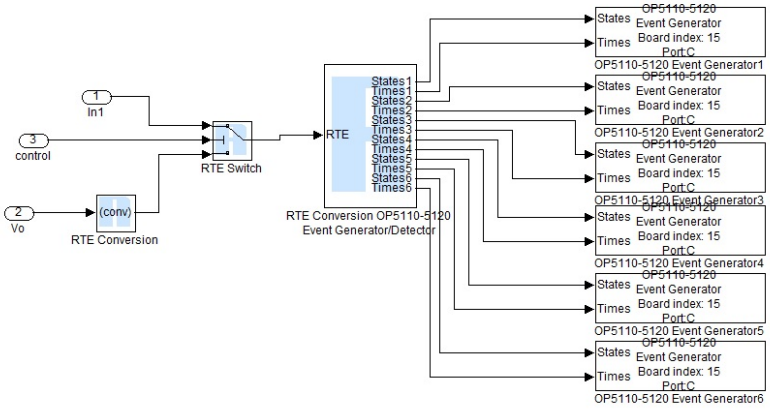



Figure 5-4: FPGA output data conversion block.

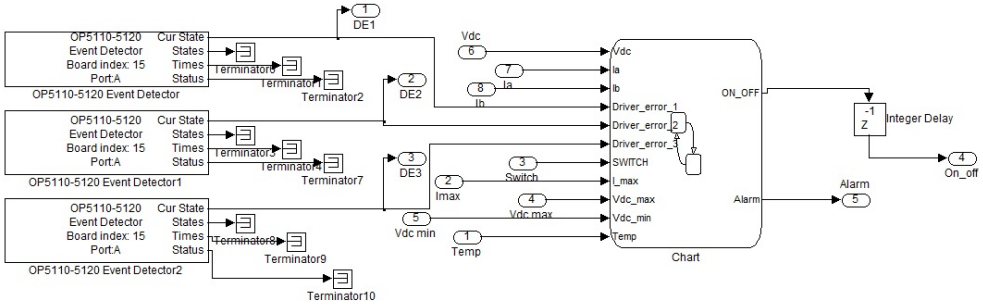



Figure 5-5: Inverter protection block.

## 5.2 Experimental results

In this section laboratory prototype experimental results are presented to support simulation results. The experimental results are divided in two main parts: The first part deals with inverter testing with LCL filter and second part present performance of reactive power controller with capacitor banks.

### 5.2.1 Inverter experimental result

The inverter is always synchronized with grid voltage, the grid voltage angle is detected using PLL block. The Fig.5-6 shows the grid $V_a$ and angle output from PLL block. The inverter experimental result are presented in different operational scenarios. These tests are performed on the inverter to verify and validate the control design. Following are the inverter test cases:

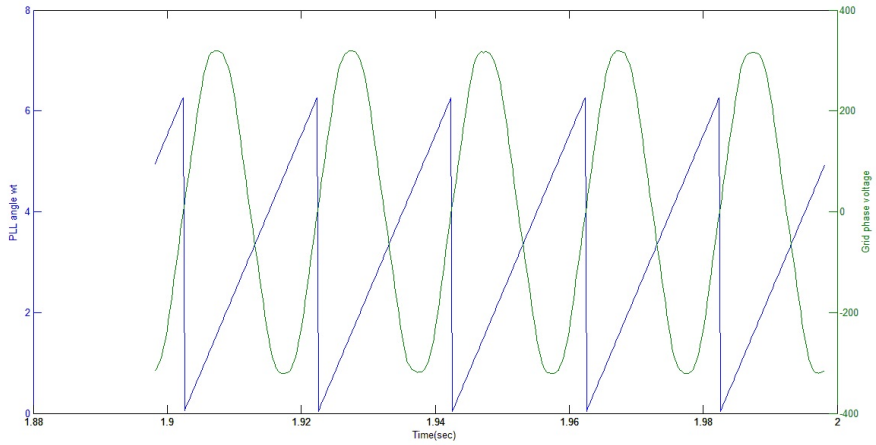
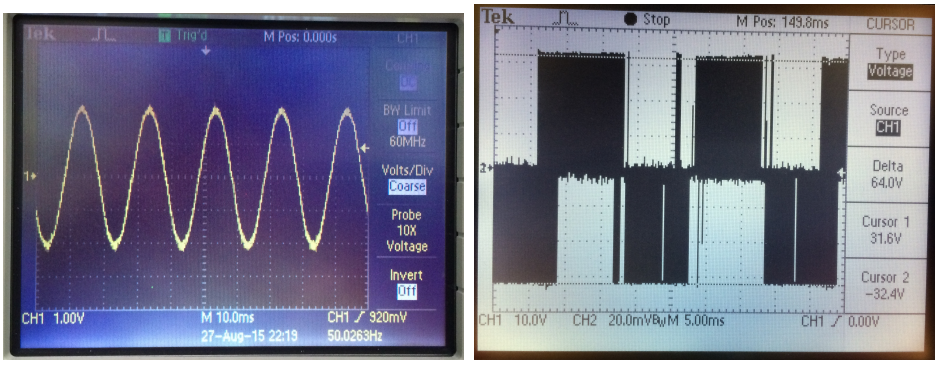



Figure 5-6: Grid phase voltage and PLL output angle.

**Case:1 (Rated reactive power demand)**

In first case, reactive power reference of $5kvar$ is given to the inverter in the form of $I_q$ current. The reference value of $I_q$ is set to $10A$ and $I_d$ reference is set to zero (see Fig.5-8b), as no active power exchange is required, while $I_d$ reference in generated by DC bus controller to compensate the losses in system. The oscilloscope graphs of inverter output current and voltage are shown in the Fig.5-7

The three phase output current of inverter and synchronous reference frame current

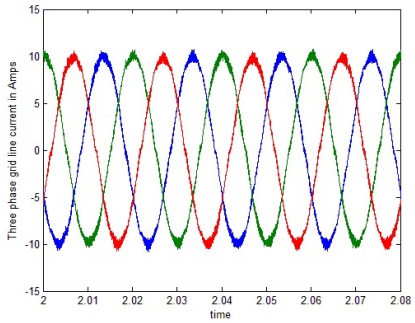



(a) Inverter output current $i_a$. (b) Inverter output voltage.

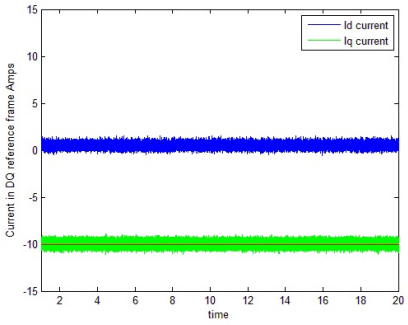
Figure 5-7: Oscilloscope graphs of inverter voltage and current.

$I_d$ & $I_q$ are shown in Fig.5-8.

The total harmonic distortion(THD) analysis of inverter output current and grid voltage is done using Matlab tool. The grid voltage THDs are around 3% due to



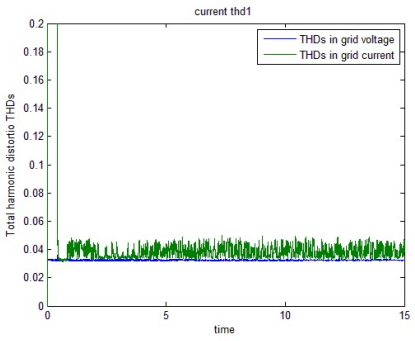

(a) Three phase inverter current.



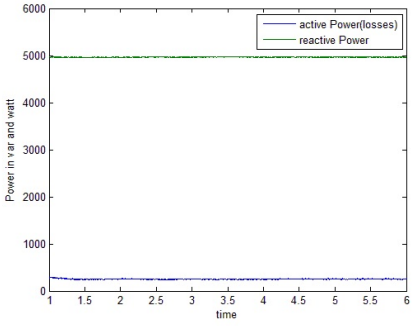

(b) $I_d$ and $I_q$ currents.

Figure 5-8: Three phase and $I_q$,$I_d$ currents of inverter.

heavy nonlinear loads. The inverter output current harmonics are 4% in average. The current & voltage THDs and reactive power output of inverter in shown in Fig.5-9.




(a) Grid voltage and current THDs.




(b) Inverter output power.

Figure 5-9: Voltage and current THDs & inverter output power.

**Case:2 (Step change in reactive power demand)**

In this case, first reactive power reference of $2.5kvar$ is give to the inverter and at time $t = 16s$ reactive power reference is switched to $5kvar$(rated power). The response of inverter current to change in reactive power demand is shown in Fig.5-10 As shown in Fig.5-11a the DC link voltage is approximately equal to reference value ($650VDC$) with small fluctuation , but when reactive power reference changed at time $t = 16s$, a small dip is observed in DC link voltage although it settled to its reference value. The Fig.5-11 shows the change in $I_q$ current and DC link voltage.

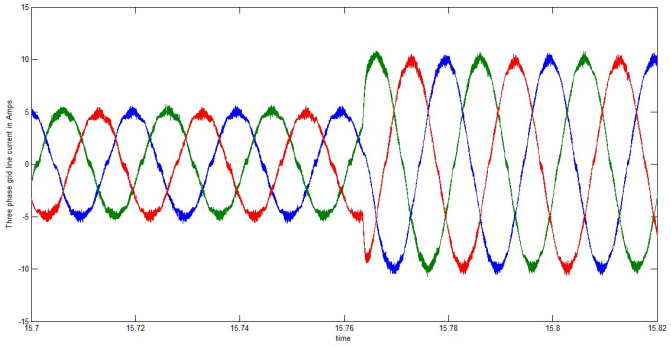
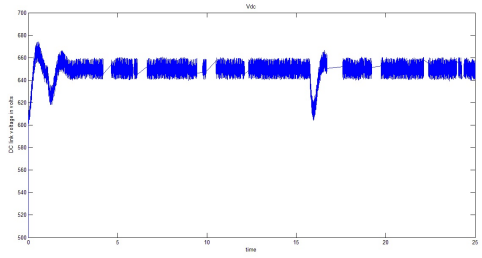
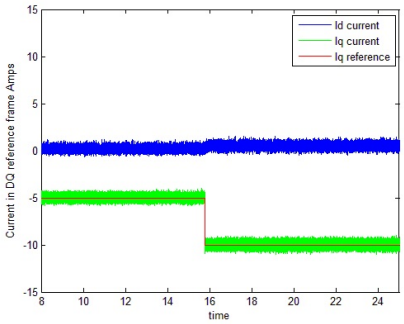



Figure 5-10: Inverter output current response.



(a) DC link voltage.




(b) $I_d$ and $I_q$ currents.

Figure 5-11: DC link voltage & $I_q$ current.

**Case:3 (Rated leading $kvar$ to rated lagging $kvar$)**

In this test case, the inverter power reference is switched from rated leading reactive power($5kvar$) to rated lagging reactive power($-5kvar$). The inverter line currents are shown in Fig.5-12.

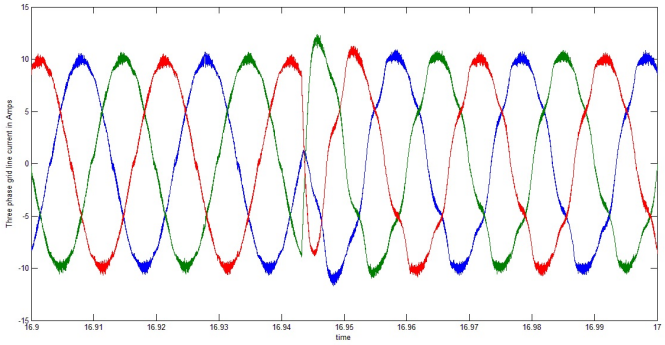
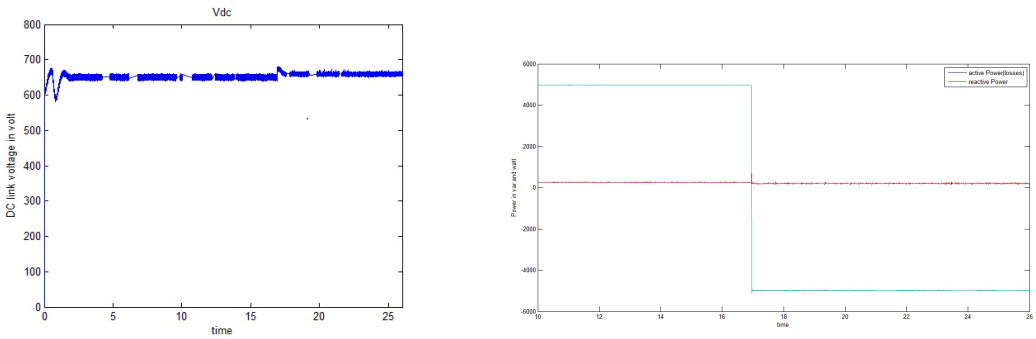



Figure 5-12: Inverter three phase output current.

When reactive power reference changed at time $t = 16.94s$, the DC link voltage rise above its reference value but after small transient it settle down to reference value as shown in Fig.5-13a. The inverter output active and reactive power is shown in Fig.5-13b




(a) DC link voltage. (b) Active and reactive power.

Figure 5-13: DC link voltage & active and reactive power.

### 5.2.2 STATCOM experimental results

In this section the complete system is tested within its design limits. The reactive power controller of STATCOM is given with the reactive power reference. Which compensate reactive power demand by generating reactive power reference for inverter and capacitor banks. Following are the test cases performed on STATCOM:

**Case:1 (Reactive power controller test)**

In this case different reactive power references are give to STATCOM to evaluate its performance. First Reactive power set point of $19kvar$ is given at time $t = 4s$ , two capacitor banks are switched ON that provides $15kvar$ and inverter supply $4kvar$ (see Fig.5-15).

At time $t = 10s$ the reactive power reference is changed to $12kavr$, This requirement can be fulfilled with one capacitor bank and the inverter reference set to $4.5kavr$, but as STATCOM minimize the capacitor bank switching, therefore two capacitor banks keep in service and the inverter provides $-3kvar$.

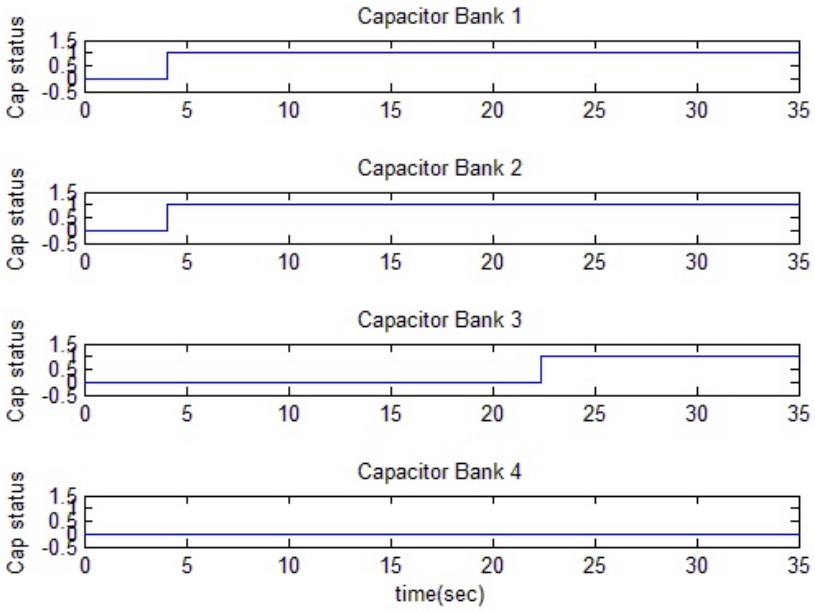



Figure 5-14: Capacitor banks status.

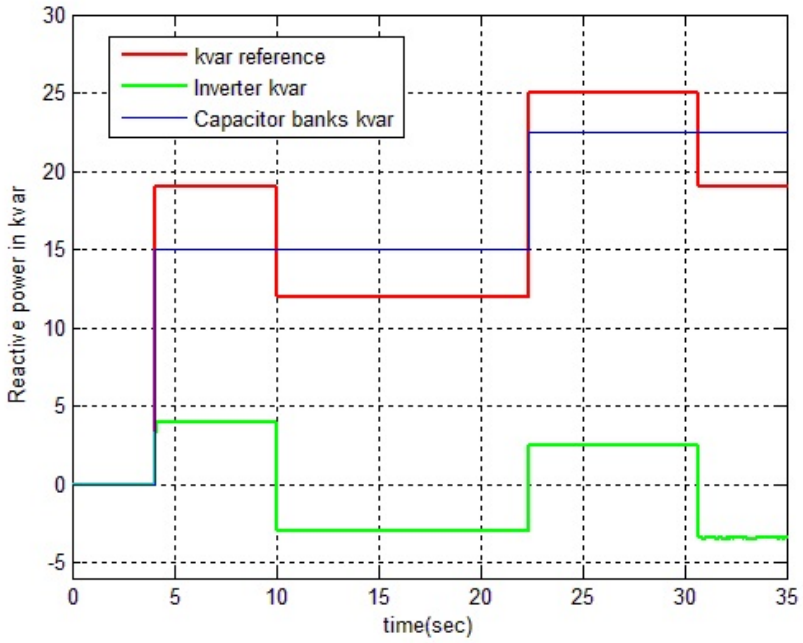



Figure 5-15: *kvar* output of capacitor bank & inverter.

**Case:2 (Minimizing capacitor bank switching)**

This test case verify the simulation study results of STATCOM.

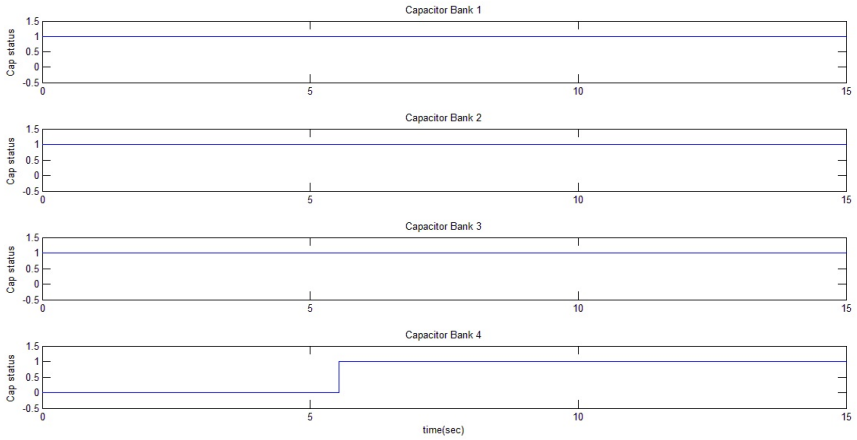



Figure 5-16: Capacitor banks status.

Reactive power reference of $26kvar$ is applied at time $t = 0.00s$(see Fig.5-17), the reactive power controller switch ON three capacitor banks(see Fig.5-16) to provide $22.5kvar$, remaining reactive power ($3.5kvar$) is delivered by the inverter(see Fig.5-17).

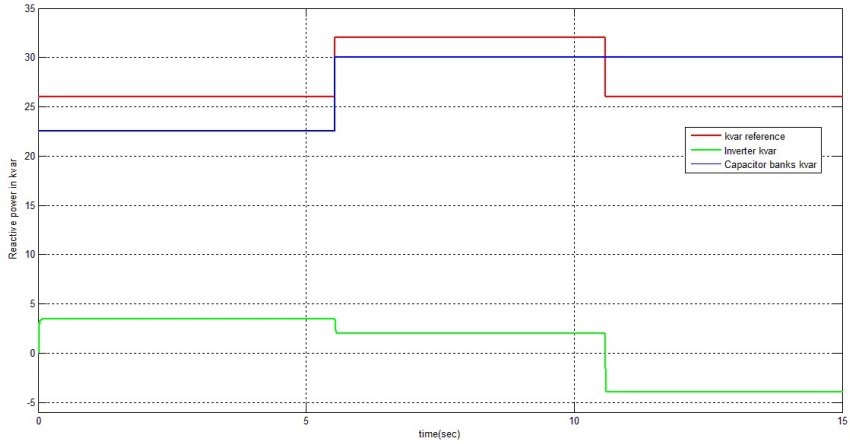



Figure 5-17: *kvar* output capacitor bank & inverter.

At time $t = 6s$ reactive power reference is changed to $32kvar$, the reactive power

controller switch ON four capacitor banks to provide $30kvar$ (see Fig.5-17), remaining reactive power ($2kvar$) is provided by the inverter.

At third instant $t = 11s$, reactive power reference again changed to $26kvar$ (see Fig.5-17), according to previous calculation three capacitor bank should be switched ON, but reactive power controller check the previous state of capacitor banks in service that was four, therefore to minimize the capacitor bank switching reactive power controller keep four capacitor banks in service to provide $30kvar$ and inject lagging reactive power $-4kvar$ from the inverter (see Fig.5-17) to fulfill reactive power demand.

# Chapter 6

# Conclusion and Future Work

## 6.1 Conclusion

Hybrid three phase grid-tied STATCOM is implemented to control the power factor in low voltage distribution network. The prototype performs intelligent control to minimize the capacitor banks switching events that increases the life of hardware with better dynamic performance. Hybrid STATCOM inverter also achieve IEEE standards for current harmonics in low voltage system. This report include design and analysis of STATCOM with simulation and experimental results, that successfully realize the objective of this research work.

The hybrid STATCOM system for low voltage application is first simulated in MATLAB simulink, after testing the system with different operational scenarios the experimental prototype is implemented using SEMIKRON inverter and OPAL RT-lab hardware in loop testing platform. The system is able to achieve the design specification. Though, there are possibilities of further improvements in this system, which are discussed in next section.

## 6.2 Future work

Following are the future scope of work:

* The control system is designed and tested on OPAL RT-lab platform, research

work can be done to implement the control on a micro-controller that fulfill industrial standards.

∗ The inverter used is the prototype is SEMIKRON Electronics Teaching System, further reach work can be done to replace the inverter with industrial grade inverter with specially design heat sink to operate at high ambiance temperature.

∗ The standalone STATCOM protection relay, independent of computer based control.

∗ Advance virtual damping techniques can be implemented that automatically tunned itself according to grid impedance variation(make system independent of grid conditions).

∗ Grid fault detection with grid fault ride through.

∗ The extra capability can be added to the inverter, to remove unbalance and harmonics from the grid when reactive power demand from inverter is at its minimum (operate as active filter).

# Appendix A

## A.1 Reference frame transformation

### A.1.1 *abc* to *dq* transformation

The sinusoidal signals are transformed in to *dq* reference frame using below equations:

$V_d = 2/3(V_a * sin(wt) + V_b * sin(wt - 2pi/3) + V_c * sin(wt + 2pi/3)$

$V_q = 2/3(V_a * cos(wt) + V_b * cos(wt - 2pi/3) + V_c * cos(wt + 2pi/3)$

$V_0 = 1/3(V_a + V_b + V_c)$

### A.1.2 *dq* to *abc* transformation

The *dq* reference frame signals are transformed in to *abc* sinusoidal signals using below equations:

$V_a = V_d * sin(wt) + V_q * cos(wt) + V_o$

$V_b = V_d * sin(wt - 2pi/3) + V_q * cos(wt - 2pi/3) + V_o$

$V_c = V_d * sin(wt + 2pi/3) + V_q * cos(wt + 2pi/3) + V_o$

### A.1.3 *abc* to $\alpha\beta$ transformation

The sinusoidal signals are transformed in to $\alpha\beta$ reference frame using below equations:

$V_\alpha = 2/3V_a - 1/2V_b - 1/2V_c$

$V_\beta = \sqrt{3}/2V_b - \sqrt{3}/2V_c$

$V_0 = 1/3(V_a + V_b + V_c)$

## A.2 DQ reference frame current control

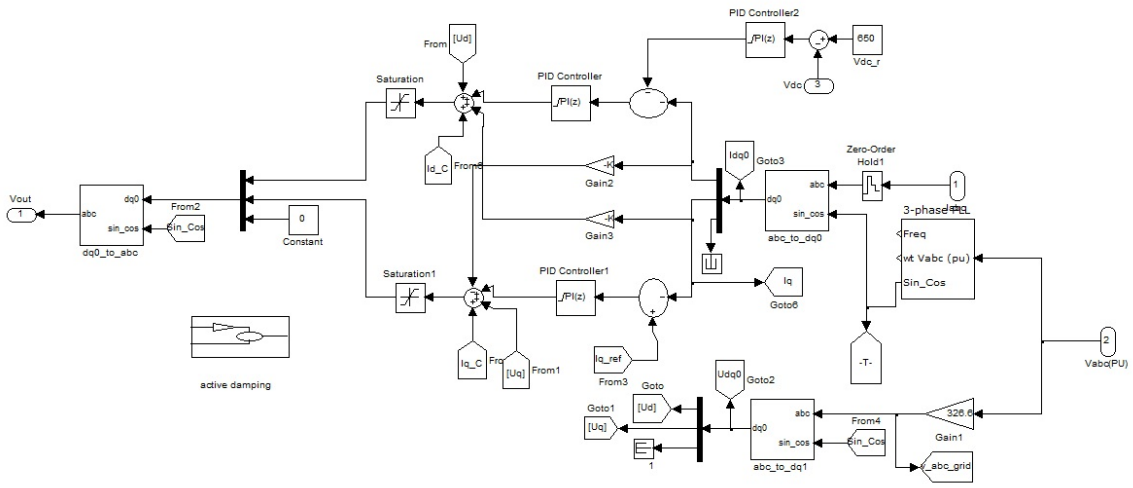



Figure A-1: DQ reference frame current control.

## A.3 SVPWM block

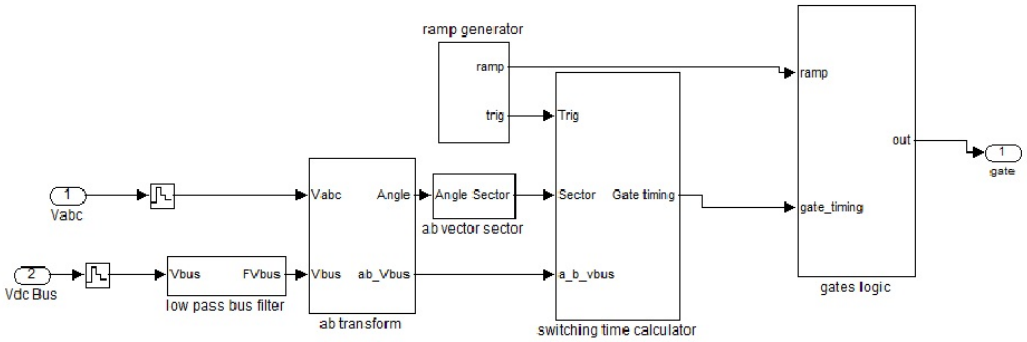



Figure A-2: SVPWM block.

## A.4 Reactive power controller

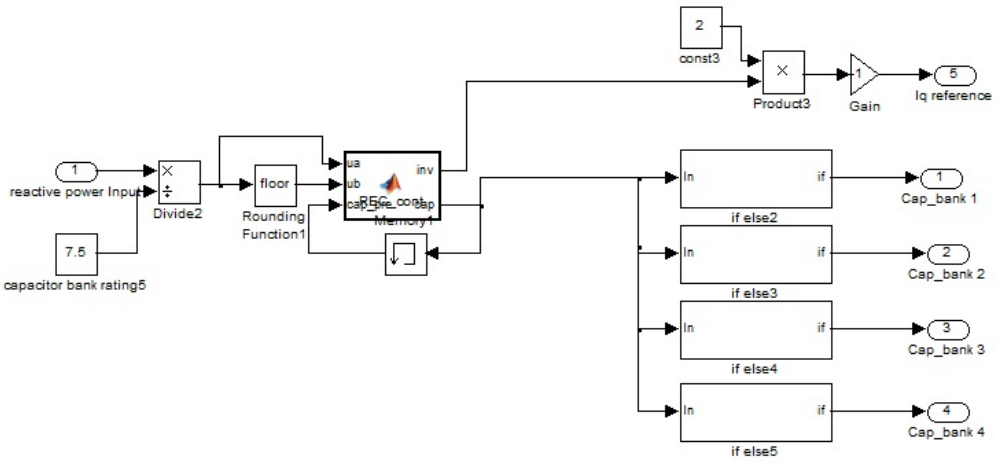



Figure A-3: Reactive power controller.

### A.4.1 Reactive power controller code

```
function [inv,cap] = REC_cont(ua,ub,cap_pre)

output_a=0;
cap_count=0;
u1=ua;
u2=ub;

if(cap_pre~= 0)% check the previous status of capacitor banks
    limit1=cap_pre*7.5+5;
    limit2=cap_pre*7.5-5;
    limit=cap_pre*7.5;
    Qref= ua*7.5;

    if(Qref<limit1)
         if(Qref>=limit2)
             cap_count=cap_pre;
             u1=0;
             u2=40;
             output_a=(Qref-limit);

         end
    end
end

if (u2 < 35)

    if (u1 < 0.66) %if reference is in just inverter rating
        output_a= u1*7.5;
    end
    if (u1 >= 0.66)% if reference is greater then inverter rating
        if (u1 >= 1)
           output_a= (u1-u2)*7.5;
           cap_count=u2;
        end
        if(u1<1)
            cap_count = cap_count+1;
            output_a= (u1*7.5)-7.5;
        end

    end
end

inv=output_a;
cap=cap_count;

end
```

Figure A-4: Reactive power controller code.

## A.5 RT-Lab workbench model

### A.5.1 Model for RT-Lab workbench

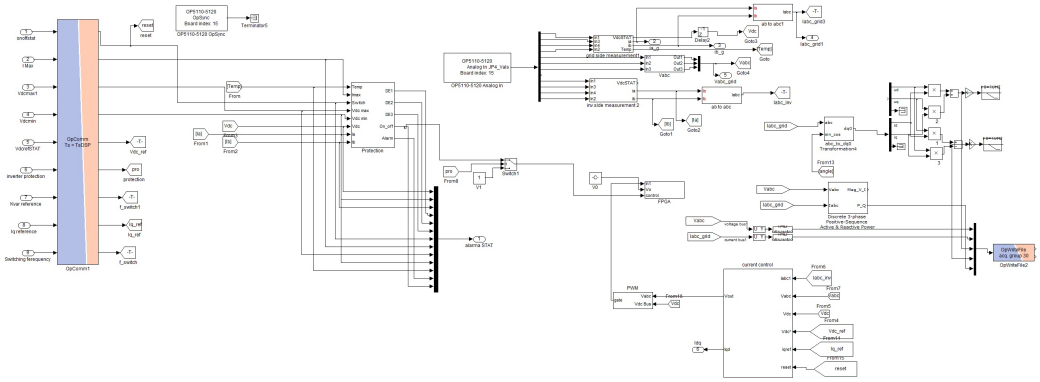


Figure A-5: Model for RT-Lab workbench.

### A.5.2 Inverter protection block limits

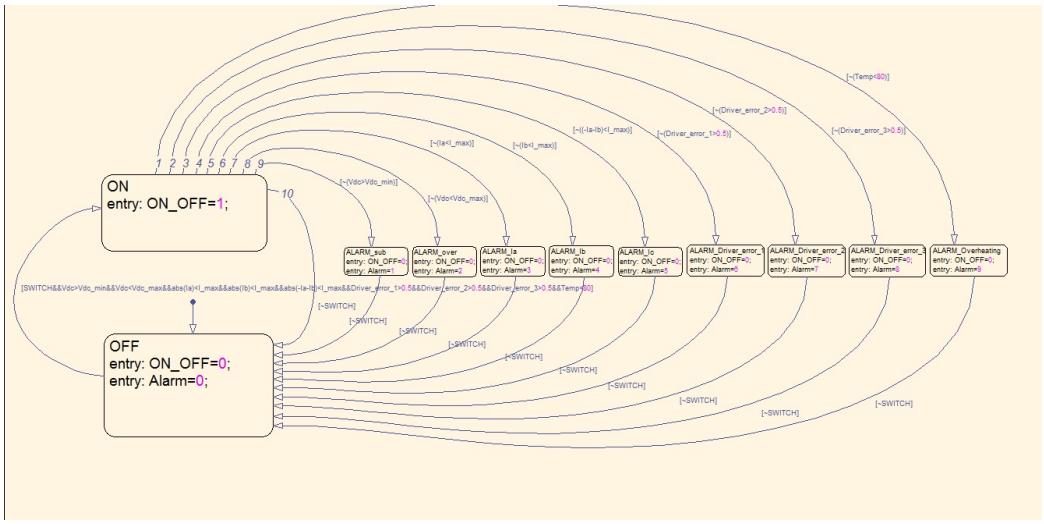



Figure A-6: Inverter protection block limits.

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