Design and Implementation of the Control of an MMC-Based Solid State Transformer

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***Abstract*— Implementation of the control of a Solid State Transformer (SST) is described in this paper. The SST topology considered is derived from a Modular Multilevel Converter (MMC), in which the cells have the capability to transfer (inject or drain) power. The MMC is combined with an isolation stage formed by Dual Active Bridges (DABs) and a DC/AC power converter. The resulting modular multiport power converter can connect both high voltage and low voltage AC and DC ports, providing isolation between the high voltage and the low voltage terminals, and with full control of the power flow. Implementation of the control of this power converter is not trivial, due to the large amount of power devices and sensors involved, and to the complexity of the control algorithms. Furthermore, the need to provide isolation among the different stages adds further concerns mainly related with cost. This paper discusses the configuration, selection of the required hardware, as well as implementation aspects for the control of the proposed SST topology.**

Keywords—Solid State Transformer (SST), Modular Multilevel Converter (MMC), centralized control, distributed control, FPGA

I. INTRODUCTION

Industrialized countries have turned their energy policies towards a reduction of the dependence on fossil resources due to environmental concerns, limited resources and the uncertain and progressive increase of their cost. Massive integration of renewable as well as maximum efficiency have become a priority. This scenario has pushed the development of innovative solutions based on high-power, high-voltage electronics power converters, like HVDC (High Voltage Direct Current), FACTS (Flexible AC Transmission Systems) and SST (Solid State Transformer), able to cope with these challenges [1].

Conventional transformers represent a key element in the power transmission system. Although it is a relatively cheap and well stablished technology, power system operation is demanding innovative and challenging new requirements, such as power quality improvements (i.e harmonics, reactive power and imbalances compensation), power flow control and a reduction of transmission losses, among others. Solid State Transformers based on power electronics devices, have the potential to manage these new functionalities, while fulfilling its main objective: connecting two AC systems providing galvanic isolation [2].

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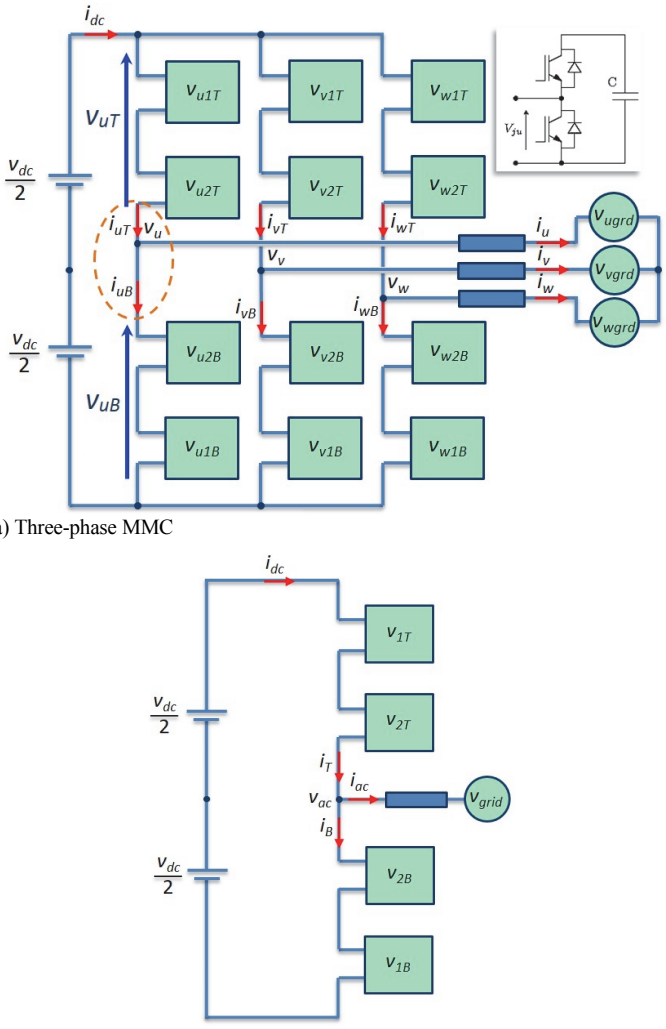


a) Three-phase MMC

b) Complex vector equivalent circuit

Fig. 1. a) Three-phase MMC, with the cells consisting of a half bridge. b) Complex vector equivalent cirtuit. For the sake of clarity, the arm inductances are not shown.

The Modular Multilevel Converter (MMC) is a promising DC/AC multilevel power converter topology subject of extensive research nowadays. It was first introduced one decade ago [3],[4]. Fig. 1a shows the schematic representation of a three-phase MMC. The physical cells forming each arm of the power converter typically consist of a half bridge and a capacitor. While it shares the advantages of conventional multilevel topologies (i.e. reduced size of filters, lower switching

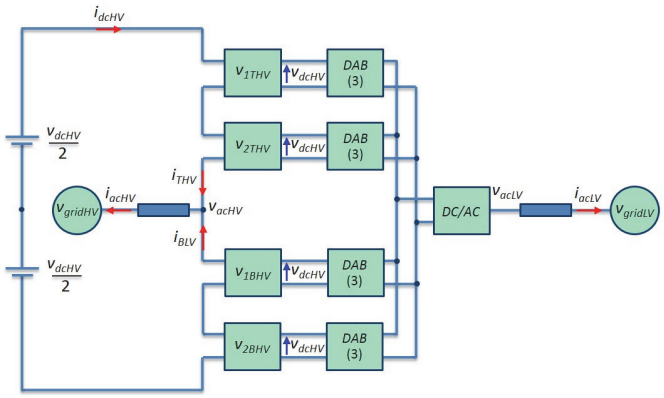


Fig. 2. MMC based multiport power converter MMC with serialized input-parallelized output.

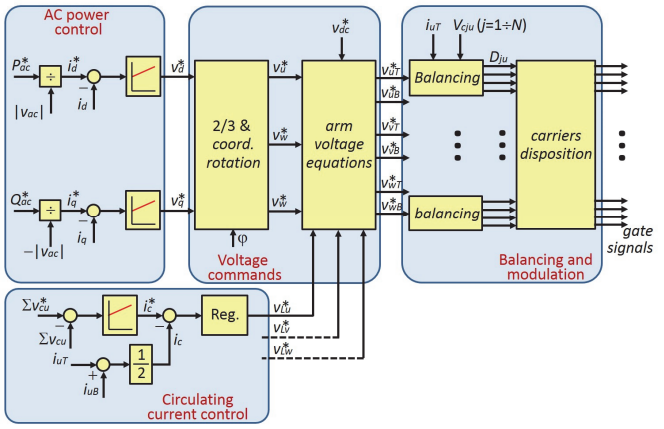


Fig. 3. Control of the MMC.

losses, capability of withstanding large terminal voltages using relatively lower voltage power devices), it also provides some attractive features such as modularity, easy scalability and distributed energy storage, therefore eliminating the need of a bulk DC capacitor [3],[4].

The MMC in Fig. 1a explicitly shows the three phases. It is possible to use a complex vector notation to represent the AC quantities (voltages and currents) of the MMC. The equivalent MMC with complex vector cells is shown in Fig. 1b [11].

It is possible to modify the MMC to transfer power at the cell level, providing new potential features such as distributed energy storage [5],[6],[7], integration of distributed energy resources at the cell level [8],[9],[10] and multiport power converters combining the high/low voltage AC/DC ports. Furthermore, multiport power converters based on the MMC topologies could provide the desired functionalities of the SST, i.e. connection of two AC systems, including galvanic isolation and full control of the power flow [11],[12] (see Fig.2). However, construction and control of the MMC based SST places significant challenges, due to the large number of power devices and sensors involved [22]. Either centralized or distributed control strategies can be used, each having advantages and disadvantages. Selection of a suitable implementation requires a thorough evaluation of the computational requirements and hardware requirements (number of input/outputs, optical fiber requirements for isolation, analog to digital channels, communications, …), as well as the existing digital control devices that can be used to realize the control.

This paper addresses the selection and implementation of the digital control of a MMC based SST, which is characterized by a large number of power devices and sensors, and large computational requirements due to the complexity of the control algorithms. Section II briefly describes the power converter topology. Section III addresses the requirements for the control of the two main stages: MMC and isolation stage using Dual Active Bridges (DABs). Alternatives for the implementation of the control are discussed in Section IV. Selection of the control hardware, implementation of the control and communications are presented in section V, VI and VII respectively. Experimental results are provide in Section VIII, Section IX summarizes the conclusions.

II. Proposed SST Topology

Fig. 2 shows the configuration of MMC based SST. For simplicity, the MMCs in the figure uses only two cells per arm (N=2). However, all the discussion following can be extended to any value of N without loss of generality. The topology of Fig. 2 is seen to combine a MMC (left side) with an isolation stage using DABs. In this figure, the left-side of the power converter will be considered as the high-voltage (HV) side. The right side of all the DABs in each leg (low voltage side), are connected in parallel. A conventional DC/AC power converter (e.g. two level or multilevel NPC, FC, …) can be used to connect with the LV AC grid.

It is noted that the power converter in Fig. 2 explicitly shows three ports: high voltage DC, high voltage AC and low voltage AC. A low voltage DC port also exists, but will not be used. This means that the power transferred by the DABs needs to be equal to the active power of the AC port in the low voltage side (losses neglected). This needs to be considered by the control algorithms.

III. Control Requirements

This section describes the control requirements for the different stages of the SST. This will be used later to assess the existing alternatives of its implementation.

a) Control of the MMC

Control of the MMC is challenging, as multiple control objectives need to be satisfied simultaneously. These include generation of the output AC voltage, control of the circulating current and balancing of the cells capacitors. Control and modulation strategies developed for MMC are basically aimed to balance the power between the AC and DC ports, which is performed by controlling the circulating current and by the balancing of the cell capacitor voltages [13].

Fig.3 shows a conventional control strategy. Active and reactive power commands are set in the high voltage AC side (see Fig.2 and Fig.3 “AC power control” block). By regulating the total capacitors voltage, the circulating current (i.e the DC current, neglecting harmonics) is trimmed to match the power between the DC and AC ports (Fig.3 – “Circulating current

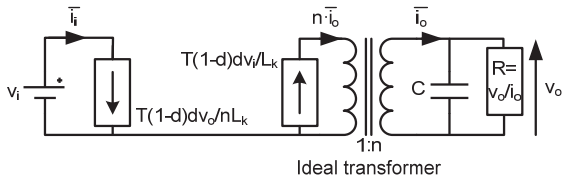


Fig. 4. Simple averaged model of the DAB.

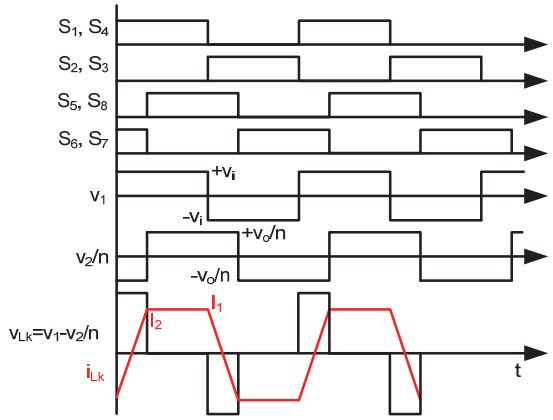


Fig. 5. Main operation waveforms of the phase-shift control method.

control" block). Simultaneously, the sorting algorithm selects the adequate cells that must be inserted/removed according to the individual cell capacitor voltages and the direction of the arm currents. Finally, a level shifted modulation strategy is responsible for generating the gate signals (Fig.3 – "Balancing and modulation" block).

As it can be noticed, control of the MMC implies a large amount of measurements and control signals. These include:

- Cell capacitor voltages (N x 3 x 2)
- DC current (1)
- Arm currents (6)
- AC currents (3)
- AC voltages (3)

It is noted that both the DC current of the MMC and the AC currents can be obtained from the measured arm currents. However, redundant current sensors are often used to enhance the accuracy and reliability. Typical sampling frequencies can be in the order of a few kHz.

b) Control of the DAB

The DAB converter was originally proposed in [3] and [15], and analyzed in more detail in [16],[17]. It is a bidirectional DC/DC converter with galvanic isolation based on two active bridges interfaced through a high-frequency transformer.

In the MMC-based SST shown in Fig.2, all the DABs are commanded to transfer the same amount of power at each MMC cell. The easiest way to control the DAB is by switching each full bridge (FB) using complementary constant pulse-width modulated signals with a 50% duty cycle, as shown in Fig.4. Using this modulation, a high-frequency square-wave voltage signal is generated at the transformer terminals ($\pm v_i$, $\pm v_o$). Considering the presence of the known leakage inductance of the transformer and controlling the transistors of both full bridges, the two square waves can be properly phase-shifted to regulate the power flow. These two phase-shifted signals (v_1 and v_2) generate a voltage (v_{Lk}) in the leakage inductance (L_k) of the transformer and a certain current (i_{Lk}) flows through it. This current is controlled by the phase shift between the primary and secondary voltages of the transformer (v_1 and v_2) [16],[17].

An averaged equivalent circuit of the DAB can be easily obtained [18], the input and output average current being (1) and (2), where d is the phase-shift, T is the semiperiod, and n the transformer ratio. Fig. 5 shows a simplified average model of the DAB.

$$\bar{i_i} = \frac{(1-d)dTv_o}{nL_k} \tag{1}$$

$$\bar{i_o} = \frac{(1-d)dTv_i}{nL_k}. \tag{2}$$

To design a feedback loop that ensures stable operation of the DAB, the small-signal dynamic model of the DAB must be considered. A simplified small-signal model of the DAB is proposed in [18] using the well-known averaged techniques presented in [19] and [20]. In this model, the output voltage variations due to variations in both the phase shift and the input voltage have the same characteristics as a first-order system response (the dynamic response of the converter is mainly determined by the value of the output capacitor and the load).

c) Control of the active rectifier on the LV side

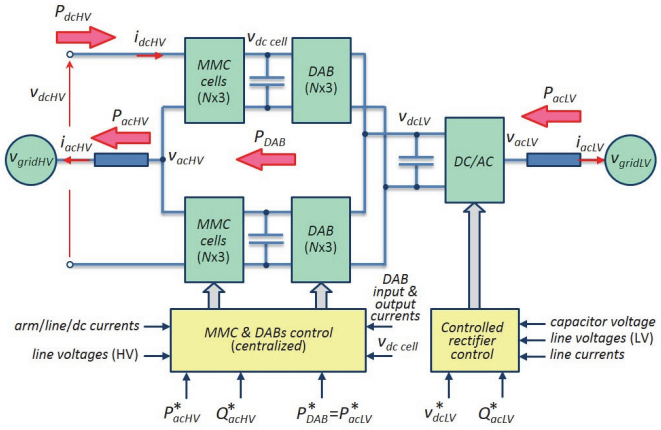
The LV DC/AC converter is controlled as a conventional active rectifier, where the commands are the DC link voltage and the reactive power at the LV AC side. The active power is therefore controlled to maintain the DC link capacitor voltage at its commanded value [23]. Control requirements for the low voltage DC/AC power converter are almost negligible compared to the requirements for the control of the MMC and DABs stages, and will not be further discussed in this paper.

IV. Control Structures: Centralized vs. Distributed Control

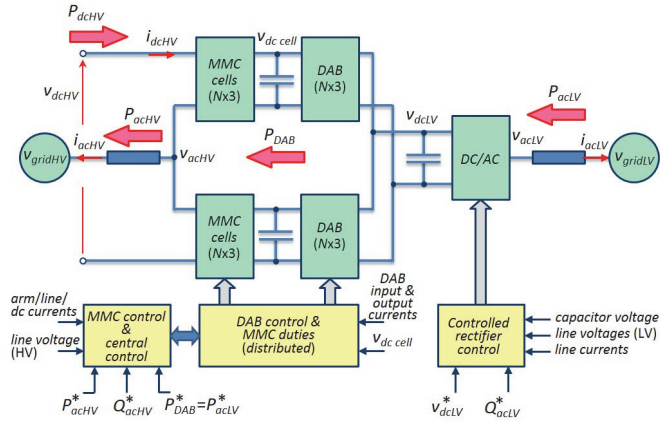
This section discusses potential implementations for the control of the SST. The two cases considered are a fully centralized control –in which a central controller measures all the variables and controls all the power switches of the MMC and DABs–, and a distributed control –in which a central controller measures some variables and executes the main converter control algorithms, but each MMC cell/DAB has a dedicated local control. Both cases are discussed following.

a) Centralized control

In a centralized control topology, one single processing unit is responsible of the control of both the MMC cells and the DABs. This is schematically shown in Fig. 6a. In this configuration, the aforementioned processing unit will have to manage the acquisition of every voltage and current sensor signal by means of a high enough number of AD converters and generate the corresponding gate signals sent to the drivers. Therefore, this topology requires a very large number of



a) Centralized control



b) Distributed control

Fig. 6.- Implementation using a) a centralized control and b) a distributed control

TABLE I. CENTRALIZED VS. DISTRIBUTED CONTROL: INPUT-OUTPUT REQUIREMENTS OF THE CENTRAL CONTROL

		Centralized control	Distributed control
Number of ADC channels	MMC variables	12	12
	DAB variables	3×3×2N = 18N (72 with N=4)	– (*)
Number of signals for communications	To/from MMC ADCs (No OF needed)	20	20
	To/from DAB ADCs (OF)	(4+3)×3×2N = 42N (168 with N=4)	– (*)
	To/from slave FPGAs (OF)	–	3×2=6 (communications optical fiber rings)
Number of signals for the drivers	To/from MMC (OF)	3×3×2N = 18N (72 with N=4)	– (*)
	To/from DAB (OF)	6×3×2N = 36N (144 with N=4)	– (*)
I/O ports	Without OF	20	20
	With OF	(42+18+36) N = 96N (384 with N=4)	6
	Total	20+96N (404 with N=4)	20+6

Notes: (*)This functionalities will be implemented in the distributed control
OF stands for Optical fiber

input/output ports. Most of them will be connected via optical fiber transmitters and receivers, since it is necessary to maintain electrical isolation. Table I summarizes the hardware requirements, they are assessed later in this section.

In addition to the hardware requirements, the computational requirements for the control unit are extremely high, as it has to implement both the control algorithms of the MMC and of all the DABs described in sections III-a and III-b respectively. It is also noted that these control algorithms operate with rather different sampling periods, a few kHz for the MMC and in the range of several tens of kHz for the DABs typically, what adds further challenges to their implementation in a single digital device.

b) Distributed control

In a distributed solution, control is split between a master/central control unit in charge of the MMC control algorithms and several slave processing units, each in charge of one DAB and its corresponding MMC cell. This is schematically shown in Fig. 6b. This topology allows a reduction of the number of input/output ports, also the computational burden of the central processing unit is significantly reduced. Moreover, since the slave devices are integrated in the DABs, the electrical isolation requirements for the sensors and drivers are lessened, reducing the count of optical fibers and shortening the length of those which are still necessary.

For the distributed control, it will be necessary to define a bidirectional communication between the central and slave devices. The central unit will send to the slave devices the commands for the power that each DABs has to transfer, as well as the corresponding duties for the MMC cells. The bandwidth for this communication is modest, as it does not need to transmit gate signals with precise timing. On the other hand, the slave units will send to the central unit through this link the measured cell capacitor voltages. These are needed by the central unit to realize the balancing of the MMC cell capacitors.

Table I summarizes the input/output requirements for the central control unit for the case of a centralized and a distributed control. The table includes the number of A/D channels which are needed to measure currents and voltages at different stages of the converter; number of lines for communications; number of lines to communicate with the drivers which control the power transistors. It is observed from this figure that, for the case of a SST with N=4, i.e. four cells per arm in the MMC (which is a modest amount), a total number of 384 optical fiber connections are needed, in addition to 20 cable connections (do not need isolation). It must be remarked in this regard that all the gate signals for both the DABs and the MMC cells come from the central control unit. On the other hand, the number of optical fiber connections is reduced to 6 for the case of the distributed control, where gate signals for each DAB and MMC cell are locally generated by the slave units.

Based on the preceding analysis, a distributed control has been selected. For the central control unit, a high performance System on Chip (SoC) will be used. For the slave units, low cost FPGAs are used. Discussion on the selection of the central control unit and slave units is presented in the next section.

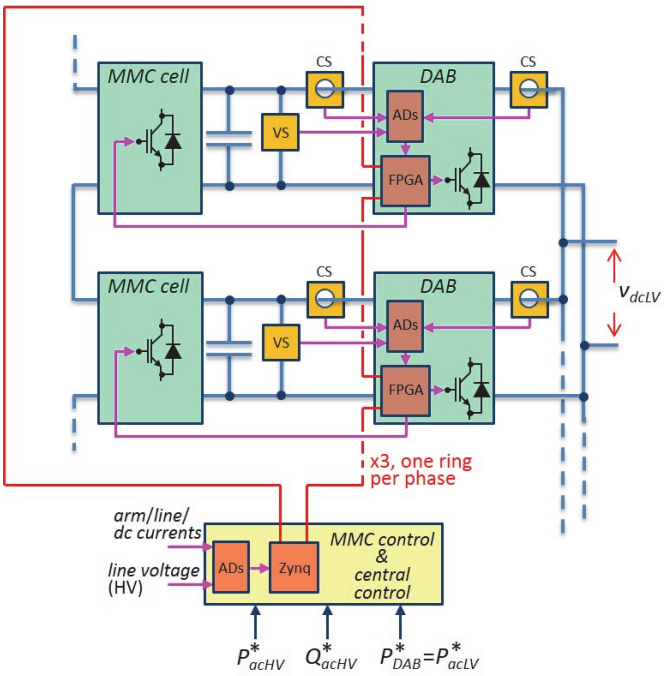


Fig. 7.- Overview of the distributed control. VS and CS stand for voltage sensor and current sensor respectively.

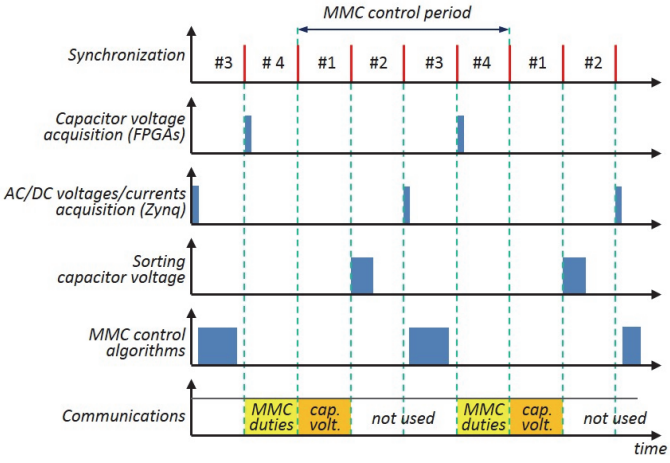


Fig. 8.- Timing diagram showing the different tasks needed for the SST distributed control, including communications

V. Selection of the Control Hardware

Fig. 7 shows the block diagram of the partially distributed control. The central control has medium processing requirements, the number of input/output signals being modest. These computational requirements could be met by high performance DSP type digital signal processors. For the implementation shown in Fig. 7, a Xilinx's Zynq-7000 SoC has been used. It comprises a dual core ARM processing system highly integrated with a FPGA. A Z-7020 device in a 200 I/O FPGA pins package has been chosen. It is noted that the I/O resources of the Zynq-7000 are significant higher than the actual needs for the implementation shown in Fig. 7. The reason for this selection is that the Zynq-7000 is currently being used to implement the control of conventional MMCs.

A low cost FPGA Spartan 3E 250K by Xilinx has been selected for the control of the DABs and generation of MMC cells gate signals. The current and voltages needed by the external control loops of the MMC are measured by two eight channel parallel bus 12 bit AD converters managed by the Zynq-7000. This requires a total of 20 non-optical fiber lines between the converters and the central control, 12 of them being the data bus and the remaining 8 being control signals, with the electrical isolation being provided by the sensors themselves (see Table I).

VI. Communications

The use of a distributed control system requires a communication network able to provide the bandwidth demanded by the control. As already mentioned, communication between the central control unit and the slave FPGAs will be bidirectional: the central control unit will transmit duty cycle values to the distributed control units, while the distributed control units will transmit the measured cell capacitor voltages to the central control unit, which are needed for balancing of the MMC cell capacitor voltages. The switching frequency of the MMC has been established in 5 kHz. Consequently, the information acquired by all the slave control units has to be transmitted in less than 200 μs.

The use of optical fiber is mandatory due to isolation requirements. Point-to-point communication is disregarded, due to the complexity and cost of the hardware. Ring configurations are therefore targeted. Each node in the ring will include one low-cost emitter and one receiver. The length of the optical fiber is also reduced, as the distance among DABs is significantly smaller than the distance between the DABs and the central control unit.

Considering the described scenario, a serial communication protocol using an optical fiber ring was considered advantageous. A modified version of TosNet protocol [21] was selected, as it can be fully implemented in the FPGAs with no need of additional hardware. In addition, TosNet is a master-slave isochronous protocol, which allows to coordinate the operation of all of the nodes by means of an internal deterministic synchronization signal (synchronization signal in Fig. 8).

The implemented protocol supports up to sixteen nodes. Three separate optical fiber rings will be used, one for each phase (see Fig. 7). Each ring consists of eight slave nodes, which correspond to the FPGAs in each DAB (four cells per arm, i.e eight cells per leg), and one master node, which is implemented in the central control unit. The central control unit is responsible for generating the synchronization signal, and consequently for the synchronization of the overall control process.

TosNet makes use of a shared memory block, which is transmitted to all of the nodes in the ring in every network cycle. In the proposed configuration, each of the slave nodes has assigned two sixteen-bit register of the memory block. The first register contains the MMC cell duty cycle; it is written by the central control and read by the slave FPGA. The second register contains the MMC cell capacitor voltage; it is written by the slave FPGA and read by the central control.

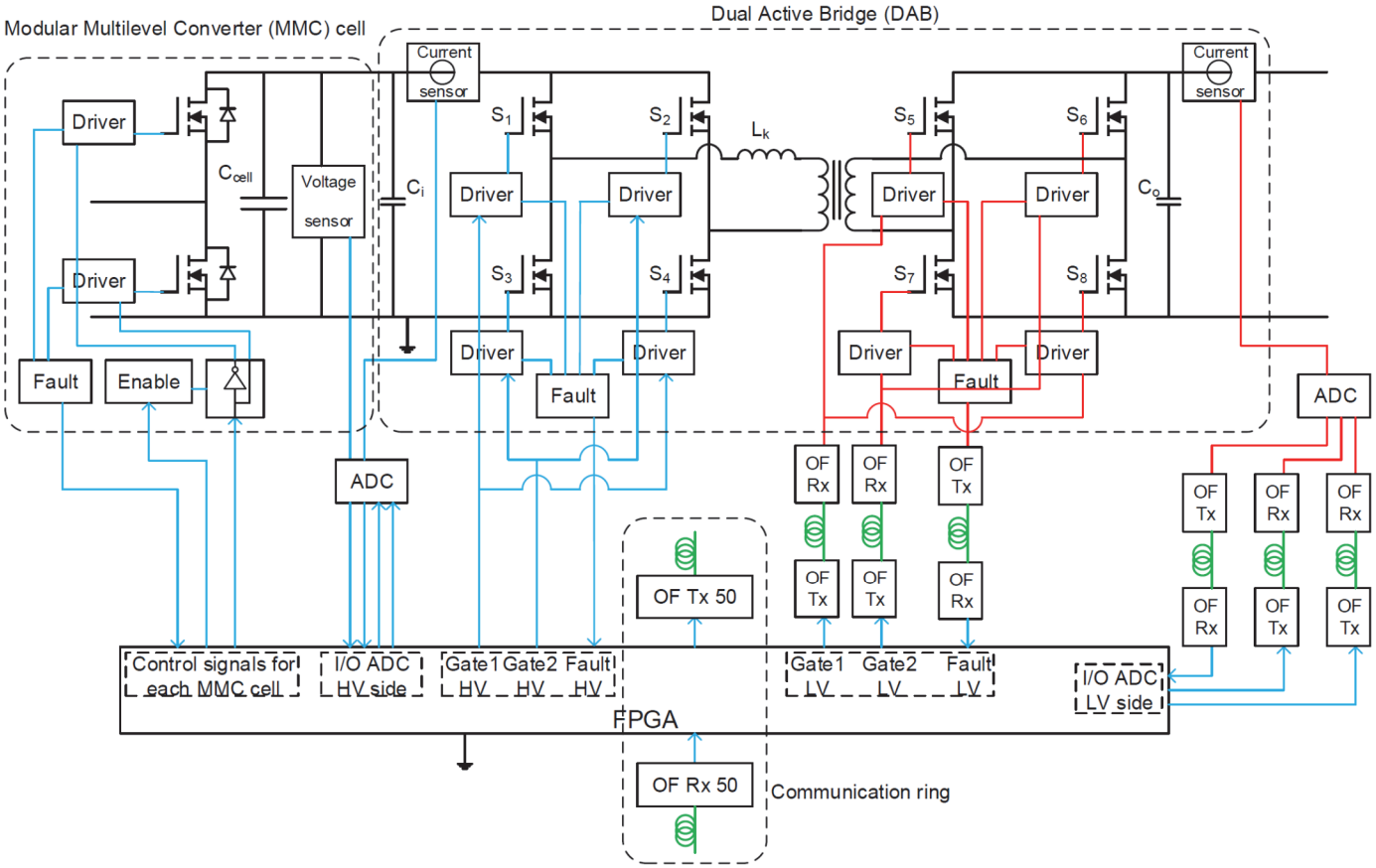


Fig. 9.- Detailed MMC cell and DAB, including sensors and control signals to/from drivers. "Of" stands for optical fiber.

Fig. 8 shows the timing diagram with the different tasks needed for the SST distributed control. The sampling period of the MMC is synchronized with the communications period, each MMC sampling period consisting of four communications periods (#1 to #4 in Fig. 8). In each communication period, the memory block containing the MMC cells duties and the cells capacitors voltage is transferred to all the elements in the ring (central control and slave FPGAs). However, the content of the memory block is only updated/read at well defined instants of time of the control process. The overall process works as follows:

- Communication period #4 (see Fig. 8): Cell capacitor voltages are acquired by the slave FPGAs. MMC duties to be applied to each MMC cell for the next control period are received by the slave FPGAs through the communications ring. Cell capacitor voltages transferred through the communications ring are not used.
- Communication period #1: Cell capacitors voltages are transferred by the slave FPGAs to the central control through the communications ring. Duties transferred through the communications ring in this period are not used.
- Communication period #2: Capacitor voltages are sorted by the MMC central control. Information transmitted through the communications ring is not used.
- Communication period #3: MMC AC and DC terminal voltages and currents are acquired. This occurs at the center of the MMC control period, therefore reducing the switching harmonics in the sampled AC currents. After this, the central control executes the control algorithms of the MMC. As a result, the duties for the MMC are available to be transferred during the next communication period (#4). Information transmitted through the communications ring is not used.

VII. Implementation of the Distributed Control

Fig. 9 shows a detailed block diagram of a generic MMC-based SST cell, including MMC cell and DAB. The central control unit (SoC) is responsible for the acquisition of the MMC terminal current/voltage measurements (DC and AC ports), implementation of the outer level control loops, and synchronization of the communications ring.

The slave FPGAs mounted in each DAB control the gate signals for both the DAB and MMC cell power switches, and measure the current and voltage signals needed for the control of the DAB current and MMC cell DC voltage. It is observed from Fig. 9 that the FPGA is located in the high voltage side of the DAB. The voltage sensor of each cell and the current sensor in the high voltage side of the DAB are connected to the corresponding ADC, which is directly connected to the FPGA (no isolation is needed). On the contrary, the current sensor in the low voltage side of the DAB requires an isolated ADC. Three optical fibers are needed for the communication between the FPGA and the low voltage side ADC.

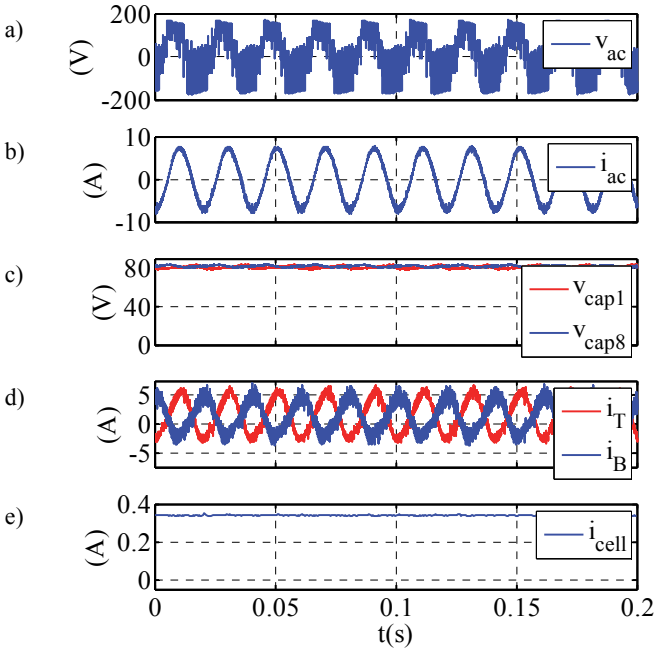


Fig.10.- Experimental results. a) AC voltage, b) AC current, c) capacitor voltage of two cells, d) top and bottom arm currents, and e) current transferred by the DAB

The driver signals for the power switches in the primary of the DAB are directly connected to the FPGA. Optical fiber is used to provide the required isolation between the FPGA and the secondary of the DAB. Two gate signals are required to control the four power switches used by each full bridge of the DAB.

The gate signals for the MMC cell half-bridge are calculated by the FPGA from the duty commands received from the MMC central control through the communications ring. Three signals are used to connect the FPGA with the MMC cell:

- Gate signal. Using this gate signal and analog circuitry, two complementary PWM signals are generated to control the two power devices of the cell.
- Enable signal. Open all the switches of the MMC in case of failure, or previously to the DAB turn off.
- Fault signal. Is sent by the drivers to the central control whenever an anomalous condition is detected.

Finally, only two fiber optic lines are required for the communication ring connecting the central control and the slave FPGAs. To fulfill bandwidth of the communication protocol, the selected optical fiber can operate up to 50MBd. However, the rest of signals transmitted using optics fiber (gate signals, fault signals and ADC signals) can use a reduced bandwidth (up to 1MBd), thus enabling a cheaper optical fiber.

VIII. Experimental Results

Fig. 10 shows the experimental results obtained with a scaled prototype using the proposed SST concept and decentralized control strategy. The experiments were realized using a single phase MMC. Fig. 10a and 10b show the phase currents and voltages of the AC side of the MMC. Fig. 10c and 10d show two MMC capacitors voltages, and the top and bottom arm currents. Finally, Fig. 10e shows the current transferred by the DAB. As described in the preceding sections, the central control unit implements the control loops of the MMC shown in Fig. 3, while the DAB low cost FPGA shown in Fig. 9 controls the DAB current.

IX. Conclusions

This paper has described the implementation of the control of a modular solid state transformer. Configuration of the control, selection of the control hardware, and communications requirements have been addressed. A distributed control, with the central control using a high performance Zynq device and the local controls using a low cost Spartan FPGA, combined with a TosNet protocol for the communication, has been shown to be a viable solution, meeting the control requirements at a reasonable cost.

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