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Active input current shaper without electrolytic capacitor for retrofit lamps applications

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***Abstract* -- The evolution of solid-state lighting technology has transformed traditional solutions in lighting. High-Brightness Light-Emitting Diodes (HB-LEDs) have become very attractive light sources due to their excellent characteristics, namely high efficiency, a long lifetime and low maintenance. It is evident that HB-LED drivers must be durable and efficient in order to enjoy these advantages. Moreover, to replace incandescent bulbs, the ac-to-dc HB-LED driver must be simple and have low-size and comply with international regulations (i.e., injecting low frequency harmonics into the mains supply). With the last modifications regarding low power lighting equipment (i.e. < 25W), authors have traditionally focused their efforts on increasing efficiency by sacrificing sinusoidal input current, yet all their solutions obviate the suppression of the traditional electrolytic capacitor of ac-to-dc converters, highlighting that this is the price to pay for a simple and low-size solution. This paper, however, puts forward the design of a simple and low-size ac-to-dc HB-LED driver for retrofit lamps without an electrolytic capacitor in order to extend its lifetime. The solution proposed here derives from a well-known technique used in the past, the Active Input Current Shaper (AICS), but without an electrolytic capacitor in this case. If the electrolytic capacitor of an AICS is removed, then low frequency ripple arises at its intermediate dc bus, adding some distortion in the line input current over the proper natural one of an AICS. However, this addition is slight in comparison to the proper natural distortion of AICSs. Moreover, the low frequency ripple at the intermediate bus is not transferred to the output with the help of the rapid output dynamic response of AICS, which prevents flicker. The paper presents a theoretical analysis that guarantees a compromise between compliance with international regulations and the use of capacitor technologies other than the electrolytic design. Finally, a 24 W experimental prototype has been built and tested to validate the theoretical results presented in this paper.**

***Index Terms*— Ac-to-dc power conversion, harmonic distortion, LEDs, lighting, power factor, switched mode power supplies.**

I. INTRODUCTION

High-Brightness Light-Emitting Diodes (HB-LEDs) are now recognized as a rapidly emerging technology, considered the true alternative to many mature technologies (i.e., incandescent bulbs, compact fluorescent lamps, etc.) due to their high efficiency, low maintenance and durability. To enjoy these advantages, however, HB-LED drivers must be both durable and efficient.

As HB-LEDs are diodes, the default method for driving them is to control the dc forward current through this semiconductor device. If the primary energy source is the ac line, then some type of ac-to-dc converter must be placed between the line and HB-LEDs. Furthermore, the low-frequency harmonic content of the line current must comply with specific standards (IEC 61000-3-2 [3-6] and the ENERGY STAR® program [7]). Traditionally, as these regulations establish a very strict harmonic content for lighting (e.g. IEC 61000-3-2, Class C), only sinusoidal line waveforms are able to comply with these standards. Therefore, the only practical method to comply with these regulations is to use active high Power Factor (PF) converters. These converters, known as Power Factor Correctors (PFCs), constitute expensive, complex solutions. Two year ago, there was a modification for lighting equipment with power levels lower than 25 W. At this point compliance with the IEC 61000-3-2 standard becomes more relaxed due to the fact that now low-power luminaries (i.e. < 25 W) must comply with it but applying limits of Class D and not Class C [6]. Hence, new solutions can arise.

A possible application for replacing incandescent bulbs lamps is to use two strings of around 10 x 1 W HB-LEDs in parallel connected to the output of an ac-to-dc driver to produce the same luminance flux as that produced by a 100 W incandescent bulb. These configurations supply output voltages of around 20 V and power levels below 24 W. The most widespread solution is to use a flyback converter operating in Discontinuous Conduction Mode (DCM) with switching frequencies below 100 kHz in order to obtain efficiencies of around 82 %. With the last modifications regarding low power lighting equipment (i.e < 25 W), authors have traditionally focused their efforts on increasing the efficiency by distorting the line input current of the ac-to-dc driver despite the increase in its cost and complexity. Some examples are solutions based on an asymmetrical half bridge flyback converter

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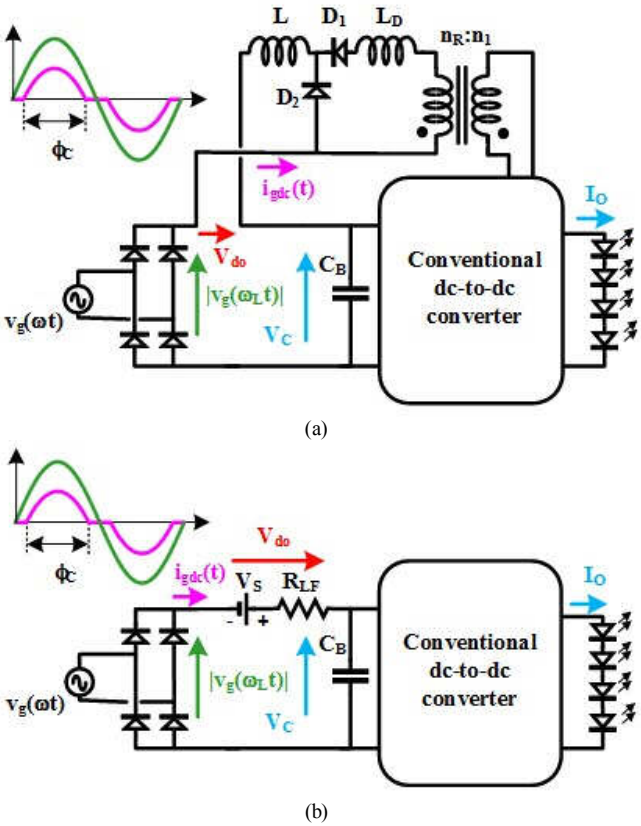


Fig. 1. a) AICS solution. b) Equivalent circuit of an AICS.

[8], two stage resonant buck converter [9] or tapped-inductor buck converter [10-11]. However, all these proposals exhibit a major drawback: the use of an electrolytic capacitor to reduce the low frequency ripple of the output current reducing the lifetime of the equipment.

This paper presents a simple and low-size ac-to-dc HB-LED driver based on a well-known concept, namely the Active Input Current Shaper (AICS). The proposal of this solution arises from the latest modifications of the regulations for low power lighting equipment (i.e., IEC 61000-3-2:2014 [6], Class D for < 25W), which are now more relaxed than previous standards (i.e., IEC 61000-3-2:2010 [5], Class C for < 25W), no longer requiring a sinusoidal input current. AICS are topologies that recycles some amount of power from the output to the input of the converter in order to shape the line input current. Thus, they presents a natural distortion of the line input current which depends on the amount of power recycled (the larger value of power recycled the more sinusoidal input current and the lower efficiency). To carry out this natural operation of AICS, an electrolytic capacitor is needed to stabilize its intermediate bus. AICS. If the electrolytic capacitor is replaced by another technology that leads to a decrease in its capacity, then some low frequency ripple arises in the intermediate bus, thus adding some distortion over the proper natural one of line input current of AICS. However, this added distortion is slight in comparison to the natural one of AICS. Moreover, due to the help of its rapid dynamic response, the low frequency ripple is not fully transferred to the output from the intermediate bus. As a result, an ac-to-dc HB-LED driver for retrofit lamps applications without an electrolytic capacitor (i.e. with extended lifetime) and no flicker is achieved which complies with regulations.

With this goal in mind, the present paper is organized as follows. Section II reviews the basic concepts of AICS applied to the flyback family of converters. In Section III, the experimental results of a 24 W AICS prototype without low frequency ripple in the intermediate verifies the conclusions of the review in Section II. Moreover, in Section III, the electrolytic capacitor is removed from the AICS prototype, allowing low frequency ripple in the intermediate bus. As a result, the distortion of the line input current due to the low frequency ripple in the intermediate bus is negligible compared to the distortion naturally generated by the operating of the AICS. Section IV presents a static analysis of the AICS with low frequency ripple in the intermediate bus, including the modelling of input current distortion and its analysis in order to verify the conclusions drawn from the experimental results. Finally, Section V concludes the paper.

II. A REVIEW OF ACTIVE INPUT CURRENT SHAPERS (AICS).

A. Basic concepts of AICS

The concept of the AICS is very well known in the design of ac-to-dc Switching Mode Power Supplies (SMPS), [14-18]. This solution is based on conventional dc-to-dc converters, with a slight modification: an additional output, obtained from the converter transformer (Fig. 1a), is connected between the diode bridge and the bulk capacitor (CB).

This output, called "delayed output" in [12], was proposed in the context of two fully regulated outputs in dc-to-dc converters [13]. Although it seems similar to a conventional forward output, an extra inductor (L_D) is placed between one terminal on the secondary side transformer and the diode D_1 (Fig. 1a). With this extra inductor and with L working in Continuous Conduction Mode (CCM, i.e., $L >> L_D$) or working in Discontinuous Conduction Mode with moderated decreases of L (DCM, i.e., $L > 2L_D$), the Thévenin equivalent circuit of the "delayed output" becomes a voltage source (V_S, see Fig. 1b) with a loss-free resistor in series (R_{LF}, see Fig. 1b). This "delayed output" recycles a certain amount of energy, redirecting it to the input in order to shape the line input current. The larger value of power recycled, the more sinusoidal input current and the lower efficiency, but by suitably choosing the values of these two elements (i.e., V_S and R_L), the AICS can achieve both high efficiency and a limited low-frequency harmonic content of the input current.

The current in a half cycle of input voltage can be easily deduced from the behavior of the AICS. The input rectifier starts to conduct when the input voltage (i.e., $v_g(t)=V_{gp}\cdot|\sin(\omega_L t)|$) reaches ($V_S$-$V_C$). Thus, the expression of the rectified input

current can be written as:

$$i_{gdc}(t) = \frac{V_{gp}\cdot|\sin(\omega_L t)| - V_C + V_S}{R_{LF}}, \quad (1)$$

where V_C is the voltage of the intermediate bus and ω_L and V_{gp} are the angular frequency and the peak value of input voltage, respectively. Note that this expression is only valid for the interval $[(\pi-\phi_C)/2, (\pi+\phi_C)/2]$, where ϕ_C is the conduction angle (see Fig. 1). By equating (1) to zero, the expression for the conduction angle can be easily calculated:

$$\phi_C = 2\cos^{-1}\left(\frac{V_C - V_S}{V_{gp}}\right). \quad (2)$$

Therefore, the line input current is defined by (1) within the $[(\pi-\phi_C)/2, (\pi+\phi_C)/2]$ interval and by zero outside of this positive semi-cycle interval of the line input voltage. Likewise, $i_g(t)$ is similarly defined for the negative semi-cycle of the line input voltage (see Fig. 1). Note that the higher the ϕ_C, the greater the amount of energy recycled to the input and therefore, the lower the efficiency.

From the expression of the input voltage, (1) and (2), the average input power will be:

$$P_g = \frac{1}{\pi}\int_{(\phi_C-\pi)/2}^{(\phi_C+\pi)/2}\left[i_{gdc}(t)\cdot V_{gp}\cdot|\sin(\omega_L t)|\right]dt = \frac{{V_{gp}}^2}{2\pi R_{LF}}\left(\phi_C - \sin(\phi_C)\right). \quad (3)$$

The rectified input current can be rewritten as a function of the average input power, conduction angle and peak value of the input voltage using (1), (2) and (3):

$$i_{gdc}(t) = \frac{2\pi P_g}{V_{gp}}\left(\frac{|\sin(\omega_L t)| - \cos\left(\frac{\phi_C}{2}\right)}{\phi_C - \sin(\phi_C)}\right). \quad (4)$$

Moreover, from (4), it is straightforward to obtain the minimum ϕ_C value complying with international regulations for a given input voltage and input power (i.e., the minimum ϕ_C which introduces higher efficiency). Table I shows these minimum values (i.e., ϕ_{Cmin}), which are the same for both American and European mains supplies. Some of these values have been previously calculated in [15, 18]. As can be seen in Table I, the more restrictive the standard, the higher the value of ϕ_{Cmin}. The input current of the AICS can now be represented. Figure 2 shows the normalized input current for several optimized designs that meet international regulations at nominal input voltage in addition to maximizing efficiency. All the designs in Fig. 2 were carried out following the optimized design procedure proposed in [15, 18].

TABLE I. MINIMUM VALUE OF ϕ_C COMPLYING WITH INTERNATIONAL REGULATIONS

	ϕ_{Cmin} (°)
EN 61000-3-2 Class C regulations	**140.49**
EN 61000-3-2 Class D regulations	**63.12**
ENERGY STAR® for commercial applications	**55.59**
ENERGY STAR® for residential applications	**103.87**

B. Implementation of the voltage source and the LFR with the forward "delayed output"

The analysis of the forward "delayed output" presented in [12] allows the calculation of V_S and R_{LF}. Figure 3 shows the

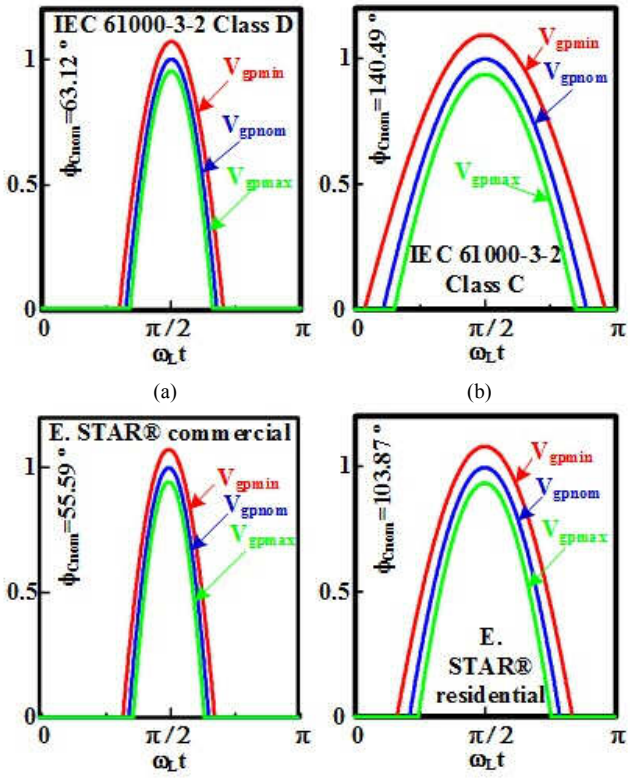


Fig. 2. Normalized input current for different optimized designs at different peak values of $v_g(t)$: a) Class D European design. b) Class C European design. c) ENERGY STAR® American design for commercial applications. d) ENERGY STAR® American design for residential applications.

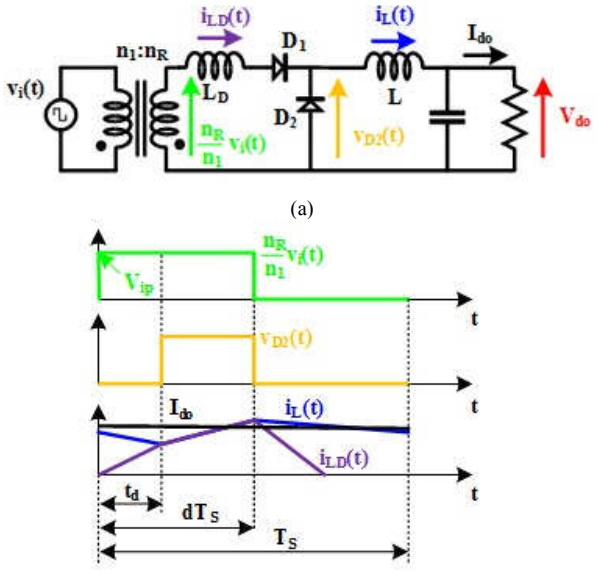


Fig. 3. a) "Delayed output". b) Main waveforms.

equivalent circuit of the "delayed output". As can be seen, it is a forward output, but with an additional inductor, L_D, in series with the rectifier diode, D_1. Due to the action of this inductor, there is a delay between the turn-off of D_2 compared to the traditional forward output. In fact, D_2 stops conducting later because L_D must be charged until $i_L(t)$ (i.e., when $i_{LD}(t)$ reaches

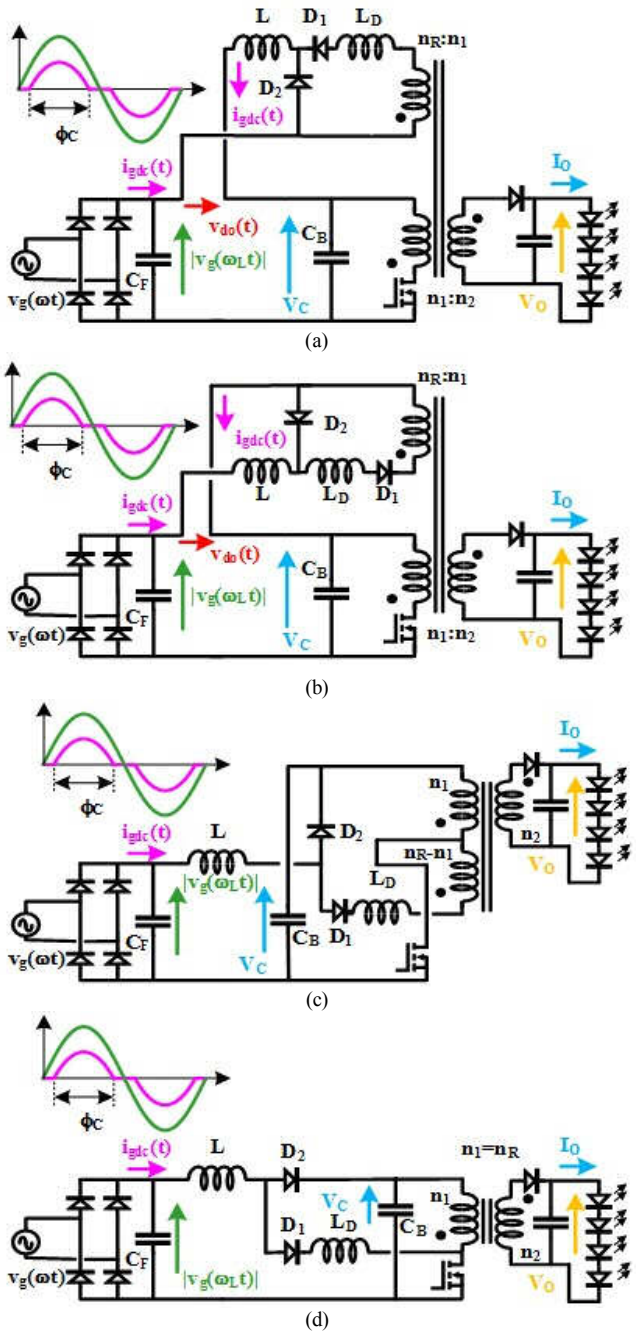


Fig. 4. Implementation of an AICS based on a flyback converter. a) Basic scheme. b) After moving L, L_D, D1 and D_2. c) Using an extra tap instead of "delayed output". d) Using no extra tap (n_1=n_R).

$i_L(t)$) via the action of the voltage reflected on the secondary side of the transformer of the forward "delayed output" (see Fig.3b).

From Fig. 3b, the delay time can be deduced by applying Faraday's law to the "delayed output":

$$t_d = \frac{i_L(t=t_d)}{\frac{n_R}{n_1} v_i(t)}, \quad (5)$$

where $v_i(t)n_R/n_1$ is the voltage reflected on the secondary side of the forward "delayed output", n_R/n_1 being the turns ratio of

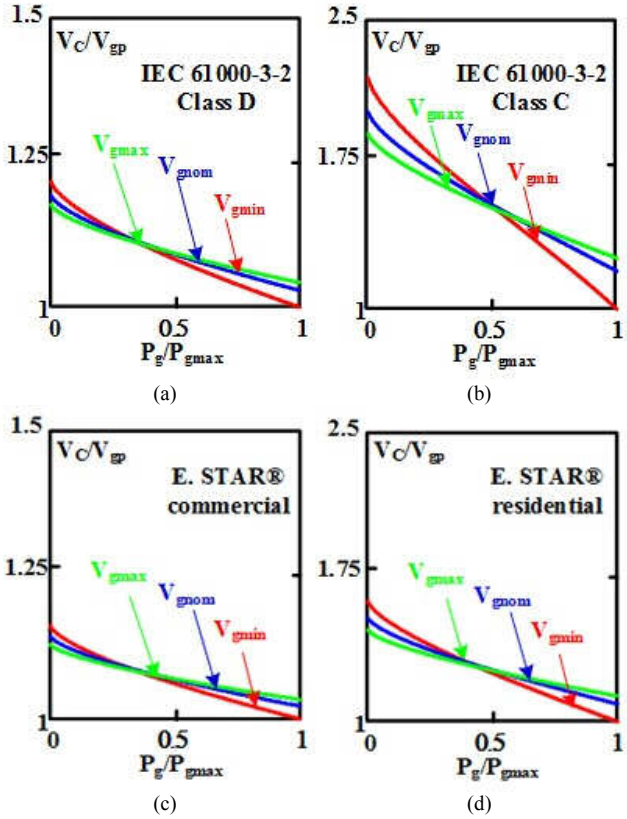


Fig. 5. Normalized voltage of the intermediate bus versus normalized power at different peak values of the input voltage for different optimized designs. a) Class D European design. b) Class C European design. c) ENERGY STAR® American design for commercial applications. d) ENERGY STAR® American design for residential applications.

the transformer. The effective duty ratio applied to the output LC filter can be deduced from Fig. 3b:

$$d' = d - t_d \cdot f_s. \quad (6)$$

where d is the duty cycle *and* $f_S=1/T_S$ is the switching frequency, T_S being the switching period.

Assuming that there is no ripple through inductor L (for the sake of simplicity) because the forward "delayed output" operates in CCM (i.e., $L>>L_D$), the output voltage of the "delayed output" is:

$$V_{do} = \frac{n_R}{n_1} \cdot V_{ip} \cdot d - L_D \cdot f_s \cdot I_{od}, \quad (6)$$

where V_{ip} is the peak value of $v_i(t)$ and I_{od} is the output current of the "delayed output". From Fig. 1, it can be deduced that the forward "delayed output" becomes a real source voltage. Equation (6) can thus be rewritten as follows:

$$V_{do} = V_S - R_{LF} \cdot I_{od}, \quad (7)$$

where:

$$V_S = \frac{n_R}{n_1} \cdot V_{ip} \cdot d, \quad (8)$$

$$R_{LF} = L_D \cdot f_s. \quad (9)$$

Note that no energy is dissipated in the R_{LF} if all the components are ideal. Finally, it should be stressed that the L_D energy is transferred to the primary side of the transformer; in this case, to the equivalent voltage source, $v_i(t)$.

C. *Using a flyback converter to design the AICS*

Figure 4 shows the implementation of an AICS in a flyback converter (it will be the same in any other member of the flyback family of dc-to-dc converters: SEPIC, Cuk and Zeta). First, Fig. 4a defines the basic implementation. Second, two modifications of this implementation are shown in Fig. 4b and Fig. 4c, where the transformer becomes an autotransformer. Fig. 4d shows a particularization of the solution shown in Fig. 4c. This is a straightforward implementation of AICS by using a flyback converter, ideal for simple and low-size solutions. The price to pay is the loss of a degree of freedom in the design, as the autotransformer disappears (i.e., $n_R=n_1$). Finally, this implementation only introduces two extra inductors and two extra diodes with respect to the traditional flyback topology.

By using a flyback topology to implement the AICS, the input voltage of the dc-to-dc converter becomes V_C. Taking into account CCM operation, the following equation can be written:

$$V_O = \frac{n_2}{n_1} \cdot V_C \cdot \frac{d}{1-d} \ , \tag{10}$$

where n_2 is the number of turns of the secondary side of the transformer. Moreover, Equation (8) becomes:

$$V_S = \frac{n_R}{n_1} \cdot V_C \cdot d. \tag{11}$$

As (11) shows, V_S depend on V_C, the duty cycle and the turn ratio of the "delayed output". In fact, suitably choosing n_R/n_1 allows us to set V_S freely. Moreover, V_C and V_S are related by the fact that the output voltage of the AICS must be kept constant by the action of the feedback loop. A new equation must now be deduced using (2), (10) and (11):

$$V_C - \frac{n_R}{n_1} \cdot V_C \cdot \frac{V_O}{\frac{n_2}{n_1} V_C + V_O} = V_{gp} \cdot cos\left(\frac{\phi_C}{2}\right). \tag{12}$$

From (3) and (12), the evolution of V_C as a function of the design parameters (i.e., the conduction angle for nominal conditions and full load, ϕ_{Cnom}, and the duty cycle for minimum peak value of the input voltage, d_{max}) can be calculated. V_C may be represented versus input power for different V_{gp} values. Figure 5 shows the voltage on the intermediate bus for different optimized designs following the design procedure in [16, 18] (the same as the designs in Fig. 2). The optimized design procedures in [16, 18] focused on minimizing the value of V_C and the amount of recycled energy, maintaining compliance with international regulations at nominal input voltage and full load. By suitably choosing n_R/n_1, the voltage drop across the series connection of V_S and R_{LF} could be zero at the minimum input voltage, V_{gpmin}, and full load, P_{gmax}. Under these conditions, V_C (i.e., V_{Cmin}) becomes equal to V_{gpmin}. Although V_C is minimized, it is not kept constant for different operating conditions (i.e., P_g and V_{gp} variations), at least if the flyback converter is operating at constant switching frequency, as can be seen in Fig. 5. This is the price to pay for the simplicity of this solution compared to a two-stage solution, in which the voltage across the intermediate bus is controlled, making no suitable regular AICS for wide input voltage range applications. Finally, it should be noted that, in the structure shown in Fig. 4d, V_C pre-limiting cannot be achieved due to the fact that n_R/n_1 is set *a priori*.

III. Experimental results: increasing low frequency voltage ripple of the AICS in the intermediate bus to eliminate the electrolytic capacitor

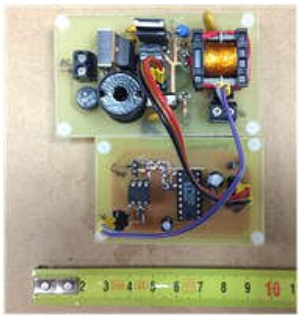
A prototype of the proposed ac-to-dc HB-LED driver based on an AICS (Fig. 6a) was designed to comply broadly with relaxed regulations (i.e., IEC 61000-3-2, Class D and ENERGY STAR® program requirements for commercial applications), subsequently built and tested. A design was carried out in line with [16, 18] for the following specifications: $\phi_{Cnom}=70º$, $P_{gmax}=24$ W, $V_O=19$ V, $f_S=110$ kHz (to provide a tradeoff between switching power losses and the size of the prototype), American design (i.e., $90\sqrt{2}<V_{gp}<130\sqrt{2}$ and 60 Hz), CCM operation of the "delayed output" (i.e., L=1,8 mH) and $d_{max}=0.6$. The circuit was designed according to the scheme shown in Fig. 6a, where R_{LF} = 43.45 (i.e., $L_D=0.39$ mH), $n_S=n_1$. The choice of the turns ratio of the transformer ($n_2/n_1=0.1$) is made according to a trade-off between current and voltage stress in both the power transistor and diode, providing a duty cycle range at full load from 0.35 to 0.45. The prototype was controlled using a commercial IC, as shown in Fig. 6b (UC2825 manufactured by Texas Instruments). Finally, the converter output was connected to a matrix of two strings of 6 HB-LEDs in parallel using a 1-ohm resistor per string to equalize currents. Table II summarizes all the main components.

TABLE II. Components of the experimental prototype

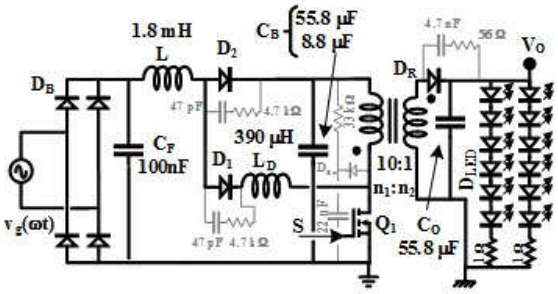
Fig. 6b and c reference	Value
D_1	BYP08P140
D_2	HFADBTB
D_B	3KBP04M
D_R	8TQ100
D_{Sn}	MUR4100
D_{LED}	LXK2PW14T00 (Luxeon)
Q_1	NDF10N60ZH
Q_2 and Q_3	BD140 and BD139
U_1	UC3825
U_2	MCT2

A. *AICS without low frequency ripple in the intermediate bus (C_B=55.8 μF)*

The prototype was tested until both its temperature and that of the HB-LEDs stabilized at the aforementioned specifications. The final operating temperature was reached after 45 min of operation. Figure 7a, b and c shows the line input current, voltage in the intermediate bus, input voltage and output voltage of the AICS and Fig.7d the drain to source voltage of Q_1 MOSFET. As expected, the experimental results of $i_g(t)$ match theoretical values. Furthermore, the voltage of the intermediate bus is between 150 v and 200 V (depending on V_{gp}), as expected. In this implementation, V_C cannot be pre-



(a)



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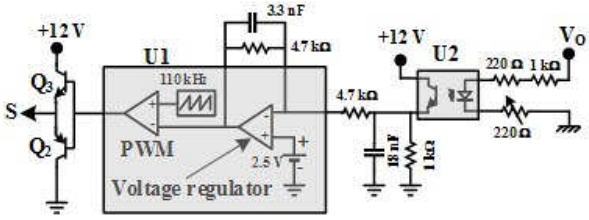


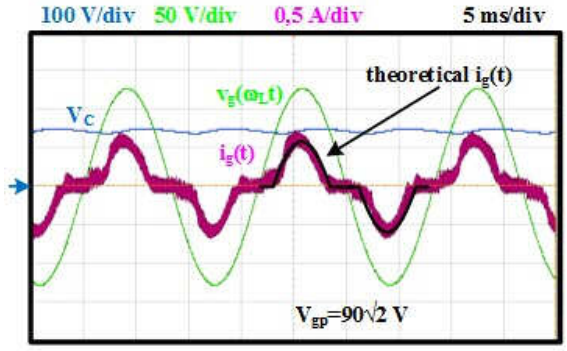
(c)

Fig. 6. Experimental prototype based on a flyback converter. a) Picture. b) Schematic of power stage. b) Schematic of the control stage.).

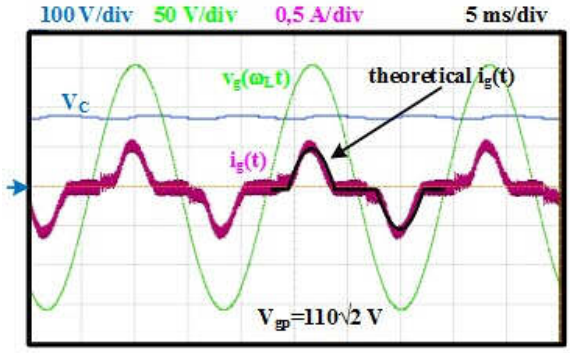
limited (i.e., $n_1=n_R$). However, this is the price to pay for using an implementation as simple as the one proposed here.

B. AICS with low frequency ripple in the intermediate bus (C_B=8.8 µF)

In this second test, the electrolytic capacitor of the intermediate bus (C_B=47 µF) has been removed and only the ceramic capacitor remains (C_B=4 x 2.2 µF). As a result, some low frequency ripple arises at the voltage of the intermediate bus (see $v_C(t)$ in Fig. 8), adding some distortion over the proper natural one of the AICS line input current (i.e. the input current is now not sinusoidal during the conduction angle and ϕ_C is neither centered around nor equidistant from $\omega_L t=\pi/2$). This added distortion seems slight in comparison to the proper natural distortion of AICS (see $i_g(t)$ in Fig. 8a, b and c). Also, Fig.8d shows the drain to source voltage of Q_1 MOSFET. Moreover, this slight increase in input current distortion can be explicitly checked in comparison to the first test in Fig. 9, where the experimental harmonic content of $i_g(t)$ is shown both for with and without an electrolytic capacitor. The experimental results corroborate the previous conclusion: the



(a)



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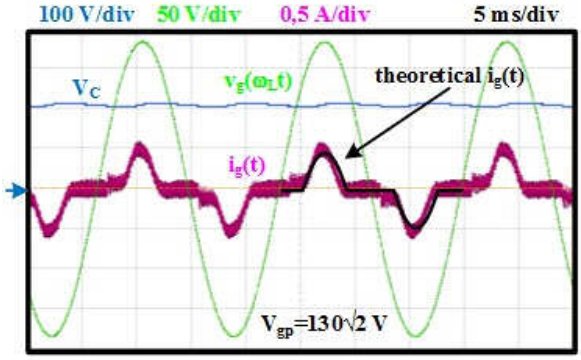
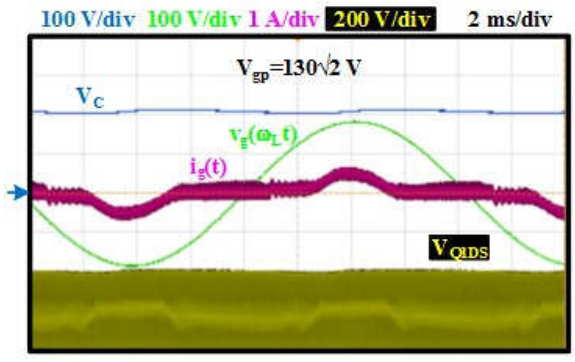


(c)



(d)

Fig. 7. Line input current ($i_g(t)$), voltage of the intermediate bus (V_C), line input voltage ($v_g(t)$) and output voltage (V_O) of the AICS without low frequency ripple in the intermediate bus: a) V_{gp}=90 V_{rms}. a) V_{gp}=110 V_{rms}. a) V_{gp}=130 V_{rms}. d) Drain to source voltage of MOSFET Q_1 (V_{DSQ1}).

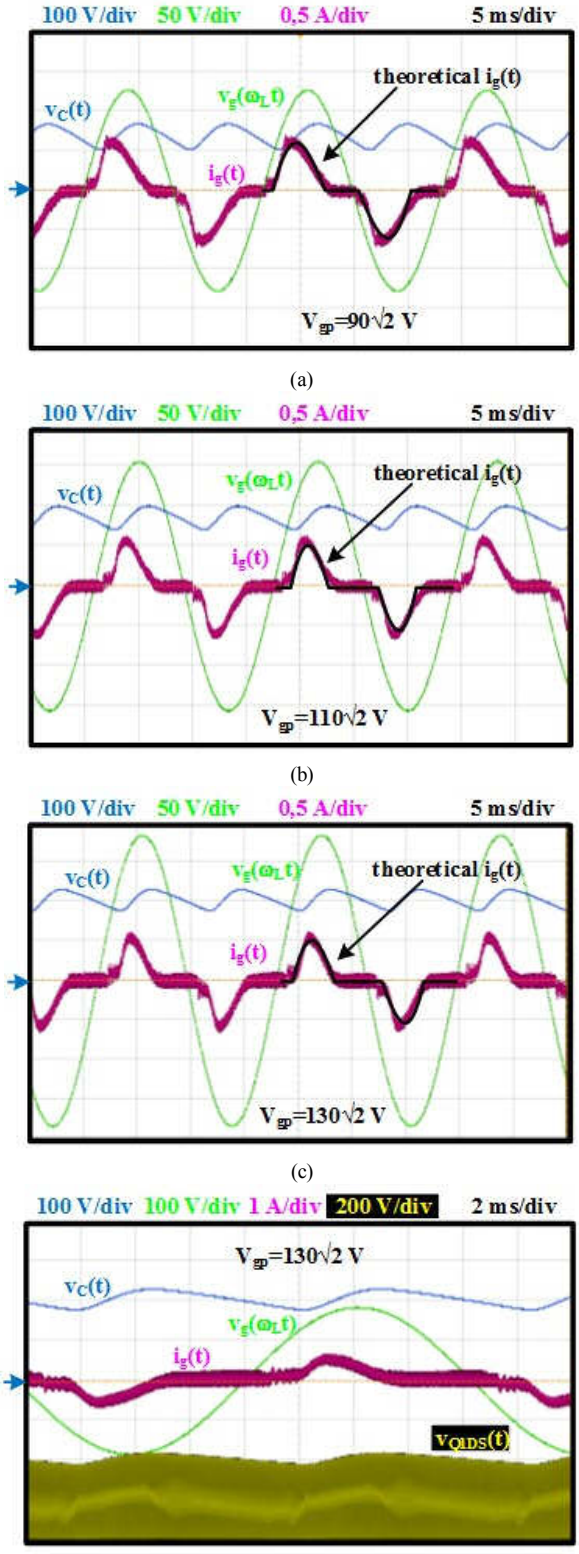


Fig. 8. Line input current ($i_g(t)$), voltage of the intermediate bus (V_C), line input voltage ($v_g(t)$) and output voltage (V_O) of the AICS with low frequency ripple in the intermediate bus: a) V_{gp}=90 V_{rms}. a) V_{gp}=110 V_{rms}. a) V_{gp}=130 V_{rms}. d) Drain to source voltage of MOSFET Q_1 (V_{DSQ1}).

added distortion by eliminating the electrolytic capacitor is negligible in comparison to the proper natural one. As a consequence of this, compliance with the IEC 61000-3-2 Class D international standard is likewise achieved. Table III also shows compliance with ENERGY STAR® program requirements for commercial applications and the slight increase in THD and slight decrease in PF.

Now the question is how the low frequency ripple of the intermediate bus is reflected at the output of the AICS. The answer is shown in Fig. 10. As can be seen, the low frequency ripple of the output voltage (V_O) and output current (I_O) is very low because of the contribution of the rapid output voltage feedback loop (Fig. 6b), which has been designed to eliminate flicker.

TABLE III. PF AND THD IN BOTH TESTS

TEST	Vgp (V_{rms})	PF	THD(%)
AICS without low frequency ripple in the intermediate bus (CB=55.8 µF)	90	0.905	50.10
	110	0.854	64.83
	130	0.83	66.71
AICS with low frequency ripple in the intermediate bus (CB=8.8 µF)	90	0.849	47.63
	110	0.812	57.49
	130	0.789	67.04

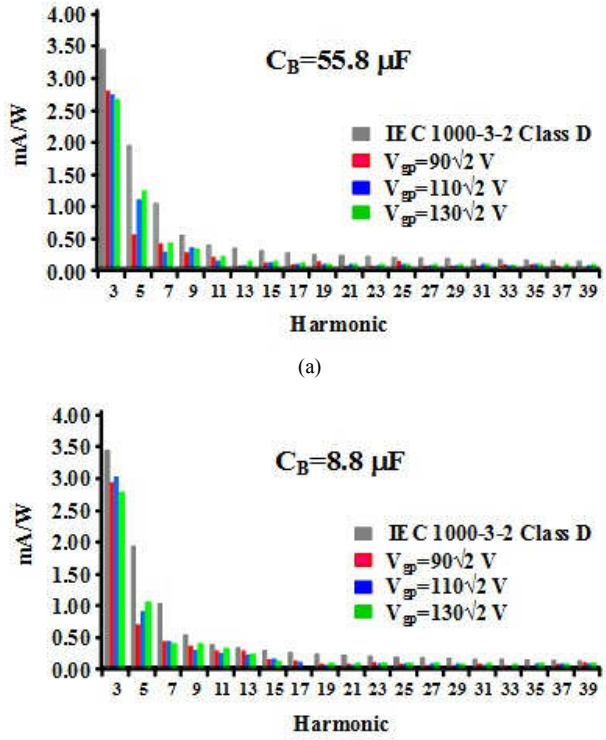


Fig. 9. Experimental harmonic content with (a) and without (b) an electrolytic capacitor for different line input voltage.

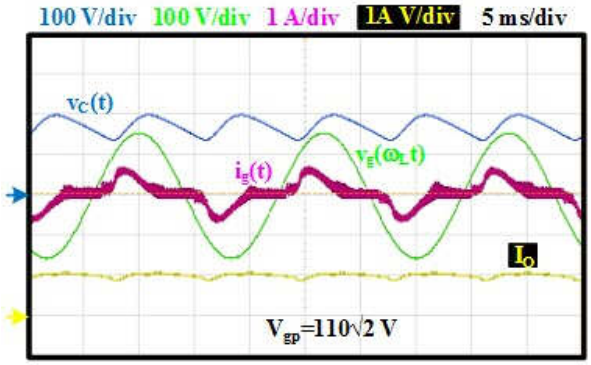


Fig. 10. Line input current ($i_g(t)$), input line voltage ($v_g(t)$), output voltage (V_O) and output current (I_o) of the AICS with low frequency ripple in the intermediate bus.

In order to validate the absence of flicker, the considerations in [19] have been followed. To limit the biological effects and detection of flicker in general illumination, Modulation (%) should be kept within the shaded region defined by [19]. Modulation (%) must be calculated assuming perfect ac power line conditions, being:

$$Modulation\ (\%)_C = 100 \cdot \frac{(L_{max} - L_{min})}{(L_{max} + L_{min})}, \qquad (13)$$

where L_{max} and L_{min} correspond to the maximum and minimum luminance of each harmonic of the ac component of the output current, respectively. In this test, proportionality between luminance and the ac component of the output current has been assumed. The results of this analysis are shown in Fig. 11. As can be seen, all the ac harmonic content falls within the shaded region, and therefore, the absence of flicker is achieved.

Finally, the efficiency measured in both prototypes is the same, i.e., 83.2 % at nominal input voltage. Figure 12 shows the efficiency versus the line input voltage. This efficiency is lower than other proposed topologies for replacing incandescent bulb lamps [8-11], but expected in AISC based on flyback. Traditionally, the efficiency of AISC is relatively low, due to the fact that some amount of power is processed twice by the AICS in order to shape the line input current. However, the operation of AICS allows the elimination of the electrolytic capacitor without flicker at the output current, which is the objective of this paper. Therefore, it could be said that the relatively low efficiency is the price to pay for replacing the electrolytic capacitor with a non-electrolytic one with lower capacitance (i.e. with extended lifetime) without flicker at its output.

IV. Analysis of the AICS with Low Frequency Voltage Ripple in the Intermediate Bus

At this point, it is obvious that a theoretical analysis of the AICS solution with low frequency ripple in the intermediate bus is required. This analysis should focus on the distortion of the line input current in order to validate the experimental results presented in the second test of the previous section.

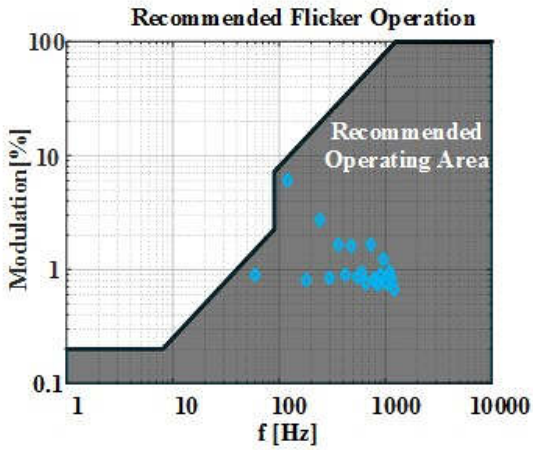


Fig. 11. Modulation (%) of the output current of the proposed design in the recommended operating area defined in [18].

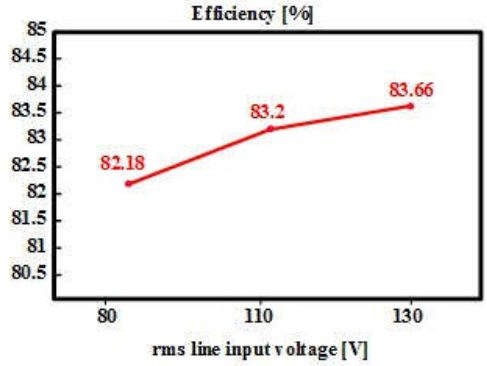


Fig. 12. Efficiency of the experimental prototype for different line input voltages.

If some ripple arises in the intermediate bus of the AICS due to the substitution of the electrolytic capacitor by another technology, the constant voltage, V_C, becomes $v_C(t)$:

$$v_C(t) = V_{Cdc} - V_{Cac}\sin(2\omega_L t) = V_{Cdc}(1 - k\sin(2\omega_L t)),$$

$_{dc}$ and V_{Cac} are respectively the dc component and ac component of the voltage across the intermediate bus, and k is the value of the relative ripple of $v_C(t)$. Note that only the component of twice the line frequency of $v_C(t)$ has been taken into account for the sake of simplicity.

The study is carried out for a flyback converter operating in CCM (or a member of the flyback family of dc-to-dc converters: SEPIC, Cuk and Zeta). Equation (13) and a modification of Equation (10) (i.e., changing d to d(t) and V_C to $v_C(t)$) can be used to calculate the duty ratio:

$$d(t) = \frac{Vo}{\frac{n_2}{n_1}(V_{Cdc}(1 - k\sin(2\omega_L t)))}. \qquad (14)$$

The duty ratio now varies with twice the line frequency due to the action of the output voltage feedback loop, which is designed to contribute either $i_O(t)$ or $v_O(t)$ to be constant. It is well-known that the output voltage feedback loop of the AICS can be designed with a very rapid dynamic output response to contribute the elimination of the low frequency ripple, which now originates from the input of the flyback dc-to-dc converter (i.e., the

intermediate bus of the AICS). This characteristic of the AICS [15-18] is the key to attenuate enough the low frequency ripple from $v_C(t)$ to the output (keeping a non-large output capacitor) and to ensuring that the removal of the electrolytic capacitor at intermediate bus does not involve flicker. However, this variation in the duty cycle plus the low frequency ripple of $v_C(t)$ has consequences on V_S (which becomes $v_S(t)$ in this analysis). From a modification of (11) (i.e., changing d to d(t), V_C to $v_C(t)$ and V_S to $v_S(t)$), (13) and (14), the expression of $v_S(t)$ can be deduced:

$$v_S(t) = V_o \frac{\frac{n_R}{n_1}}{\frac{n_2}{n_1}} \frac{(1-k\sin(2\omega_L t))}{(1-k\sin(2\omega_L t))+\frac{V_o}{\frac{n_2}{n_1}V_{Cdc}}}. \quad (15)$$

As (15) shows, $v_S(t)$ is now not a constant voltage source and therefore the line input current will not be sinusoidal during the conduction of the diodes of the rectifier bridge. Using a modification of (3) (i.e., V_C being $v_C(t)$ and V_S being $v_S(t)$), (13) and (15), the line input current will be:

$$i_{gdc}(t) = \frac{1}{R_{LF}} \cdot \left[V_{gp}|\sin(\omega_L t)| + V_o \frac{\frac{n_R}{n_1}}{\frac{n_2}{n_1}} \frac{(1-k\sin(2\omega_L t))}{(1-k\sin(2\omega_L t))+\frac{V_o}{\frac{n_2}{n_1}V_{Cdc}}} - V_{Cdc}(1-k\sin(2\omega_L t)) \right]. \quad (16)$$

It should be noted that this expression is only valid for the interval in which $v_g(t)$ is greater than $v_C(t)$-$v_S(t)$. This interval can be calculated by equating to zero (16):

$$V_{gp}|\sin(\omega_L t_i)| + V_o \frac{n_S}{n} \frac{(1-k\sin(2\omega_L t_i))}{(1-k\sin(2\omega_L t_i))+\frac{V_o}{nV_{Cdc}}} - V_{Cdc}(1-k\sin(2\omega_L t_i)) = 0; \quad i = 1,2, \quad (17)$$

where the conduction angle becomes:

$$\phi_C = 2\pi \frac{t_2 - t_1}{T} \quad (18)$$

As can be deduced from (16), the average input current of the AICS with ripple in the intermediate bus is non-sinusoidal during the interval $[t_1, t_2]$.

.Finally, the expression of R_{LF} can be deduced from the input power using (17). For the sake of simplicity, R_{LF} has been considered constant in this theoretical analysis:

$$R_{LF} = \frac{1}{P_g \frac{T}{2}} \int_{t_1}^{t_2} i_{gdc}(t) V_{gp}|\sin(\omega_L t)| dt = \frac{1}{P_g \frac{T}{2}} \int_{t_1}^{t_2} \left[V_{gp}|\sin(\omega_L t)| + V_o \frac{n_S}{n} \frac{(1-k\sin(2\omega_L t))}{(1-k\sin(2\omega_L t))+\frac{V_o}{nV_{Cdc}}} - V_{Cdc}(1k\sin(2\omega_L t)) \right] V_{gp}|\sin(\omega_L t)| \, dt. \quad (19)$$

At this point, the line input current of the AICS with low frequency ripple at intermediate bus can be plotted for a given specification. Figure 13 shows the normalized input current for the same optimized designs presented in Fig. 2, though now introducing some ripple on $v_C(t)$ (i.e., k<0.3).

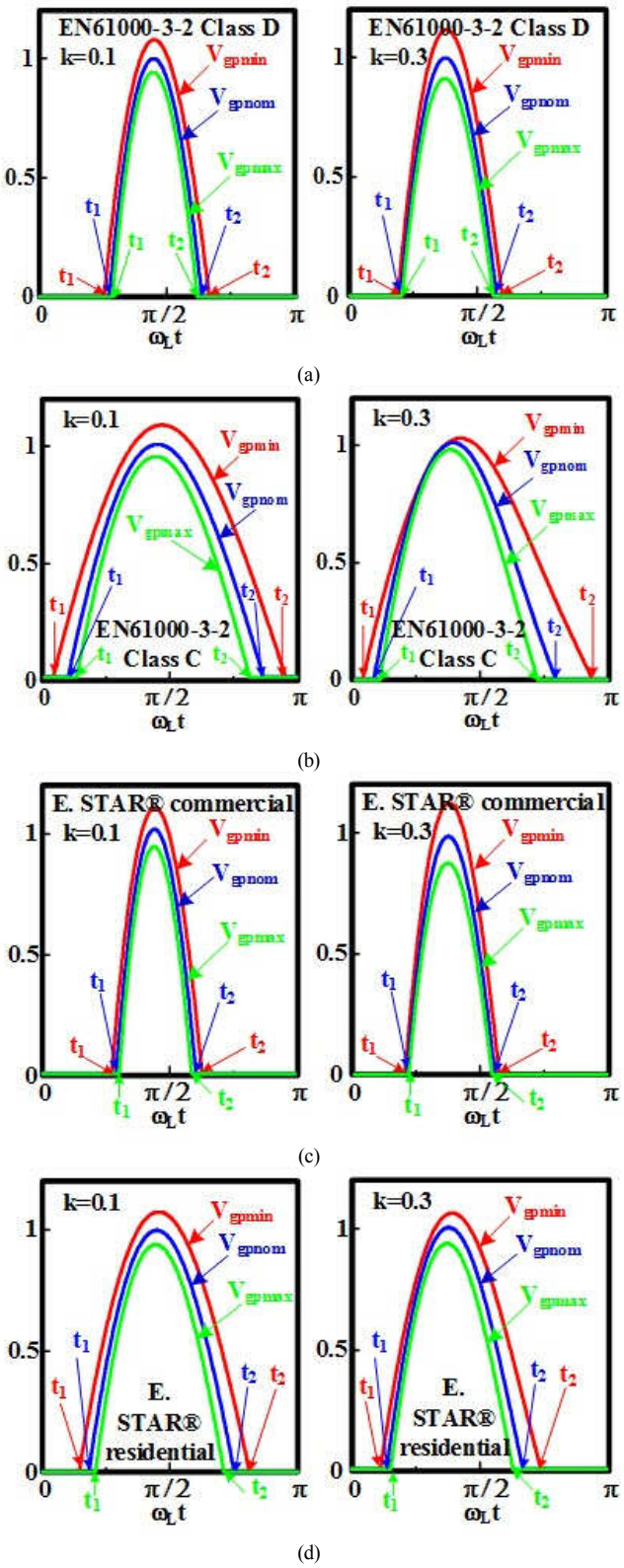


Fig. 13. Normalized input currents for different optimized designs at different peak values of $v_g(t)$ and k values: a) Class D European design. b) Class C European design. c) ENERGY STAR® American design for commercial applications. d) ENERGY STAR® American design for residential applications.

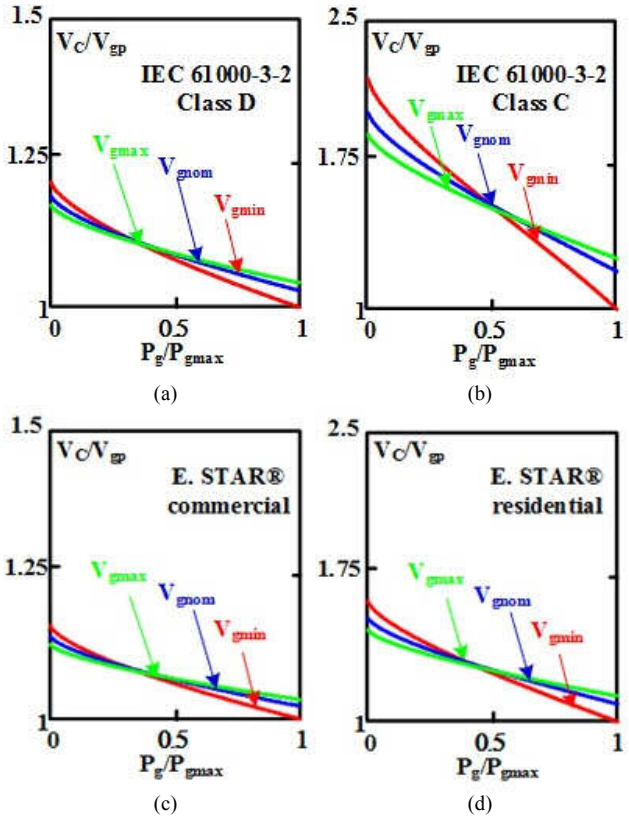


Fig. 14. Normalized ϕ_C at different V_{gp} values versus k for different optimized designs: a) Class D European design. b) Class C European design. c) ENERGY STAR® American design for commercial applications. d) ENERGY STAR® American design for residential applications.

As can be seen, slight distortion is introduced in $i_g(t)$ as k increases in all the optimized American and European designs. It is obvious that the input current is now not sinusoidal during the conduction angle and also that the interval which defines the conduction angle (i.e., $[t_1,t_2]$) is neither centered around nor equidistant from $\omega_L t=\pi/2$ as was introduced in experimental results of Section III.B. Although the expression of the conduction angle could be calculated from (17) and (18), no transcendent equation is thus obtained. Figure 14 shows the evolution of the normalized conduction angle (i.e., normalized to k=0 design) versus k for different V_{gp} values k of the optimized American and European designs. As can be seen, the variation of ϕ_C is not significant in any situation for moderate increases in k (i.e., k<0.3).

At this point, however, no conclusion can be drawn regarding the distortion of the input current of AICS by introducing low frequency ripple in the intermediate bus of an optimized design. Thus, using (17), (18) and (19), the PF and THD of $i_g(t)$ can be calculated as a function of k for different V_{gp} values (see Fig. 15). From Fig. 15, it can be concluded that the added the distortion of the line input current over proper natural one of AICS due to moderate frequency ripple values (i.e., k<0.3) in the intermediate bus is negligible. This means that compliance with ENERGY STAR® regulations (due to the non-variation of PF versus k) is still ensured for moderate values of k

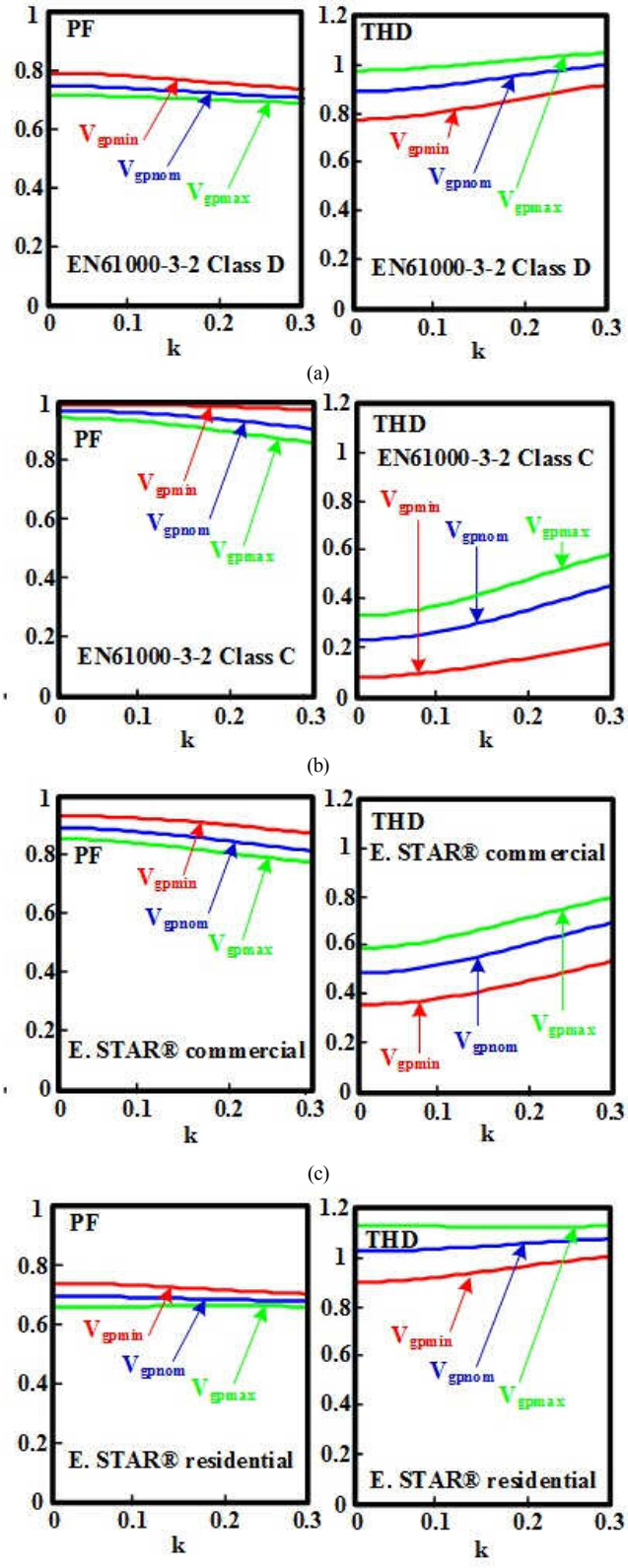


Fig. 15. PF and THD at different peak values of $v_g(t)$ versus k: a) Class D European design. b) Class C European design. c) ENERGY STAR® American design for commercial applications. d) ENERGY STAR® American design for residential applications.

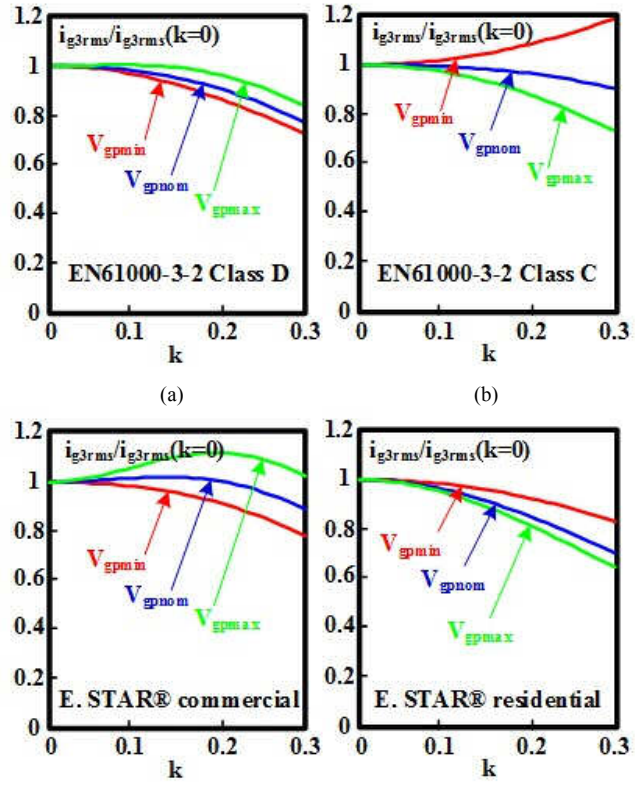


Fig. 16. Normalized 3rd harmonic of $i_g(t)$ versus k at different peak values of the input voltage for different optimized designs: a) Class D European design. b) Class C European design. c) ENERGY STAR® American design for commercial applications. d) ENERGY STAR® American design for residential applications.

(i.e., k<0.3) in traditional optimized designs.

For EN 61000-3-2 Class D regulations, however, the imposed limits refer to the power processed by the ac-dc HB-LED driver, while for Class C, the limits depends on the PF and on the rms value of the first harmonic. Figure 16 shows the normalized rms value of the third harmonic of $i_g(t)$ (i.e., normalized to a k=0 design) for optimized designs. As can be seen, the variation in the rms value of the normalized third harmonic is not significant in any situation for moderate values of k (i.e., k<0.3). Moreover, this analysis have been extended to all harmonic taken into account in the regulations with the same results: the rms value of each normalized harmonic is not significant, being the increase of the normalized 3rd one the greatest. This means that compliance with EN 61000-3-2 is ensured for these k values (i.e., k<0.3) if traditional optimized designs at k=0 [16, 18] have been previously employed. Therefore, this last analysis corroborates previous conclusion: the added distortion of the line input current by allowing some low frequency ripple at intermediate bus can be neglected in comparison to proper natural one of AICS.

Therefore, the proposed conclusion of this analysis is to design a traditional AICS without ripple in the intermediate bus because this ensures both compliance with international regulations and higher efficiency. Subsequently, if the aim is to eliminate the electrolytic capacitor to extend the lifetime, then it is simply necessary to ensure that the ripple in the intermediate bus is moderate (i.e., k>0.3).

Finally, the line input current of the experimental results of test B (i.e., k=0.2) can also be calculated using the theoretical model presented in this section. As can be seen in Fig. 10, the experimental results match theoretical values, thus validating the proposed model.

V. CONCLUSIONS

This paper presents an ac-to-dc HB-LED driver with no electrolytic capacitor based on the AICS solution. The operation of the AICS provides the opportunity to eliminate the electrolytic capacitor at the intermediate bus. But, by replacing the electrolytic capacitor with a non-electrolytic one with lower capacitance (extending its lifetime) some low frequency ripple arises in the intermediate bus of the AICS. As a result, some distortion of the line input current is added over the proper natural one of the AICS. However, as theoretical and experimental results show, this added distortion is slight in comparison to that of a regular AICS and compliance with international regulations (i.e. EN 61000-3-2:2014 Class D) is achieved. Moreover, no low frequency ripple is transferred to the output with the help of the rapid output dynamic response of AICS and hence no flicker is obtained in the ac-to-dc one-stage topology without an electrolytic capacitor. However, the proposed solution presents two main drawbacks: no wide input voltage range performance and slightly lower efficiency compared to other solutions. The first drawback is not critical because wide input voltage range is not mandatory in ac-to-dc HB-LED driver for substituting incandescent bulb lamps. However, the second one is the price to pay for a simple and low-size solution without an electrolytic capacitor and extended lifetime, based on the use of an AICS.

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