# Gate Impedance Characterization and Performance Evaluation of 3.3kV Silicon Carbide MOSFETs

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**Abstract – For the development of new wide bandgap high voltage semiconductors, it is necessary to carry out a thorough characterization of their behavior towards their future use in real applications. In this document a basic characterization of new 3.3 kV SiC MOSFET prototypes is presented, both static and dynamic. While the static characterization provides quite good figures of merit of the prototype under test, in the dynamic characterization, slow transitions are detected and they will be explained proposing a model for the configuration of the gate cell inner connections of the presented prototype.**

**Keywords: SiC MOSFET, high voltage, wide bandgap semiconductor**

## I. INTRODUCTION

Wide bandgap semiconductors are becoming major competitors to silicon semiconductors in those applications in which power silicon devices show limited performance. In particular, silicon carbide (SiC) MOSFETs show many advantages over their predecessors as, for example, faster switching transitions, greater blocking capability or the possibility to work at higher temperature. However, technologies used in manufacturing processes still must be optimized in order to obtain competitive devices compared to their silicon analogues, which have reached a high level of development.

The relevance of SiC devices has grown in recent years as a result of the excellent theoretical properties of this material [1]. Although SiC diodes have been available for some time and they have been included in different switching mode power supplies [2]-[5], the appearance of MOSFETs on the market is much more recent.

The fact that most of the power dissipated in power converters is located in the semiconductor devices causes that one of the main challenges consists in the improvement of them. Specifically, in relation to high voltage SiC MOSFETs they already exist 1.7 kV commercial devices [6][7], 3.3 kV devices in development [8] and it is expected that in the near future these ones will be capable of competing with silicon IGBT up to 5 kV [9]. In fact, there are already preliminary results with 10-15 kV SiC MOSFETs [10] [11].

The paper is organized as follows. Section II gives a first approach to the static and dynamic characteristics of these new devices. In Section III, a model that fits and explains the behavior of the MOSFETs according to the gate impedance is proposed. In Section IV, the results of the simulations are compared with time domain and frequency domain experimental measurements. Finally, conclusions are drawn in Section V.

*Figure 1 One of the MOSFETs under test*

## II. INITIAL CHARACTERIZATION

The aim of this article is, first, to introduce new 3.3 kV SiC MOSFETs (Figure 1) developed at the Institute of Microelectronics of Barcelona-National Microelectronics Centre (IBM-CNM), which are in manufacturing and improvement phase [12], and they have been verified by wafer characterizations of physical nature, proving its ability to block voltage and to flow current through them.

In this study, their feasibility for been used in switching power converters is also studied, and an initial characterization of them is carried out, both static and dynamic. Moreover, the dispersion of the measures is taken into account, repeating the tests in all the seven devices with provisional package which are available. It is known that they withstand different currents (4 of them, withstand a maximum drain current of 8 A, and the other 3 devices up to 3 A).

### *A. Static Characterization*

Some of the first tests done consist in measuring the input capacitances (Cgs -Figure 7) and output capacitances (Cds-Figure 8) using an impedance analyzer, and by varying the gate-source voltage ($V_{GS}$ between 0 and 15 V) and the drain-source

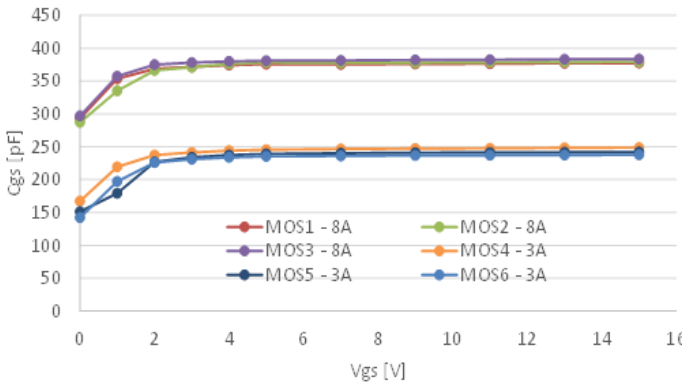


*Figure 2 Gate-source capacitance (Cgs[pF]) vs. gate-source voltage (Vgs[V]) for different devices*

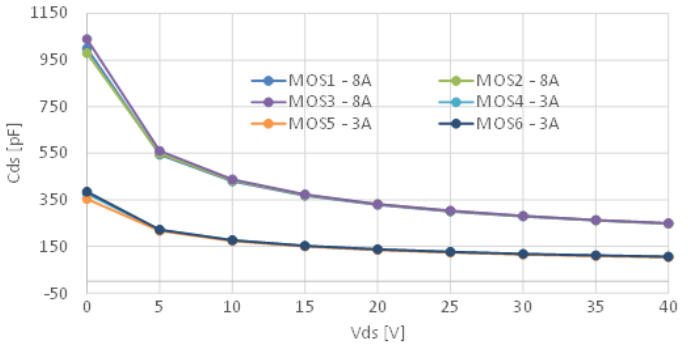


*Figure 3 Drain-source capacitance (Cds[pF]) vs. drain-source voltage (Vds[V]) for different devices*

voltage ($V_{DS}$, between 0 and 40 V), respectively.

As it is shown, as the $V_{GS}$ voltage is increased, the capacitance Cgs tends to a stable value of 374 pF for the 8 A devices, and to 250 pF for those withstanding less current. Cds capacitance tends towards a value of 220 pF for the 8 A MOSFETs, and to 100 pF for the 3 A ones. In this case the applied voltage, $V_{DS,}$ reaches only 40 V (which is the maximum voltage that the impedance analyzer is capable of applying). This is only an initial characterization of the devices a careful characterization should be done, increasing the voltage to levels closer to the voltages that the device may withstand, and checking that the output capacitance remains stable at those voltage ranges.

It is worth mentioning that the values obtained, even if they are not identical, they are consistent with those measured in a commercial 1.7 kV CREE SiC MOSFET, C2M1000170D [6].

It has also been of interest to obtain the output characteristic voltage-current curves (Figure 4 and Figure 5) from which the conduction resistance ($R_{DSON}$) and the threshold voltage ($V_{TH}$) of each device can be predicted. The measured values for the $R_{DSON}$ are about 650 mΩ for the 8 A current devices and 1Ω for those of less current and the $V_{TH}$ for both devices is between 3.5-4 V).

Similarly, the blocking capability of the MOSFETs was checked, and the parasitic diode existing in antiparallel (Figure 6) to the MOSFET was measured, whose knee voltage is in all cases around 1.5 V.

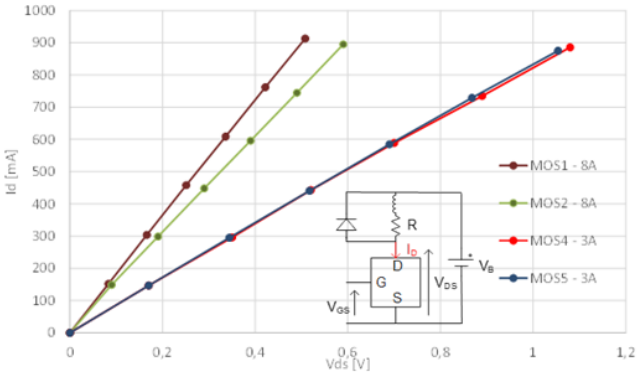


*Figure 4 Output characteristic curves Id[mA]-Vds[V] for different devices*

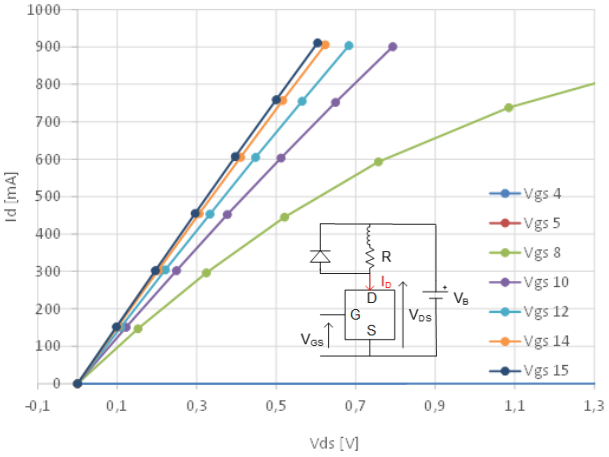


*Figure 5 Output characteristic curves Id [mA]-Vds [V] at different voltages (Vgs [V]) for a 8A MOSFET*

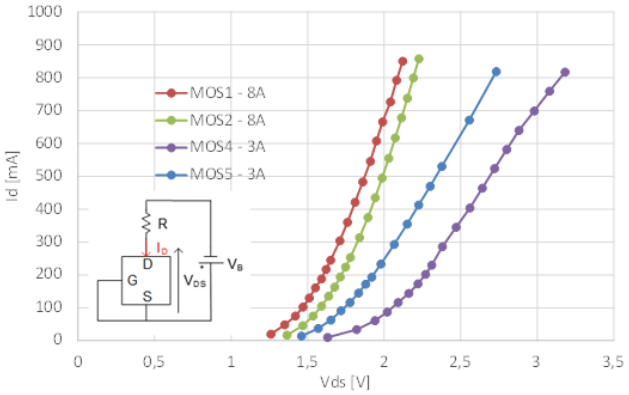


*Figure 6 Parasitic diode characterization (Id[mA]-Vds[V]) of different devices*

In any of the cases aforementioned, the results obtained are consistent both among all the devices under test, and also compared to commercial devices of a similar order of magnitude, whose $R_{DSON}$ according to the manufacturer is in the order of 1Ω and their $V_{TH}$ is approximately 2.6 V [6].

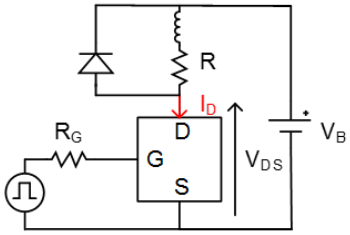


*Figure 9 Schematic of the circuit used for the dynamic characterization ($R$=94Ω, $V_B$=291 V, $f$=1 kHz)*

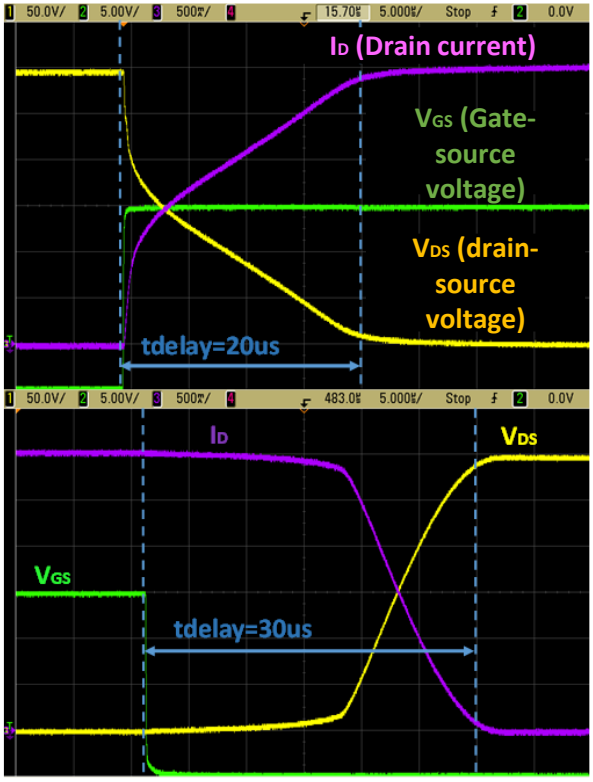


*Figure 10 Dynamic performance of the MOSFET. Up: turn-on. Down: turn-off. $I_D$ [A] (purple), $V_{GS}$ [V] (green) and $V_{DS}$ [V](yellow)*

### *B. Dynamic Characterization*

With regard to the dynamic characterization (Figure 9), initial tests at low switching frequencies (around 1 kHz to 10 kHz) are carried out. Although these lower frequencies may be considered really low frequencies for a final application, they will be reliable enough to see how transitions during switching are, and if the devices would be capable of working at higher frequencies.

In both cases, the observed behavior is not the one expected of a MOSFET, due to the unexpected slowness the devices show during transitions (Figure 10). During the turn-on, there is a first fast step both in $V_{DS}$ and in $I_D$, which turns into a slow slope until they reach their nominal voltage / current values, respectively. During the turn-off, conversely, first, a delay appears which, then, turns into a slow transition.

It must be said that the delays observed are independent of the frequency, and they make the devices unsuitable for their use in real power converters. Furthermore, in the presence of changes in voltage and current working values closer to the expected ones in applications where these MOSFET would be used, no significant improvements were found during commutations.

Figure 11 shows the dynamic response, in this case, the one of the C2M1000170D MOSFET, from CREE manufacturer, previously referenced [6]. It can be seen how the delays during transitions are much lower than in the MOSFETs under study (note the scale, which in Figure 11 is 200 ns/div against the 5us/div Figure 10).

Good static characteristics observed confirm that high voltage SiC MOSFETs have been developed. However, the dynamic tests performed suggest that there are still issues to be resolved in terms of their development.

Analyzing previous results, it is concluded that the gate circuit is slowing down these semiconductors switching, that is why a model to characterize the gate of these devices will be proposed.

## III. GATE IMPEDANCE MODELING PROPOSAL

This excessively slow performance can be attributed to the inner structure of the gate connections which conform the elementary cells forming the power device (Figure 10). This

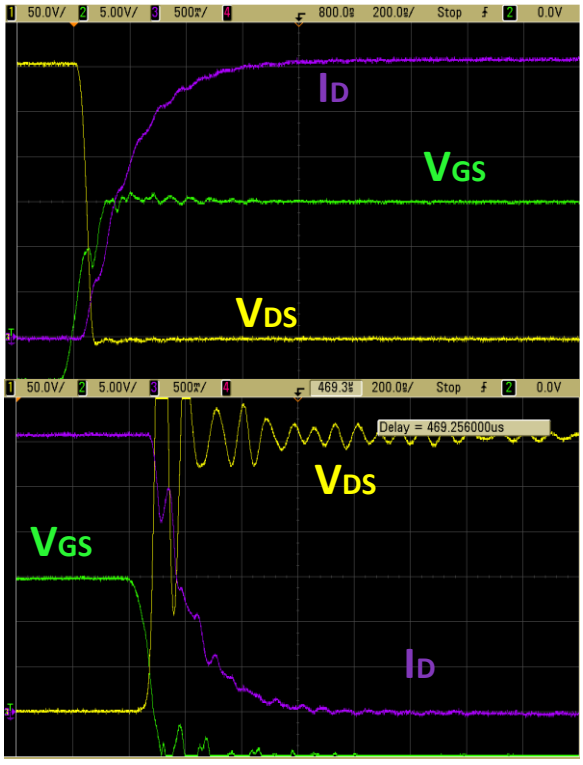


*Figure 11 Dynamic performance of the CREE MOSFET. Up: turn-on. Down: turn-off. $I_D$ [A] (purple), $V_{GS}$ [V] (green) and $V_{DS}$ [V] (yellow)*

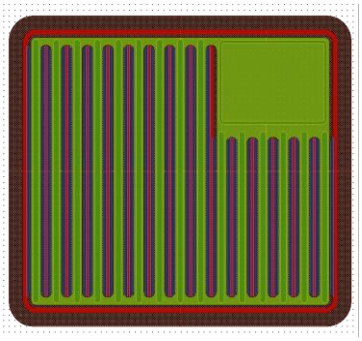

*Figure 12 Simplified structure of the SiC MOSFET under test. In green, gate contact.*

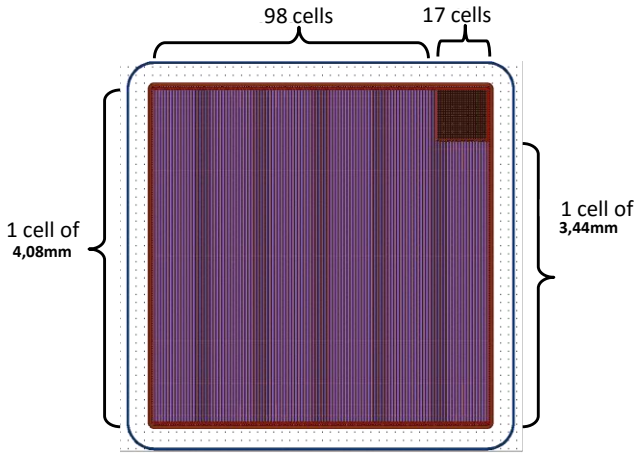


*Figure 13 Cell distribution of the SiC MOSFET*

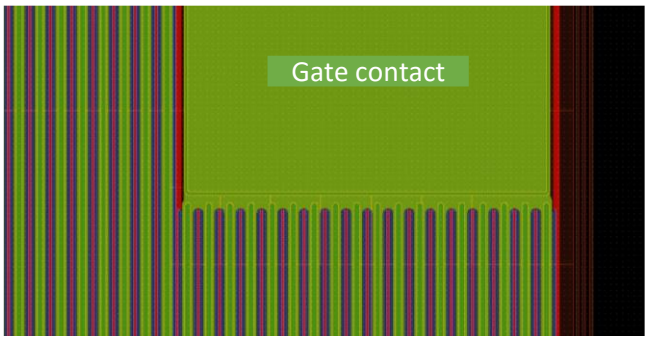


*Figure 14 Cell distribution detail of gate contacts*

structure consists of hundreds or thousands of cells linked so that the configuration of such junctions influence the gate impedance of the device and therefore its behavior.

In the case of the MOSFETs under test, it is estimated that their structure consists of cells linked by a design in strips (Figure 13 and Figure 14, where each of the cells is linked to the next / previous through a polysilicon doping), where the gate contact corresponds to a group of about 17 cells.

This arrangement can be explained by a model based on RC circuits, where three different sets of cells and two transitions between cells are proposed (Figure 15). R1-C1 pairs represent the gate contact cells characterized because their charging/discharging is very fast compared with the other junctions. In contrast, R3- C3 pairs will be characterized by a very slow charging / discharging.

The total impedance of the set, in general, for N cells, is calculated taking into account the expressions (1) and (2):

$$Z_1 = Z_{gate} = \sum_{i=N-1}^{1} R_i + \frac{\frac{1}{s \cdot C_i} \cdot Z_{i+1}}{\frac{1}{s \cdot C_i} + Z_{i+1}} \qquad (1)$$

Being

$$Z_N = R_3 + \frac{1}{s \cdot C_3} \qquad (2)$$

## IV. Experimental and Simulation Results

### A. Impedance measurements

To carry out a comparison between the proposed analytical model and the experimental measurements (Figure 17) an equivalent circuit has been simulated, shown in Figure 16, consisting of 20 RC sets whose values are shown in Table 1.

Those values follow a certain proportionality, where lower ones represent a small number of cells closer to the gate contact, while bigger values stand for a larger number of cells more distant from the gate contact.

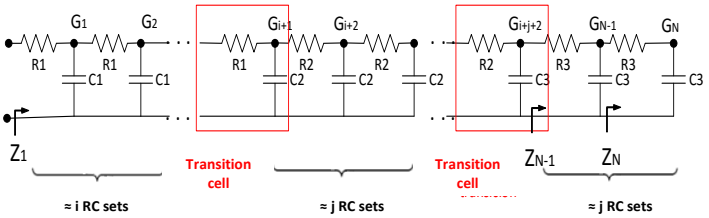


*Figure 15 RC circuit model which characterizes links among cells*

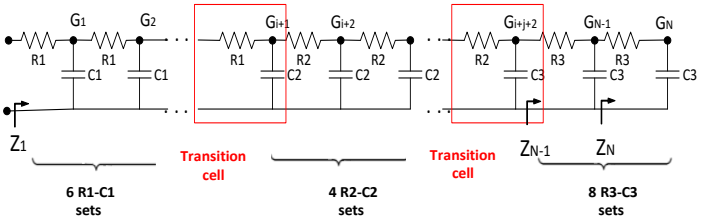


*Figure 16 Simulated equivalent RC*

*Table 1 Values of the RC sets*

| | |
|---|---|
| **R1 [Ω]** | 160 |
| **C1 [pF]** | 37,5 |
| **R2 [Ω]** | 758 |
| **C2 [pF]** | 53 |
| **R3 [Ω]** | 2275 |
| **C3 [pF]** | 159 |

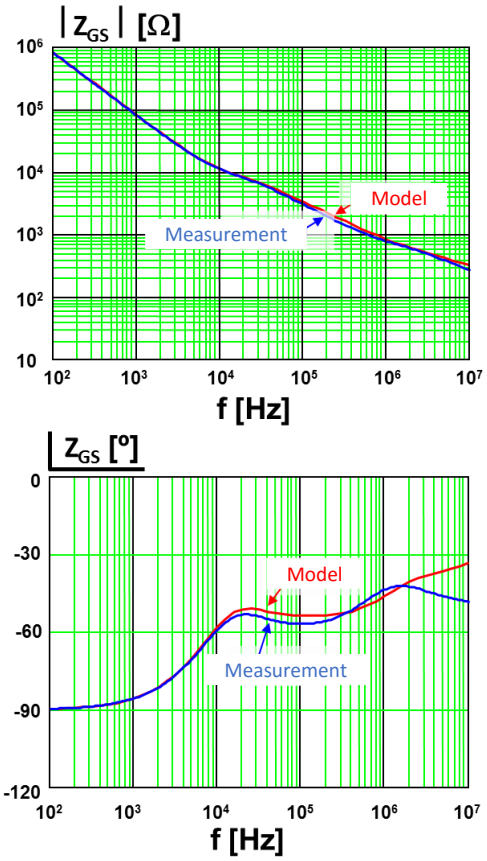


*Figure 17 Gate impedance of the MOSFET. Up: |Zg| in logarithmic scale. Down: Phase (Zg) in degrees (º) in lineal scale. In blue: measurements done with the impedance analyzer. In red: results obtained with the proposed model*

### *B. Time domain measurements*

Once established combinations R1-C1, R2-C2 and R3-C3 and the transitions that best fit the measured gate impedance and the behavior of the MOSFETs under test, a validation of the results in the time domain has been carried out.

Circuits in Figure 16 and Figure 18 have been taken into account in order to perform this simulation. This latter circuit is intended to represent the activation of the channels of different cells which the MOSFETs are composed of. The drain current is the sum of the contributions of each of these cells, each of one provide a current that is a function of the gate voltage seeing by that cell and its threshold voltage (see expression (4), where ' x ' represents the number of the cell).

$$i_x = f(V_{GX}, V_{TH}) \qquad (4)$$

The $R_{DSON}$ values have been adjusted considering the same proportionality taken for the RC sets, where quantity and closeness of cells to the gate contact is taken into consideration.

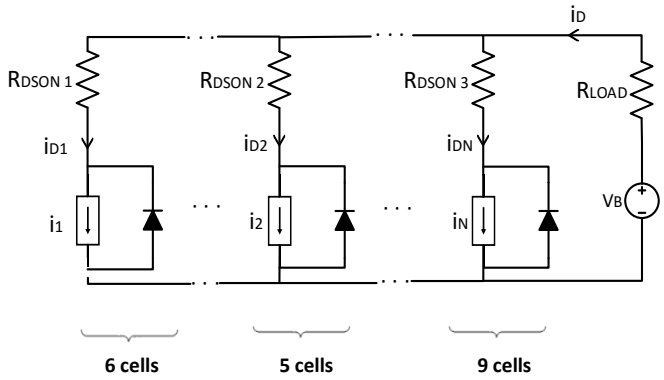


*Figure 18 Drain-source circuit of the MOSFET. $R_{DSON1}$ = 1400Ω, $R_{DSON2}$ = 16.5Ω, $R_{LOAD}$ = 5.5Ω, $V_B$ =291V*

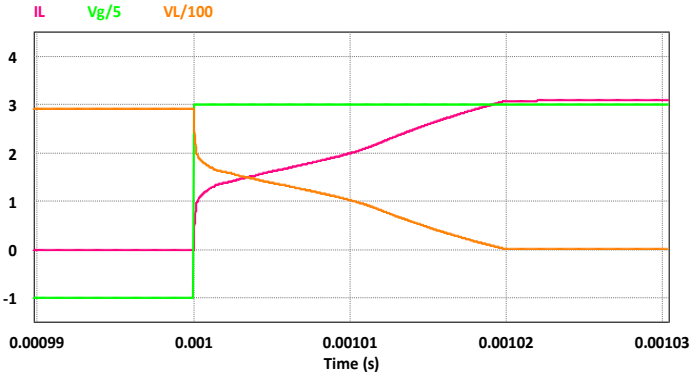


*Figure 19 MOSFET turn on. In pink $I_d$[A]. In orange $V_{ds}$/100[V]. In green $V_g$/5[V]*

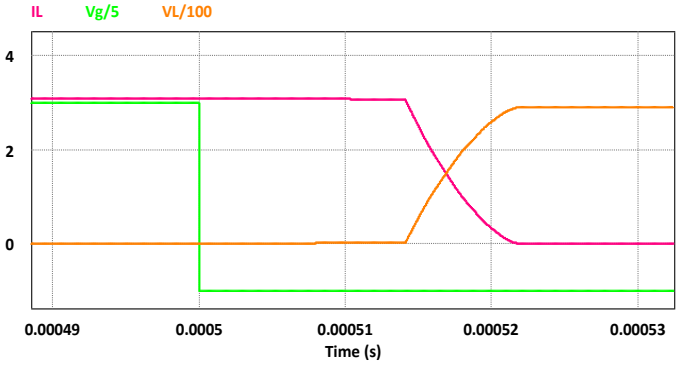


*Figure 20 MOSFET turn off. In pink Id [A]. In orange Vds/100[V]. In green Vg/5[V]*

The results of this simulation are shown in Figure 19 (turn on of MOSFET) and Figure 20 (turn off of the MOSFET).

As it can be seen, with the adjustments made in the model, the delay that appeared in the turn off of devices and the slow transitions have been achieved. These transitions are on the order of 20us, similar to the measurements obtained in the laboratory.

## V. Conclusions and future work

New 3.3 kV SiC MOSFETs have been characterized, obtaining static characteristics consistent with commercial devices from other manufacturers that offer the same range of current but lower voltage. However, the dynamic behavior is not yet the desirable one.

In order to study in detail the reason for the slowness observed in the switching, a model based on RC circuits has been proposed. It explains the slow performance of these devices during switching transitions. This model is based on the structure of the junctions between cells that make up the gate of the MOSFETs.

The proposed model has been analytically validated by mathematical software and also with simulations based on groupings of cells. Concurrently, they have carried out experimental measurements of the devices gate impedance that conform to the results obtained by simulations in MATLAB, MATHCAD® and PSIM®, thus validating the proposed model.

As future work it is intended that this gate impedance characterization would be useful to know to what extent it will possible to modify the doping of polysilicon or even the structure of the junctions between cells that make up the gate, and try to develop MOSFETs with better performance in the near future.

## VI. Acknowlegdments

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