Implementing Low Power Consumption in Standby Mode in the Case of Power Supplies with Power Factor Correction

Kevin Martín, Pablo F. Miaja, Diego G. Lamar, Javier Sebastián
Departamento de Ingeniería Eléctrica, Electrónica, de Computadores y Sistemas
University of Oviedo
33204 Gijón, Spain
martinkevin@uniovi.es

Santiago Álvarez
Santiago Engineering Design ltd.
Hong Kong, People's Republic of China

***Abstract*— This work analyzes different options to implement low power consumption in Switching Mode Power Supplies (SMPSs) with Power Factor Correction (PFC) when they are in standby mode. The standard SMPSs for power levels higher than 100 W are made up of two stages: a classical PFC stage based on a Boost Converter operating in the Continuous Conduction Mode and a second stage based on any type of isolated DC-DC converter. The value of the resistive sensors needed by the PFC control stage determines a standby consumption higher than 0.5 W if the power supply has to be designed to operate in the Universal Range of line voltages. This fact makes it very difficult to comply with European Ecodesign Regulations. To overcome this problem, several solutions are proposed and analyzed in this paper, the most promising being implemented in a real SMPS prototype.**

Keywords*— *AC-DC power converters, Low-cost power supply, Power factor correction, Standby.

I. INTRODUCTION

Most of the electronic equipment is supplied from the AC line by a Switching Mode Power Supply (SMPS), which adapts the AC voltage level to the one needed by each piece of electronic equipment. With the increasing concern about power saving and sensitive power consumption, more efficient SMPSs are required. In this sense, energy labeling is playing a major role in raising customer awareness about efficient products and incentivizing companies to enhance their products [1]. Programs such as Energy Star and 80 PLUS evaluate power supplies and electrical appliances regarding their active efficiency working at different loads. Also directives such as the European Union Ecodesign [2] and Energy Labelling [3] have been one of the factors to promote a reduction of energy consumption [4].

Although energy labelling based on active efficiency provides quite good information about SMPS performance, this may not be enough to define a power supply as 'green' or 'power saving'. In the case of electrical devices that are always plugged to the line (such as TV sets, Personal Computers (PCs), consumer electronics, etc.), it is quite common for the device to be partially switched off or not performing their main functions. In this condition, the power supply of each piece of equipment is still working in a no-load mode, also known as standby mode. While the device is on this state, power consumption usually ranges from 1 to 25 W [5]. When the consumption of all of these devices are taken into account, the power wasted in standby mode is responsible for 5% to 10% of power consumption in an average home and about 1% of global CO_2 emissions worldwide [6]. This has led to proposals such as the 1-Watt Initiative [6], which limits standby active power consumption of commercial equipment to 1 W by 2010 and 0.5 W by 2013. In Europe similar regulations have been issued and devices must reduce standby power to less than 0.5 W [7] or even less in some cases [8] in order to meet Ecodesign requirements.

Although the word standby is commonly used for all idle or no load working points and will be used in this paper as a general term, it should be noted that European Ecodesign Regulations define four different possible modes for power supplies [8], [9]:

1) ***"Active mode"*** refers to the condition where the piece of equipment is connected to the mains and one or more of its main functions are active.

2) ***"No-load mode"*** refers to the condition where an external SMPS is connected to the mains but no primary load is connected to its output. Maximum power consumption while on this mode varies between 0.5 W and 0.3 W depending on product type and specs [8].

3) ***"Standby mode"*** refers to the condition where the equipment is connected to the mains but none of its main functions are active. While on this state, it only provides a reactivation function and/or status information. The reactivation function allows the activation of the other modes by a remote switch. Maximum power consumption while on this mode is 0.5 W (up to 1 W if a status display is present) [8].

4) ***"Off mode"*** refers to the condition in which the equipment is connected to the mains but is not providing any function. Status information can be given while on this mode. Maximum power consumption while on this mode is 0.50 W [8].

Because new devices have to comply with these initiatives, standby modes have to be taken into account when designing

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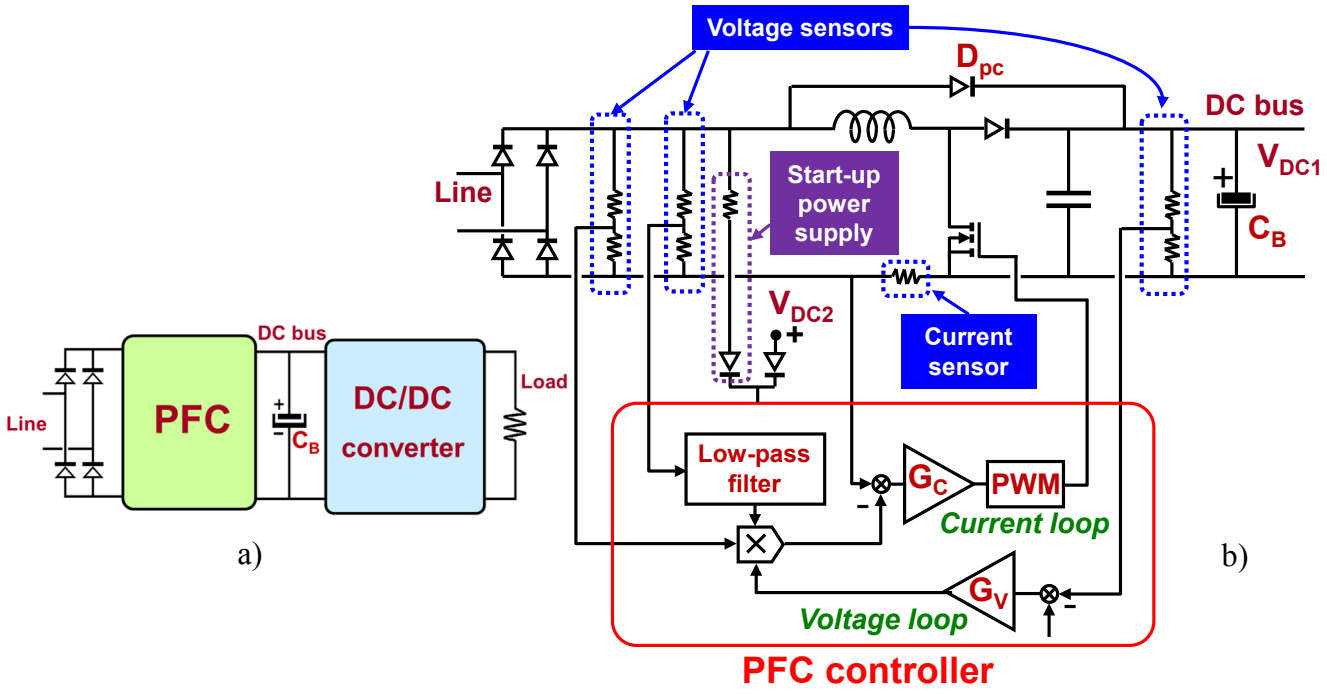

Fig. 1. a) SMPS with PFC. b) PFC based on a Boost converter controlled using a standard controller (analog multiplier approach).

AC-DC SMPSs. In some cases, just the quiescent currents of control and auxiliary circuits are well over the limits. Although there has been extensive research about power reduction in standby and off mode, proposed solutions are mainly for the DC/DC stage of off-line SMPSs without a PFC stage at the input [9-11]. However, SMPSs with input power above 75 W need a PFC stage at the input to comply with the regulations regarding the line current harmonic content [12], [13]. Only a few solutions have been proposed to maintain the standby consumption below 0.5 W in the case of SMPSs with a standard PFC stage at the input port (see Fig. 1.a). This PFC stage is usually based on a Boost converter operating in the Continuous Conduction Mode (CCM) and controlled by a commercial low-cost controller (based on an analog multiplier, see Fig. 1.b) [12], [13]. The standby consumption of both the controller and the voltage sensors is normally well above 0.5 W, especially if this controller is a low-cost one or if it is a "combo" controller (which is also in charge of controlling the DC/DC stage), both of which usually lack a disabled or low power mode. The solution proposed in [14] is based on increasing the voltage sensor resistors up to the range of several MΩ. This is only possible with some specific controllers and it degrades the controller performance [16].

To overcome the lack of solutions to allow SMPSs with PFC to drain less than 0.5 W in standby mode, this paper presents the circuitry needed to achieve this goal even when a low-cost combo controller is used. It has been successfully implemented in a prototype of commercial 100 W, 80-250 VAC, SMPS for a low-cost guitar amplifier.

Standby power consumption challenges for the used SMPS topology are presented in section II, where the proposed solution is explained. In section III the system is validated through experimental measurements. Finally, conclusions are drawn in section IV.

II. Case Of Study: A SMPS With A PFC Based On A Boost Converter

AC/DC SMPSs do not achieve 0 W consumption when the load is not connected because they have several auxiliary circuits that drain power in this situation, such as auxiliary power supplies, minimum output loads and miscellaneous auxiliary subsystems. Only some of this elements can be easily disconnected and their power consumption heavily depends on the specific implementation.

One of the most troublesome auxiliary circuits are resistive sensors. As can be seen in Fig. 1.b, the PFC stage needs several resistive voltage sensors (three in this case) for the multiplier based controller. These sensors are connected to either the rectified input voltage or the DC bus, where rather high voltages are present. If a 380 V DC bus is considered, the maximum current to dissipate less than 0.5 W is 1.32 mA. This is way less than a low-cost controller requires for operating [15] and, therefore, the control and sensors should be disconnected in standby mode. Depending on the controller used, it may not be so easy to disconnect it and it could require disabling its supply circuit.

Resistive sensors cannot be put in idle mode and additional circuitry (high-voltage switches) would be needed if they had to be disconnected from their measuring points (see Fig. 2). This approach is even more complex than it seems, as it could either require several high side drivers for the switches or could disconnect the sensors from the circuit ground, exposing the controller inputs to potentially damaging common mode voltages. A possible implementation based on discrete

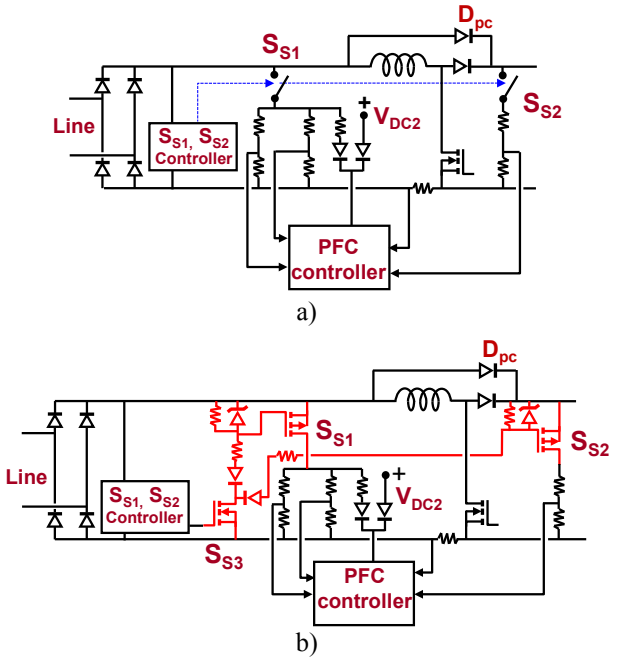

Fig. 2. Disconnecting the resistive sensing networks: a) general scheme. b) possible implementation based on several high voltage, low current MOSFETs.

components is shown in Fig. 2.b). It requires a high voltage N type MOSFET (S_{S3}) which should be on during regular operation of the SMPS. When the system enters into standby mode, it should be off in order to also switch off the high voltage P type MOSFETs (S_{S3} and S_{S2}). This solution is discarded as it requires too many high-voltage active elements, significantly increasing the cost of the converter.

The only simple way of reducing the resistive sensors power consumption is increasing their values. Even though using larger resistor values may seem as a good way to limit sensors power consumption, using very large values for these resistors is not recommended as it could compromise the measurement accuracy, noise immunity and system stability [16].

Disconnecting the whole PFC stage from the line with a single series disconnecting switch S_d can be a simpler and cheaper solution than individually disconnecting subcircuits (see Fig. 3.a). As the controller is not going to be working during standby mode, there is no need for the converter to be fed with AC voltage. Standby power consumption is then limited to the leakage current of S_d and its driving circuitry. The use of CMOS logic for this purpose and the careful design of its driving circuitry allow low consumption even from 250 VAC.

At this point, it is absolutely critical to carefully choose the current rating for the disconnecting switch S_d. The Boost converter is not naturally protected from output short-circuit and from the peak inrush current. This peak inrush current heavily depends on the line voltage just at the moment of the converter connection. It should be noted that the needed bulk capacitor C_B [12], [13] must be charged from the line in a short period of time, producing an extremely large peak current. In order to protect the converter diode (a high-frequency switching one), a robust low-frequency diode D_{pc} is often used to provide a by-pass path for this current peak. In a 100 W SMPS, the pre-charging path resistance (from the line to the bulk capacitor C_B through the rectifier and pre-charging diode D_{pc}) is typically about 2 Ω, which means a potential peak inrush current of about 180 A at 250 VAC. Therefore, the disconnecting switch S_d must be rated for this peak current value.

The inrush current peak can be limited by using a NTC thermistor (RNTC in Fig. 3) [17]. This is a simple low cost solution that requires minimum circuit modifications, but it has several drawbacks. First of all, it has to be appropriately chosen regarding energy absorption capacity, current ratings and resistive value. Besides that, as it is a temperature dependent device, if the SMPS is switched on while the NTC is still hot, the current limiting action of the NTC is not effective. Due to this possible situation, the disconnecting switch S_d has to be rated for the worst case scenario: maximum input voltage and minimum NTC resistance. Some bypass circuits have been

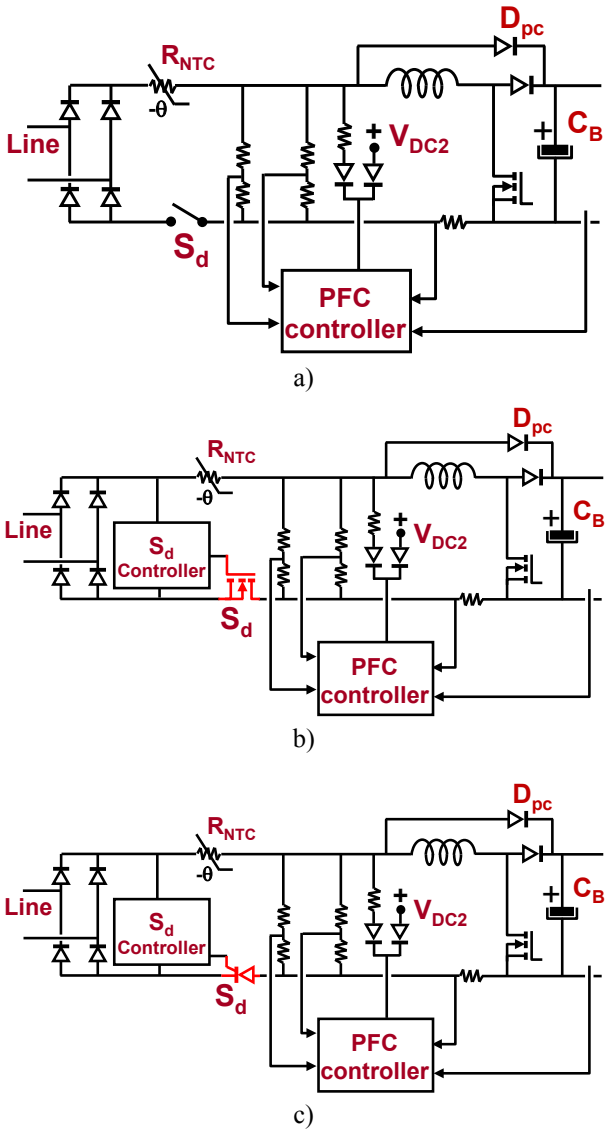

Fig. 3. Disconnecting the PFC stage: a) general scheme. b) S_d implementation based on a MOSFET c) S_d implementation based on a thyristor.

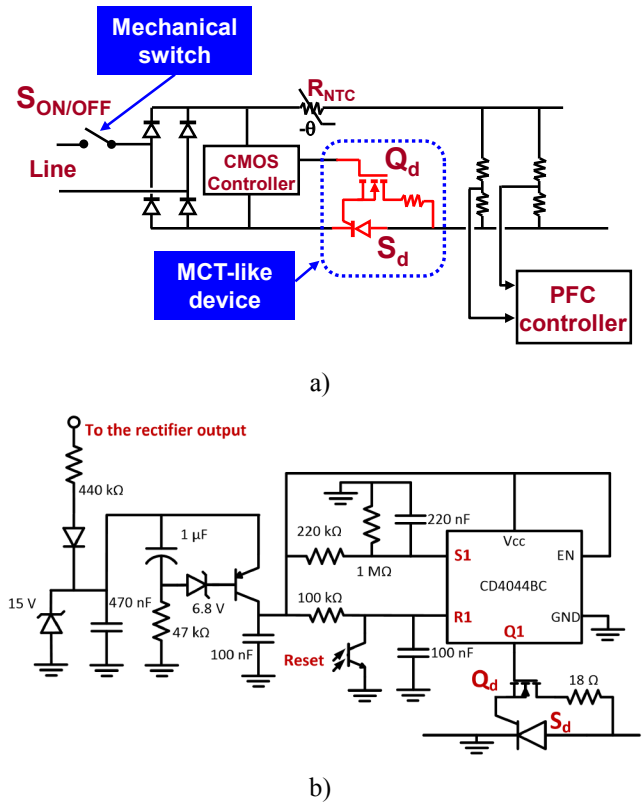

Fig. 4. a) S_d implementation based on an MCT-like device. b) Control circuitry for S_d.

proposed to avoid startups with a hot NTC, but they require another fully rated, floating ground switch and additional control circuitry, not suitable for a low cost application [18].

Ideally, the disconnecting switch S_d has to be rated for a high non-repetitive peak current, to have low conduction losses and to have a low driving current consumption (clearly lower than that of the PFC controller and their voltage sensors). Unipolar devices with isolated gate, such as MOSFETs (see Fig. 3.b), seem suitable for this application due to the fact that their gate consumption is negligible compared to that of bipolar devices. However, high voltage and high peak current MOSFETs are often too expensive and thus not appropriate for a low cost application.

In this situation, a thyristor (see Fig. 3.c) is preferred as practical implementation for the disconnecting switch S_d, as they usually have better non-repetitive peak current ratings than MOSFETs at lower prices [19], [20]. This is due to conductivity modulation in bipolar devices, such as thyristors, that does not exist in unipolar devices [21].

Nevertheless, they require higher gate currents and have to be re-triggered if their current falls below the holding current. It should be noted that the use of a PFC implies that the line current must be sinusoidal (ideally) and, therefore, the current passing through the disconnecting switch S_d (in this case, the thyristor) has to pass below the holding current level of a thyristor. As a consequence, the thyristor must re-triggered every half-line cycle in normal (not standby) mode. The control circuit in charge of properly driving the thyristor in normal mode, must be carefully designed to drain very low current in standby mode, thus allowing the complete SMPS (PFC+DC/DC converter) to comply with the Ecodesign Regulation.

The above-mentioned driving problem could be easily overcome by using a MOS-Controlled Thyristor (MCT). As the use of an actual MCT does not make sense in this application due to its cost and power range, a discrete MCT-like device is used. It can be easily implemented using a low-cost thyristor and a low-current MOSFET Q_d, as shown in Fig. 4.a. By controlling the Q_d gate instead of the thyristor gate, the S_d controller can be implemented using CMOS technology, which implies very low power consumption from the line when the SMPS is operating in either normal or standby mode. Fig. 4.b shows the actual circuit used to control the MCT-like device in a real prototype of SMPS for a low-cost guitar amplifier. This implementation is deemed the most appropriate based on Table I, which shows a comparison of the different possible implementations of S_d.

As the forward voltage drop across the thyristor when it is conducting is known, the resistor in series with Q_d is easily calculated to inject the appropriate gate current to trigger the thyristor. When Q_d is driven off by the CMOS controller, the thyristor is no longer triggered and it will disconnect the PFC and the DC/DC converter from the line at the next zero crossing of the line current. This may delay standby activation up to 10 ms, which is not critical at all.

The logic is based on a single CMOS NAND R/S latch CD4044BC, with a maximum quiescent current of 20 µA. Its output state is setup by the RC networks connected to its inputs. They are designed with different time constants so they naturally reach the desired values in a known sequence. During startup, the voltage at the latch input R1 raises faster than that across S1, enabling Q1 and, therefore, turning on Q_d and S_d. This fact keeps

TABLE I. COMPARISON OF DISCONNECTION PROPOSALS

Solution	No. of high-current, high-voltage switches	No. of low-current, high-voltage switches	Switches cost	Switch control referred to ground	Control current	Total cost
Sensor disconnection	0	3	Medium	Yes (using 3 switches)	Very Low	Medium
Series MOSFET	1	0	High	Yes	Very Low	High
Series Thyristor	1	0	Low	Yes	Too High	Low
Series MCT	1	0	Very High	Yes	Very Low	Very High
Series MCT-like device	1	1	Low	Yes	Very Low	Low

the thyristor on during regular operation of the SMPS, even if the current goes below the holding current. When a reset signal is issued from the central system controller (different from the S_d and the PFC controllers) via the phototransistor shown in Fig. 4.b, R1 goes down and the circuit enters into standby mode. It remains in this mode until the SMPS is switched off and on again using the mechanical ON/OFF switch $S_{ON/OFF}$ (shown in Fig. 4.a), that works as the main SMPS switch and that completely disconnects the whole device (the guitar amplifier) from the mains, allowing the complete shutdown of the SMPS. The above mentioned central controller is supplied from one isolated output of the DC/DC stage of the SMPS (V_{DC2} in Fig. 1.b), and it is switched off when it enters into standby mode. Due to design specs, the whole device (the guitar amplifier) has to be disconnected from the mains to reinitialize it, otherwise it would be kept in standby mode. When the mechanical ON/OFF switch $S_{ON/OFF}$ is off, both inputs of the CD4044BC are at 0 logic level, resetting the circuit to its original state and enabling a regular startup.

The circuitry that controls S_d is supplied with a regulated voltage from the diode bridge rectifier at the input of the SMPS. Using a simple Zener biasing circuit proved ineffective as the CD4044BC starts working with a supply voltage as low as 3.3 V. During startup, it would provide a low voltage control signal to Q_d that would cause hiccup in the system. In order to ensure that a minimum threshold is reached before starting operation, some additional circuitry is added. In Fig. 4.b, a simple circuit with a PNP transistor, a 6.8 V Zener and an RC network is shown. The transistor will be open as long as the voltage at its emitter is lower than 7 V, ensuring the CD4044BC will only start operation with a voltage high enough for properly driving Q_d.

III. Experimental Results

A 100 W, 80 - 250 VAC SMPS is designed and built with a front-end PFC Boost converter and an isolated DC/DC converter with several outputs (see Fig. 5). It supplies a 100 W, half-bridge audio amplifier and some digital circuitry for control, standby monitoring and signal processing purposes. The standby circuitry proposed in Fig. 4.a and Fig. 4.b is implemented in order to verify its correct operation.

The active input power in standby mode at different input voltages is always well below the European Ecodesign Regulation limits [7], [8], the maximum power consumption being 0.3W at 250 V_{AC}. Without the proposed circuit the consumption in standby mode was over 1 W, especially due to resistive sensors of the PFC stage. The measured active power consumption for different peak mains voltages with the proposed standby system is shown in Table II.

The SMPS efficiency is measured both with and without the implemented solution to reduce the losses in standby mode. The measurements show that the series thyristor has a very limited effect on the SMPS efficiency, because the efficiency reduction is about 1%, as can be seen in Fig. 6. Thyristor conduction loses are higher for 110 V_{AC}, as the input current is also higher. The overall efficiency of the complete system is fairly limited by the low cost required for the SMPS.

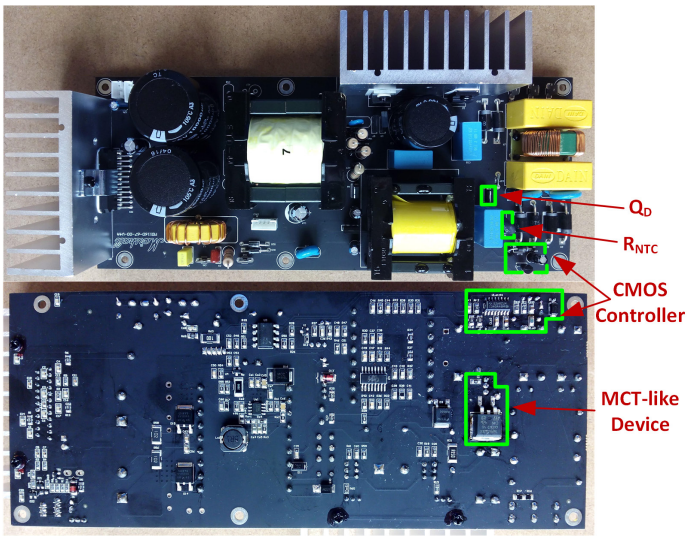

Fig. 5. Prototype of the SMPS with the added circuitry for low power consumption in standby mode.

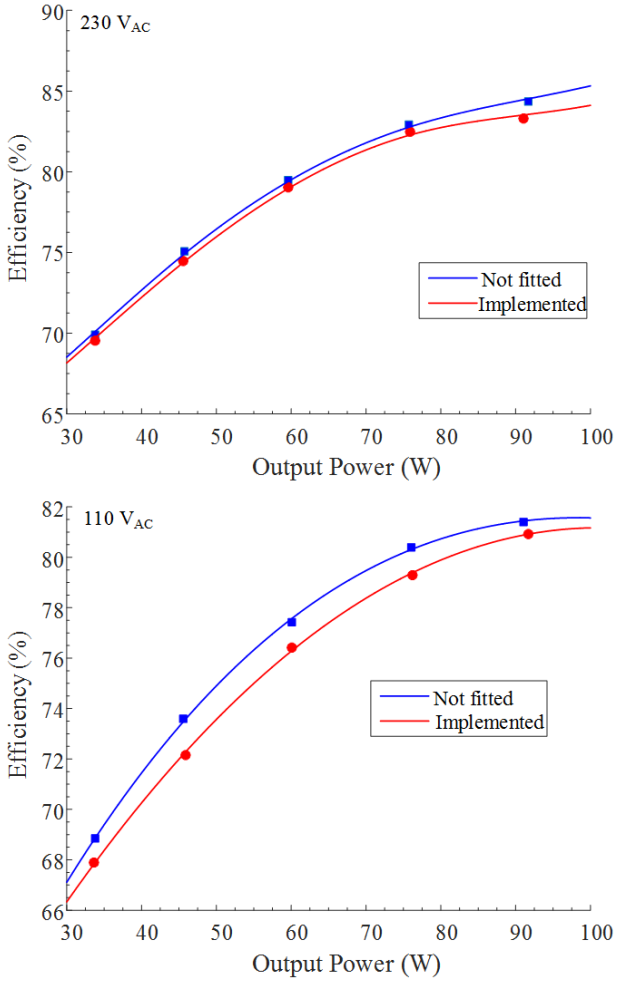

Fig. 6. System efficiency at 230 V_{AC} (top) and 110 V_{AC} (bottom) when the standby system is implemented (red) and bypassed (blue).

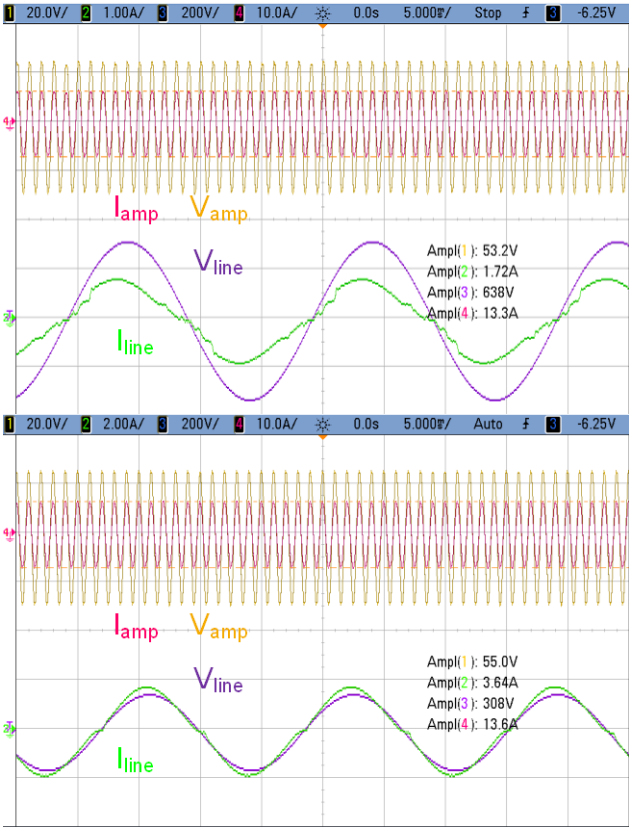

Fig. 7. 1 kHz, 100W output audio voltage (yellow) and current (pink) and input voltage (purple) and current (green). Waveforms for 230 V_{AC} (top) and 110 V_{AC} (bottom).

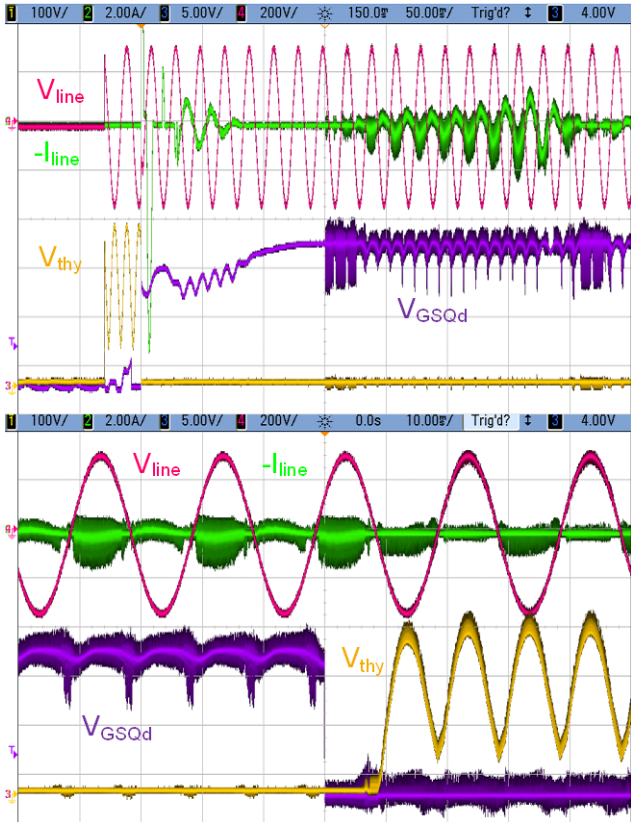

Fig. 8. Startup (top) and disconnection sequence (bottom) showing the voltage across the thyristor (yellow), the voltage across the gate-source terminals of MOSFET Q_d (purple), line input current (green, inverted) and line voltage (pink).

Power factor (PF) and total harmonic distortion (THD) of the line current have also been measured. The obtained PFs at full load are 0.92 and 0.99 at 230 VAC and 110 VAC, respectively and the line current THD measurements are below 15% for all operating points. Fig. 7 shows the line voltage and current at full load and also the audio output voltage and current. When the thyristor is bypassed, there is no significant change in these measurements.

Fig. 8 shows the startup of the converter and the activation of the thyristor. It can be seen how, when $S_{ON/OFF}$ is open, the system is disconnected from the mains. Once it is closed, the thyristor withstands the rectified input voltage while the capacitors in the voltage regulator for the control circuit (see Fig. 3.b) start charging. However, Q_d gate is kept low until the supply voltage reaches the desired threshold of ~7V. Once it is activated at an appropriate voltage level, Q_d injects current into the thyristor gate, connecting the SMPS to the mains. Depending on the angle of the grid voltage at the time of connection, a large capacitor pre-charge current surge can occur, as can be seen in Fig. 8 (I_{line}). Once the capacitor is charged and the control circuitry is supplied a stable voltage, the SMPS starts its soft start process while the Q_d gate voltage steadily increases up to 15 V with a slight ripple which does not affect normal operation of the circuit.

TABLE II. STANDBY ACTIVE POWER CONSUMPTION

Input voltage (V_{AC})	Active Input Power (W)
80	<0.1
110	<0.1
230	0.2
250	0.3

Finally, the disconnection sequence is also shown in Fig. 8. Before the Reset signal is driven down, the converter is only processing the power required by the audio amplifier in mute mode and the digital circuits. When the central controller decides that the audio amplifier is not being used and the system should enter into standby mode, it issues a disconnection signal that is applied upon the Reset input. The latch then applies zero voltage to Q_d gate and the current through the thyristor gate is interrupted.

It was mentioned before that the thyristor will not switch off until its current level decreases below the holding current, which means a disconnection delay. This delay can be clearly seen in Fig. 8, where the Reset signal is driven down slightly after the zero crossing of the line current, when this current is already over the thyristor holding current level. Because of this, the thyristor does not turn off until the next zero crossing of the line current. It is important to remember that this delay is negligible

as, at this point, the audio amplifier has already been in idle state for a long time.

IV. CONCLUSION

This paper presents a cheap, simple and robust circuit to achieve low power consumption in a SMPS with a PFC stage at its input port, when this SMPS is operating in standby mode. This low power consumption is needed to comply with European Ecodesign Regulations. The use of a series switch offers the lowest power consumption when the SMPS is in standby mode. Nevertheless, this series switch has to be rated accordingly with the fact that an extremely high inrush current is expected due to charging process of the bulk capacitor placed at the output of the PFC stage. The solution based on MCT-like device, made up of a low cost thyristor driven by a low-current MOSFET and CMOS circuitry, has been successfully implemented.

Although the proposed solution has been implemented and designed for a low cost application and is based on low cost components, it can be applied to any SMPS without major modifications.

Experimental measurements verify the right operation of the proposed circuitry in the whole input voltage range. The addition of the series thyristor has a low impact on the system efficiency and does not affect the performance of the SMPS. Disconnecting the whole system from the mains with a series MCT-like device controlled by low power CMOS circuitry is also proven as an appropriate solution for severely reducing the standby power consumption of many SMPSs in order to comply with the European Union Ecodesign directive.

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