High-Frequency Modulated Secondary-Side Self-Powered Isolated Gate Driver for Full Range PWM Operation of SiC Power MOSFETs

Jorge Garcia
Dept of Electrical Engineering, University of Oviedo
LEMUR Research Group
Gijon, SPAIN
garciajorge@uniovi.es

Emre Gurpinar, Alberto Castellazzi
The University of Nottingham
PEMC Research Group
Nottingham, UK
alberto.castellazzi@nottingham.ac.uk

***Abstract*—The present work proposes a solution for an isolated gate driver suitable for SiC MOSFETs. The driver is implemented by means of two small magnetic transformers, to provide the turn-on and turn-off gate signals, as well as the power required for an adequate gate control. The operation is based on the modulation of the PWM pulses with a high frequency (HF) square-waveform signal. The resulting modulated AC waveform is applied to the primary side of the first transformer, and reconstructed at the secondary side to obtain the gate driving signal. Simultaneously, the HF modulating signal is connected to the primary of the second transformer, to provide the required gate drive voltage levels and power at the secondary side, ensuring full range duty ratio operation. Given that both primary side signals are HF symmetrical waveforms, saturation is avoided at both transformers, for any duty ratio operation. Therefore, the proposed solution provides galvanic isolation for power and gate signal transfer with very small core sizes, allowing for an overall size reduction vs. conventional solutions. This enables much more compact designs, which are critical in high-power density applications and multilevel converters. After describing the basic operation, experimental results on a prototype are shown, thus demonstrating the feasibility of the proposed solution**

Keywords—gate driver, SiC MOSFET, Wide Band Gap devices

I. INTRODUCTION

The development of WBG power transistors has introduced a number of challenges in power converters design [1]. One of these challenges is the design of compact, reliable gate drivers suitable for PWM operation, ensuring fast turn-on and turn-off transitions for wide duty ratio operations, ideally 0%-100%.

The usual solution for an isolated SiC MOSFET gate-driver is a combination of an optocoupler plus a dedicated isolated DC-DC converter to supply the output power stage that amplifies the switching signal [2]. The main drawbacks of this solution are the relatively large footprint area of the driver circuit, as well as low dv/dt immunity due the parasitic components in the optocoupler and the isolated DC-DC converters, which can cause harmful circulating currents. Several transformer-based gate signal converters have been proposed in the literature. The solutions based on pulse transformers present the inherent problem of core saturation for wide duty ratio ranges [3]. In the case of using a series blocking capacitor to avoid core saturation, problems arise when fast dynamics are required in the duty ratio command. Several options based on turn-on and turn-off symmetrical pulses have also been reported. However these solutions do not allow full range duty ratio operation and require complex circuitry design for the pulses generation [4][5].

On the other hand, several gate drivers based on modulating the gate signal with a HF waveform have been proposed [6],[7]. Some of these solutions use very high modulation frequencies, in the range of several MHz. In that case, these solutions use resonant converters to obtain adequate power transfer, resulting in complex circuitry to cope with challenges such as high sensitivity to modulation frequency variations, high turn-on/turn-off transient speed requirement, etc. Furthermore, for generic PWM frequency operation, the lack of synchronization between HF and LF waveforms might provide periodical duty ratio glitches. In the case of non-resonant transformers, the modulating frequency is smaller, around 1 MHz. This worsens the synchronization effect. In addition, these devices present a blocking series capacitance to avoid core saturation due the LF PWM component in the modulated frequency, which limits the dynamic performance of the duty ratio. Finally, given that the same core is used for power and signal transmission, the power transfer is limited at very low duty ratio operations.

II. DESCRIPTION OF THE PROPOSED DRIVER

This work aims to solve the issues with the state-of-the-art solution presented in the introduction. Fig. 1 shows a block diagram of the proposed circuit implementing an isolated gate driver. The original pulse waveform, ranging from 0 to 15V, $u_p(t)$, is modulated with a HF signal $u_{osc}(t)$, coming from an analog oscillator. An adapting stage converts the modulated signal into a pure AC signal, $u_{pri}(t)$, at the primary side of the signal transformer TR_1. Provided that the signal presents a negligible DC component, core saturation is avoided for any duty ratio. The signal at the secondary side is then rectified at the output of the transformer, $u_{rect}(t)$, and therefore it provides a reconstructed version of the original pulsed signal. This signal is then supplied to the power device as $u_{gs}(t)$, through a power stage that provides the required voltage and current levels required at the gate of the switch.

This output power stage is supplied from a second transformer, TR_2, A power signal, generated with the same oscillating signal output is connected to the primary side of TR_2. At the secondary side

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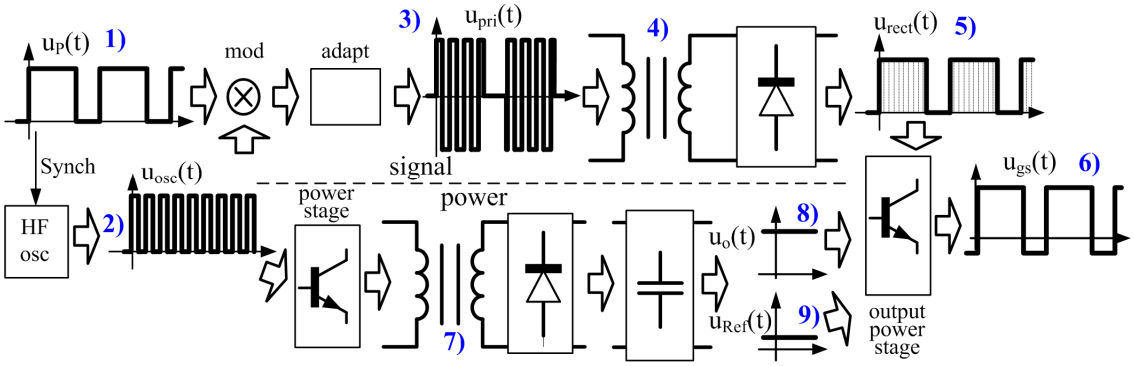

Figure 1: Block diagram of the proposed driver.

of TR_2, a rectifying stage and a capacitive filter provide both an output DC voltage, V_{CC2}, and a voltage reference, $u_{ref}(t)$, that is later used to generate the negative turn-off voltage at the gate driver.

III. SCHEMATIC OF THE DRIVER

For clarification, the schematics for implementing the driver have been divided into three blocks.

The oscillator block, represented in Fig. 3, is implemented by means of discrete HF operational amplifiers (LM6172). The outputs of this subsystem, u_{osc} and u'_{osc}, are two square wave symmetrical waveforms with 180º phase-shift. The importance of the phase-shift will be explained in the following paragraph.

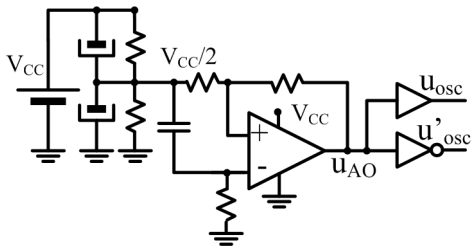

Fig. 3: Schematic circuit of the oscillator block.

The u_{osc} and u'_{osc} are supplied to the two modulators shown in Fig. 4. These devices, wich are also implemented through operational amplifiers and discrete BJT complementary stages, provide the modulated waveforms u_{mod} and u'_{mod}, depicted in Fig. 5. As it can be seen, both modulated waveforms have the same shape, but it must be noticed the 180º phase-shift between signals, coming from the oscillator block. Both u_{mod} and u'_{mod} signals are supplied to the terminals of the primary side of a transformer, TR1. Therefore, the voltage at the primary of this transformer, u_{pri}, has a waveform as depicted in Fig. 5. As it can be seen, this waveform has a negligible DC component, aiming to avoid core saturation for any duty ratio value.

At the secondary side, the waveform is rectified by means of fast Schottky diodes and a resistor, to obtain the reconstructed signal u_{rect}. Due the effect of parasitic elements at the transformer, at the operational amplifiers and at the BJT stages, this signal might present a slight distortion with respect to the original pulsed signal. This distortion is particularly important in terms of the rising and falling edges of the waveform. In order to ensure fast transitions, the waveform is injected to a comparator and to a final BJT complementary stage, to get the signal u_g, that is connected to the gate of the SiC power device.

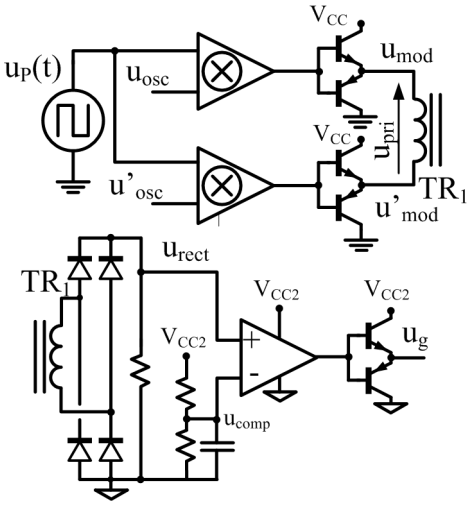

Fig. 4: Schematic circuit of the modulator and demodulator blocks.

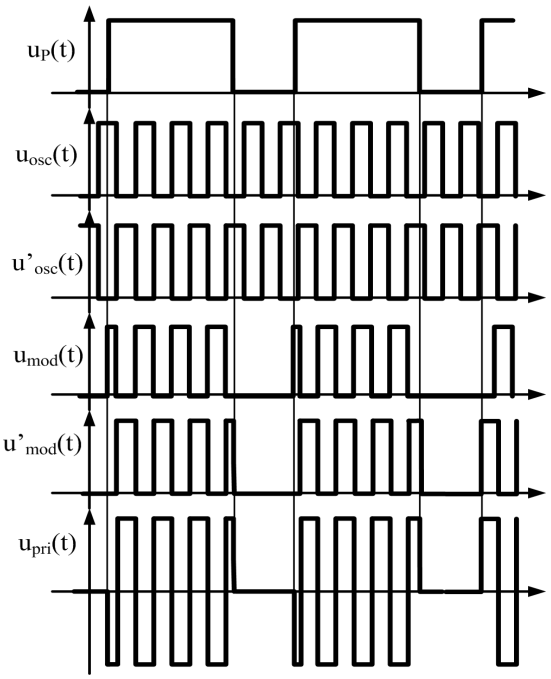

Fig. 5: Schematic circuit of the modulator and demodulator blocks.

The final power block, shown in Fig. 6, uses the input signals coming from the oscillator in order to generate a pure AC HF waveform, which is supplied to the primary side of a transformer, TR_2. At the secondary side, the signal is rectified and filtered, and a regulator provides the reference voltage required to obtain the negative turn off voltage of the driver. This terminal is connected to the source of the power device. Although this approach is indeed a dedicated DC/DC isolated stage, it has advantages versus a conventional power supply. As it is a simple solution, taking benefit of the existing modulating stage, the components count, and as a consequence, the required PCB size is quite small, enabling for better system integration capability. Moreover, the parameters of the voltages can be tuned easily, by adjusting the turns-ratio and the voltage reference, enabling a flexible design for devices with different gate requirements.

Finally, as the transformers in the driver have a custom design, it allows for a full control in the design of the parasitic elements. This enables for keeping under control the parasitic capacitance between primary and secondary sides of the driver, yielding to a high Common-Mode Transient Immunity (CMTI) design of the final driver.

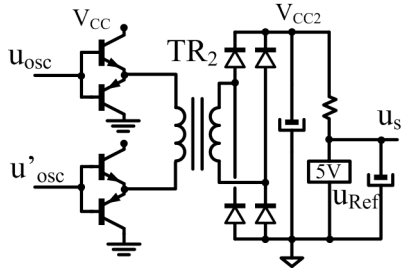

Fig. 6: Schematic circuit of the secondary side power generation and negative reference block.

IV. Simulation Results

A careful design has been carried out and verified through simulations in an iterative process. The characteristic parameters of the commercial SiC MOSFETs have been used in the implementation play a major role in the system performance. The output turn-on and turn-off V_{GS} values are selected as -5V and +20V, respectively. The modulating signal has been chosen as 500 kHz, the input supply voltage was selected as Vcc=15V and the input PWM signal is TTL compatible. The target switching frequency of the design is 100kHz. Figure 7 shows the main simulation waveforms in the gate driver. As it can be seen, the final output waveform has the required parameters.

V. Prototype Characterization

Fig. 8 shows the prototype of the proposed gate driver for a single SiC MOSFET. The oscillator, adapting stages and output signal stages have been implemented through discrete OpAmps (LM7171). The power stage have been implemented through complementary transistors. The transformers have been implemented in TX10/6/4 cores from Ferroxcube. It must be noticed that the prototype shown in Fig. 8 can be significantly reduced in size, as it is a single layer design, with relatively large passive components (SMD2106). A size reduction in a factor of 2 to 4 can be easily achieved. The power consumption of the driver is 3.0W at 100 kHz and 50% duty ratio; a consumption reduction is targeted in future optimizations.

The main waveforms in the prototype at 100kHz operation and duty=50% are presented in Fig. 9. CH1 shows the TTL compatible logic signal coming from the control stage. CH2 shows the input signal after an initial step-up stage up to Vcc. CH3 is the signal from the square waveform oscillator. The oscillator is reset at each falling edge of the control signal in order to avoid pulse glitches at the output when both signal pulses are too close.

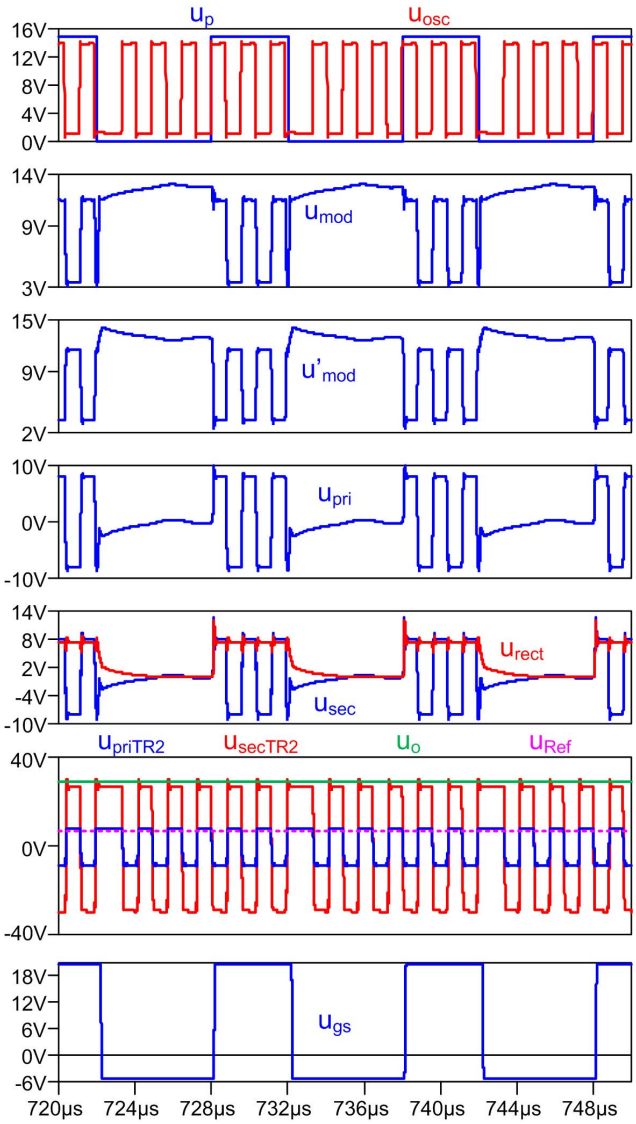

Fig. 7: Simulation waveforms of the proposed driver

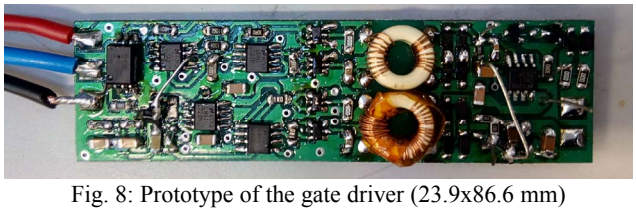

Fig. 8: Prototype of the gate driver (23.9x86.6 mm)

The modulator and adapting stage provides the signals depicted in CH4-CH5. Both signals have the same voltage value (Vcc) at low input voltage, and a complementary modulating signal at high input value. After amplification, each of these signals is connected at the primary transformer terminals, thus the transformer input is directly CH6. At the secondary side, the rectified signal CH7 supplies the output stage (comparator+power stage), to finally provide V_{GS} signal CH8.

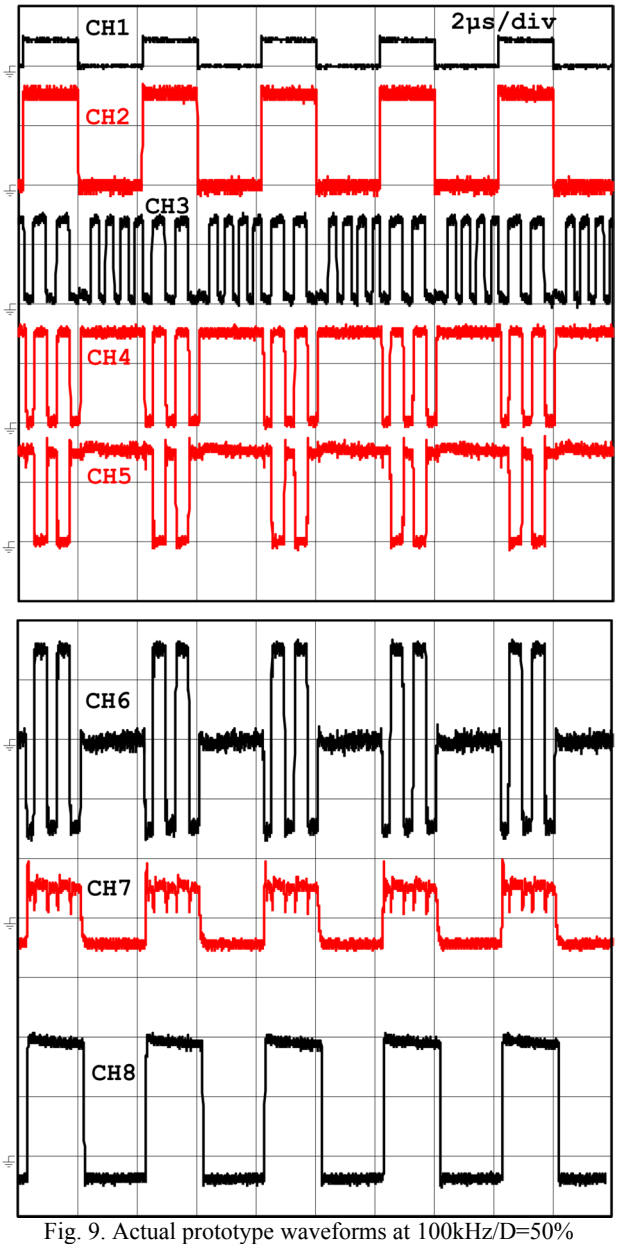

Fig. 9. Actual prototype waveforms at 100kHz/D=50%

The driver has been loaded with different RC circuits that model the gate resistance and capacitance of SiC MOSFETs without drain-source voltage. This is intended to demonstrate the functionality of the design for SiC MOSFETs with different current and voltage ratings in the market. Fig. 10 shows the driver rise and fall times for the given RC combinations (R=0,1,2,5 and 10 Ω, C=0.5, 1, 2 and 4 nF). The driver has been tested at switching frequencies up to 200 kHz, for the full duty range showing good performance.

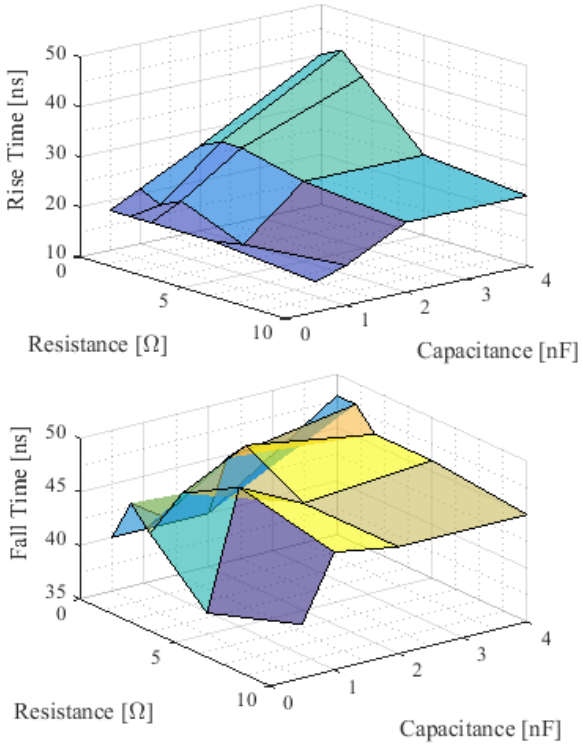

Fig. 10: Rise (up) and fall (down) time at the driver output for several R and C values

VI. Experimental Results on a 2 kW Converter

The performance of the driver has been tested on an existing 400V/2kW DC-DC buck-boost synchronous converter with C2M0080120D SiC MOSFETs from CREE. Fig. 11 shows the main SiC switches waveforms at 100 kHz, 1.8kW load level.

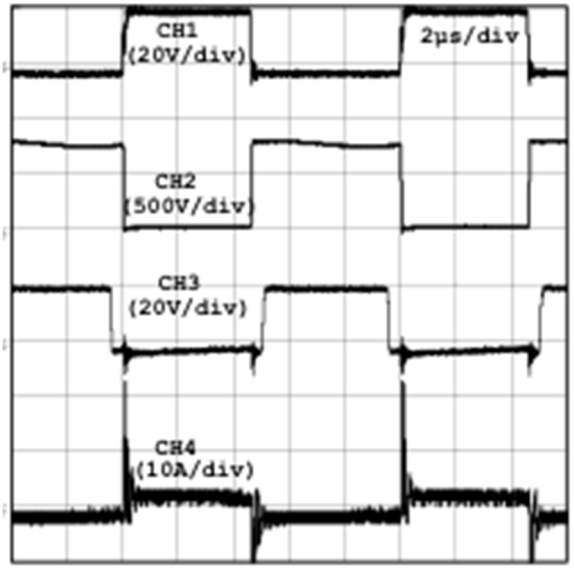

Fig. 11: Experimental waveforms at a bidirectional buck-boost converter. CH1 (yellow): $u_{GS}(t)$ at Switch S_1 (output switch), CH3 (magenta): u_{DS} at S_1. CH2 (green): $u_{GS}(t)$ at Switch S_2., CH4 (blue): I_L (AC). 400V_{dc} input, 100 kHz switching frequency, 5A output.

Fig 12 shows the details of turn on and turn off. As it can be seen, 38 ns rise time and 27 ns fall time are achieved at 800V drain-source voltage. The gate resistor at the driver has been increased from 0 Ω up to 15 Ω to reduce the gate ringing that can be seen in Fig. 13. This ringing is due the resonance between the parasitic inductor of the SiC MOSFET and gate driver and the gate capacitance [8]. Fig. 6 shows the V_{DS} rise and fall times vs. the V_{DS} voltage at 100kHz, 50% duty-ratio and 5A output current.

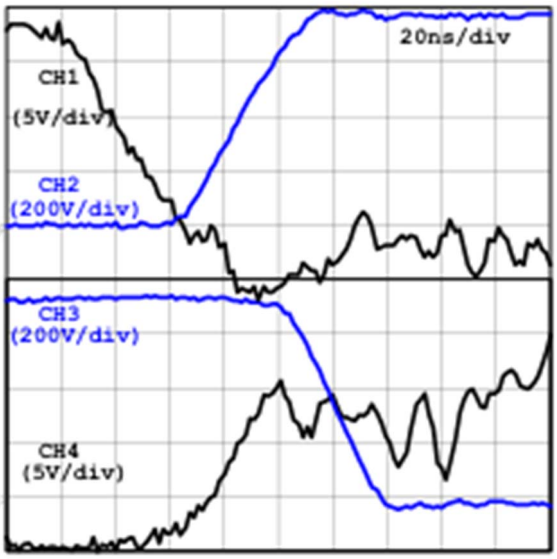

Fig. 12. V_{GS} (CH1) and V_{DS} (CH2) details at turn on and turn off.

Finally, Figs. 14 and 15 show the power consumption of the proposed modulated driver. Fig 14 shows the power consumption of a single driver, at full load of the converter, at f_{sw}=100kHz and f_{mod}=500kHz, for several duty ratio values. As it can be seen, the power consumption is around 3W. It must be noticed that this value is a minimization target for future versions of the driver. Fig 15 shows the power consumption per driver, at full load of the converter, at f_{sw}=100kHz and D=50%, for several modulating frequencies. As it can be seen, an increase of the modulating frequency would yield to higher power losses in the driver.

VII. Conclusions

An isolated gate driver for SiC MOSFETs has been proposed, analyzed, built and tested. The prototype shows good general performance in a 2kW buck-boost demonstrator. The proposed driver allows for simple, compact designs of power converters, with full range duty ratio and switching frequencies up to 200 kHz. The main operation principles have been summarized and demonstrated through experimental validation in a working prototype. The main contributions are the ability of the full range duty ratio operation (0%-100%) in SiC devices with asymmetric turn-on/off voltage values in modulated schemes, the absence of blocking capacitor that allows for high bandwidth operation, the synchronization of the HF and LF waveforms to avoid pulse glitches, the implementation of all the scheme through discrete components and operational amplifiers (that allows for full control of the design parameters such as dV/dt, and enables for high size reduction possibilities).

Future developments include optimization in size and consumption of the driver, decreasing of parasitic elements in the gate-source path in the driver, validation in different WBG devices, inclusion of protections in the driver operation and further optimization of rise and fall time speeds.

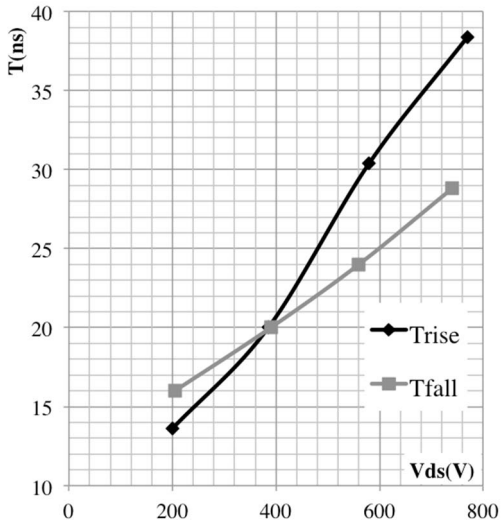

Fig. 13. **V_{DS} rise and fall times vs the V_{DS} voltage, for the converter operating at 100kHz, 50% duty-ratio and 5A output current.**

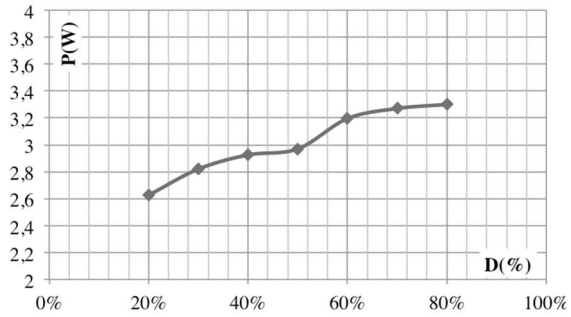

Fig. 14. Power consumption per driver, at full load of the converter, at f_{sw}=100kHz and f_{mod}=500kHz, for several duty ratio values.

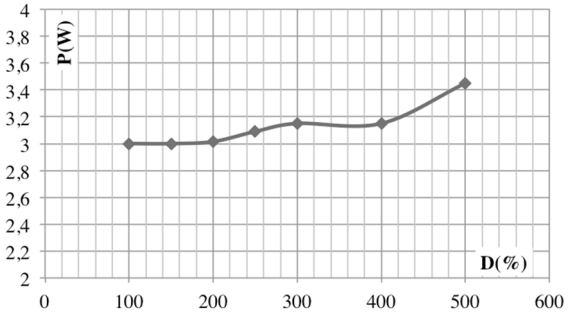

Fig. 15. Power consumption per driver, at full load of the converter, at f_{sw}=100kHz and D=50%, for several modulating frequencies.

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