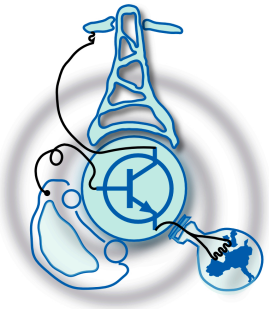
Design, verification and early validation of electronic circuits applied to traction

by

Borja Martínez Fernández



Submitted to the Department of Electrical Engineering, Electronics, Computers and Systems
in partial fulfillment of the requirements for the degree of
Master of Science in Electrical Energy Conversion and Power Systems
at the
UNIVERSIDAD DE OVIEDO
July 2018

Author .....

Certified by .....
Alejandro Saavedra Miner
Company Coordinator
Thesis Supervisor

Certified by .....
Pablo García Fernández
Associate Professor
Thesis Supervisor

Design, verification and early validation of electronic circuits applied to traction

by

Borja Martínez Fernández

Submitted to the Department of Electrical Engineering, Electronics, Computers and Systems
on July 26, 2018, in partial fulfillment of the
requirements for the degree of
Master of Science in Electrical Energy Conversion and Power Systems

Abstract

Nowadays an important part of the innovation process of the new traction products is based on the design or redesign of the electronic circuits. Since current regulations and growing pressure to improve the competitiveness of the sector have been increased, heuristic methods (trial and error) have become outdated. This part of the process is critical for companies from an economic point of view. Because of that, new needs have arisen and early validation of these electronic components in order to incorporate them into the product safely and dependably is mandatory, as long as companies do not want to become overshadowed by their competitors.

This Final Master Thesis (MTh) revolves around design, verification and early validation of electronic circuits applied to traction and their components by the application of electronic design techniques and methods based on high reliability systems. Their implementation has been done by software, more precisely the tool Cadence OrCAD and its complements: OrCAD Layout, OrCAD Capture CIS, PSpice A/D and PSpice Advance Analysis. This project has some critical milestones such as the creation of the components used for the traction circuits, verification of those components, hierarchical design of the whole circuit, verification the behaviour of the different hierarchical blocks, verification of the reliability of the electronic circuits through several methods and test.

Finally, the main objective is not to obtain a simulation in which everything is working perfectly under the desired conditions like other projects involve. The principal aspect of this MTh is focused on obtaining, through the simulation, the failures of the electronic circuit that have been observed during its real working time to fix them by redesigning the circuit in a previous stage to the building state, leading to a significant reduction in the production cost.

Thesis Supervisor: Alejandro Saavedra Miner
Title: Company Coordinator

Thesis Supervisor: Pablo García Fernández
Title: Associate Professor

Contents

List of Figures

List of Tables

Chapter 1

Introduction

Presently vehicles are changing from a traditional model based on fossil fuels to a model based on electricity, which is considered cleaner and with a lower environmental impact. The most common example is electric cars (hybrid or fully electrical), but in this case the most interesting case from the point of view of the project are the electric locomotives.

The European Court of Auditors determined that freight transport contributes in a high manner to the competitiveness and development of the industry in the European Union[1]. However, most of the 75% of this transport are trucks, in other words, freight transport is done by diesel or gasoline vehicles and as a consequence the CO_2 emissions are very high. One of the main objectives of the Horizon 2020[1] is reducing the CO_2 emissions. Railways have been proposed as an alternative, despite the fact that they are a good solution, most of the railways in Europe work with diesel. Although the emissions are reduced, the new regulation adopted on September 14th 2016, in which the emissions of the diesel motors was established, using diesel vehicles has been punished.

This has been a hard blow for the railways, since they did not have a fixed normative in that way. Because of that, there is an increase of electric or hybrid trains, but taking into account that the use of diesel motors is being diminished with time.

[1]The H2020 is a project which tries to improve the global presence of Europe by three principal actions; excellent science, industrial leadership and societal challenges. For more information about the H2020 consult [2]

Most of the railway companies are focusing its production on electric railways.

Ingeteam Power Technologies has a department of electric traction, which has been working several years with electric railways. One of the most problematic parts is the control stage. The present project comes alive due to the failures that have appeared during the development of this control stage, labelled hereinafter Electra. It was born in June 2009 in order to achieve a reduction of 20% in relation to the old system, which was very expensive, it was not specific for the railway sector, it did not operate in an industrial temperature range and most of their components were out of date. The final decision was the design of a new Electra that was adapted specifically to the railway sector. However, there are no simulations, hence, several problems have appeared since then.

The way in which Electra is tested is a build and test method. This is far from ideal because if the traction circuit is not well designed a lot of components or even the whole PCB will result in damage. Of course, the PCB is very robust and has external protections, so that a failure cannot spread to the system. From its birth it has been changing and improving, most of these changes have been focused on enhancing its performance.

The main goal of this MTh is to achieve a real simulation of the Electra to avoid heuristic methods thus reducing the final cost of production.

Chapter 2

Objectives

2.1 Introduction

This section will explain the main objectives that were proposed at the beginning of the project, and how they have been adapted to the necessities of the company. Two kind of objectives can be distinguished: those ones which are more relevant will be labelled as principal objectives, and those ones which are not critical but improve the project will be labelled as secondary objectives.

2.2 Principal projects

Before defining each of them, it is necessary to know how the project was proposed. These were the main objectives for the project.

- Manage the complexity of the design.
- Assignment of the functional requirements to the different design blocks.
- Verification and early simulation of the circuits developed.
- Failure analysis and improvement of diagnostic covered.
- Prediction and improvement of reliability based on de-rated factors and stress models applying design rules.

- Specification of the PCB routing and layout to improve the Power Integrity, signal integrity and thermal integrity.

Every one of them until the last point are going to be achieved through this project. Nevertheless, these objectives are further developed hereunder.

2.2.1 Hierarchical design

The design presented has a lot of elements, and it is very difficult to manage all the system. This can be solved by dividing the system in smaller units.

As it will be seen in the chapters below, the control stage of the control electronics has a lot of elements and different kinds of circuits. Hence, it is very difficult to work with the whole circuit. The solution proposed is to use a hierarchical design, which will reduce the complexity. Thus, it will be easier to manage the whole circuit.

In a first moment the whole PCB was the objective. Nevertheless, the priority changes in the middle of the project to simulate three parts of the system: the Digital Inputs/Outputs, the analog Inputs/Outputs and the encoder.

Only the digital Input/Outputs and the encoder have been developed.

2.2.2 Developent of Libraries

This was not an initial objective. However, since the company does not have any libraries, they have been created from zero. This objective is the most important of the whole project since, as it will be shown below, the single components such as resistances, capacitors, optocouplers and so on, will decide the validity of the project.

2.2.3 Creation of functional blocks

This objective consists on creating different blocks which contain the functional aspects of the circuit but they should be independent of the content thereof. This kind of circuits are labelled as black-box circuits. This point is detailed in the chapter *Libraries*.

2.2.4 Verification and early validation of the design

This part will consist on testing the designed circuits through transient simulations at which the parameters of the design are changed to observe its behaviour.

Inside this part a verification of all the basic components should be done. However, this implies a huge amount of time and other objectives must be reached, as a consequence this part is omitted.

2.2.5 Failure analysis and improvements

This objective is related with the previous one, since through the simulations used to verify the behaviour of the circuit, the failure test to see the operation limits are done.

2.2.6 Prediction and improvement of the reliability

In order to check the reliability of the system, some test based on the de-rated factors and Electrical Overstress (EOS) will be done. These tests are related to each other and in order to do them, a tool of OrCAD will be used.

This will be explained thoroughly in the chapter *Verification Methods* in the section *Advance Analysis*

2.3 Secondary Objectives

2.3.1 Additional simulations

This objective is mainly focused on amplifying the range of validity of the project. Some of these simulations will include EMC analysis, temperature analysis, frequency analysis and so on.

As it can be seen, all of these tests are used to determine the operation limits of the simulation developed.

2.3.2 Design of the footprints

Since Ingeteam Power Technology does not route Electra, this aspect is not very important. However, to further improve the library in case in the future the company desires to route the PCB by itself, having the components with the footprint included, will be a huge advance.

2.3.3 Design Rule check

This objective was in a first moment a main one. However, because of the lack of time, it was not considered relevant and other activities were considered more important.

Chapter 3

State of the art

3.1 Introduction

Nowadays, just as much to the investigation or the development of new products or even to improve the oldest ones, simulation tools are very useful. Simulations allow to identify the critical part of a system, its behaviour and more options. But these characteristics are not the main reason for using software tools to make a simulation. The main reason is to avoid heuristic methods, which are the ones used before the simulation tools appeared.

Heuristic methods are based on building and testing the circuits. These methods, from an economical point of view, are a very bad option, since some of these tests can destroy some parts of the system or even the whole system if it is not well designed. The solution is the one mentioned above, using a simulation software the behaviour of the system could be achieved, thus, a significant reduction of the construction time will be obtained. Furthermore, this process will prevent the degradation of the components and also the expensive measuring instruments that must be used after the prototype is built. In addition, simulation software has the advantage of providing a solid base regarding the behaviour of the system, potential problems can be addressed before the construction of the prototype. In contrast, if the system is not simulated, the time that will be spent looking for failures could be very significant, also these failures could lead to the damage of the components and also the measuring

instruments as it has been said above. This will increase the economic losses of the project.

What is more, having a system with a simulation will result very useful in the future if some improvements are desired to be done. But one of the main challenges of achieving a good simulation is the constant change of the technology, i.e. if the technology advances but the simulator tool remains with the same characteristics, the user will be responsible of developing the new components if an electronic simulation is desired. In this project, an electronic system will be simulated.

3.2 Simulation tools

Through history there have been several software tools used to simulate electronic circuits, one of the first tools was the *Simulation Program with Integrated Circuits Emphasis* also known as SPICE. It was developed in the University of California Berkeley as a class project in 1969-1970 by Donald O. Pederson & Laurence W. Nagel[3].

In a first moment SPICE works with code generation unlike the newest that are being used currently. It should be said that SPICE was the base of other kinds of software simulations.

In this section several tools that are used for simulation will be discussed.

3.2.1 PSIM

This tool is very useful to make fast simulations and get an idea of the behaviour of the system. Its main problem lies in the fact that it does not have a proper tool to route the circuit as other kind of software have.

Its main advantage lies in its simplicity, also it is one of its main disadvantages. As a first software to simulate electronic circuits it is considered the best option.

3.2.2 Altium Designer

Altium designer is a junction of tools used for the electronic design in all the phases. In contrast to PSIM this software allows to simulate the schematics and also it has the option to make the routing of the PCB.

Altium has the following options

- Connection to a data base: this characteristic is used to generate libraries and include them inside a data base, optimizing the process of modelling a library and hence the schematic.
- Visors of PCB and Gervers to see the circuits printed in the technical office.
- SPICE Mixed Simulation: this allows the software to use Spice models.
- Signal Integrity: in order to see the behaviour of the PCB.

3.2.3 Mentor and OrCAD

Both of them are different companies but they are the most competitive ones in the market. They have a wide variety of options when compared to Altium and also PSIM. Both pieces of software offer a huge amount of options; notwithstanding the fact that they are not a single piece of software, they have been fragmented by functionality and the main problem lies in the price of each tool. Hence, if a a complete tool with all the packages is desired a huge amount of money is required.

Typically small companies cannot afford this kind of software with all the packages, then, they often use simpler software such as Altium, which includes more options even when their results are worse.

3.3 Software used in the project

This project is going to be done with the software from CADENCE OrCAD. It has been chosen because it is the one used by the company.

Two packages are needed: the Capture CIS will allow to do the transient simulations and also the development of the components; and the PSpice Advance Analysis, used to do the de-rating factors and also the EOS analysis.

This software has a huge grade of difficulty, which can be considered one of its main disadvantages. Furthermore, it is very difficult to find some models for the libraries, as a consequence the components, most of the times, must be designed from zero. This increases the difficulty of using this software.

The principal characteristics have been addressed, but the main advantages and disadvantages of OrCAD are shown hereunder.

3.3.1 Advantages

OrCAD is characterized for having a wide variety of libraries, this is a very important point since the development of the components is the hardest part of building an schematic. Another advantage is that its interface is not as easy as other software such as PSIM, but it is not difficult. And one of the biggest advantages of this software lies in the power of the analysis which allows to make huge simulations at different ranges of accuracy. It can be said that, if the components are well designed, it can be 100% sure that the behaviour of the simulation and the prototype will be the same. Of course, the variations are allowed, it will depend on the restrictions of the simulation. OrCAD can be defined as a multifunctional tool due to the amount of packages that it includes.

3.3.2 Disadvantages

OrCAD is a software that is very difficult to use at the beginning. Hence, its learning curve is very steep. As it has been explained, OrCAD is formed by several packages that are independent and must be bought at a considerable price.

Chapter 4

Electra

4.1 Introduction

This chapter will describe the Electra, also the different PCBs it involves. In addition, the different parts it comprises according to their functionality, this is the base for establishing a valid design later.

4.2 Description

Electra is the name given by the company to the power electronics placed in the converter.

All the traction elements are integrated inside the converter, whose main function is to transform and adapt the voltage of the cathenary to control the motor.

The first stage could vary depending of the voltage of the cathenary, if it is an AC voltage it should be transformed into a DC voltage with a rectifier and if it is a DC voltage it should be adapted to the desired values. The rectifier is connected to a capacitor (DC-link) which feeds an inverter of IGBTs to transform again this voltage into a controlled AC voltage.

The control is done by the Electra, which is one of the most important parts of the traction system because it has more functions than generating the control signals. It includes several sensors to determine the state of the motor at all times. The way

in which the Electra works is the following:

1. Information reception.

2. Signal processing.

3. Sending information.

These are the main functionalities of the Electra, and they are basically to distinguish the different parts in which it can be divided as it is explained in the section below. Figure 4-1. shows the Electra.

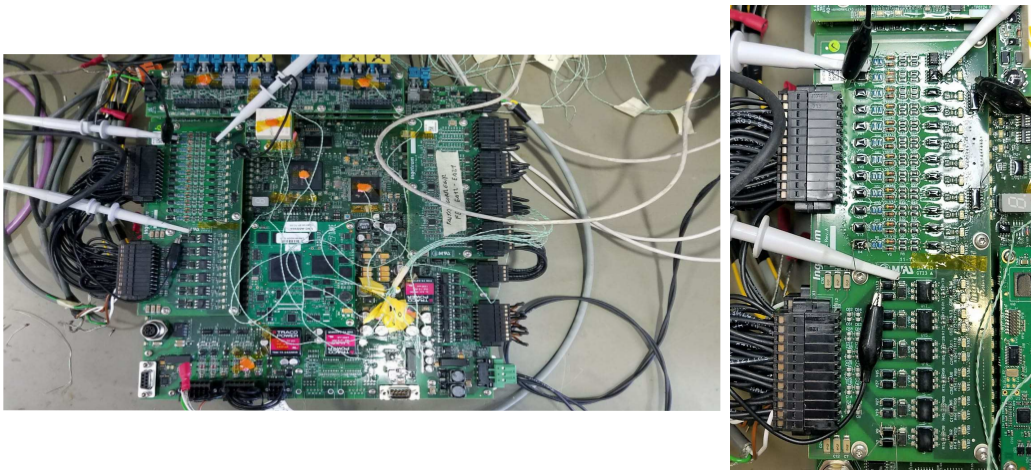


Figure 4-1: On the left side the Electra is shown. On the right side the TB0107 is shown.

Heeding Figure 4-1. several PCBs can be observed. Those PCBs are imposed by design because depending on the operation mode some components must be used or not, hence several PCBs with the same configuration are used to achieve an efficient behaviour. Each of them receives a label to be used from here to the end. The labels are:

- TB1350: it represents the main body of the PCB.
- TB0107: it is the expansion of the digital Input/Outputs.
- TB0106: it is the expansion of the analog Inputs/Outputs.

- TB0145: it is the expansion of the fiber optic and traction cut-off protection.
- TB1006: it is the powerpc.

4.3 Technical architecture

One of the most important parts doing a hierarchical design is to establish the different parts of a system and the interconnection between them.

For the Electra there are several parts that were divided during its development, and they have been taken as a reference for this project. After identifying them, new levels of hierarchy will appear, but this is not the objective of this section. Hence, a brief definition of each part will be given here. Figure 4-2. represents the different parts of Electra.

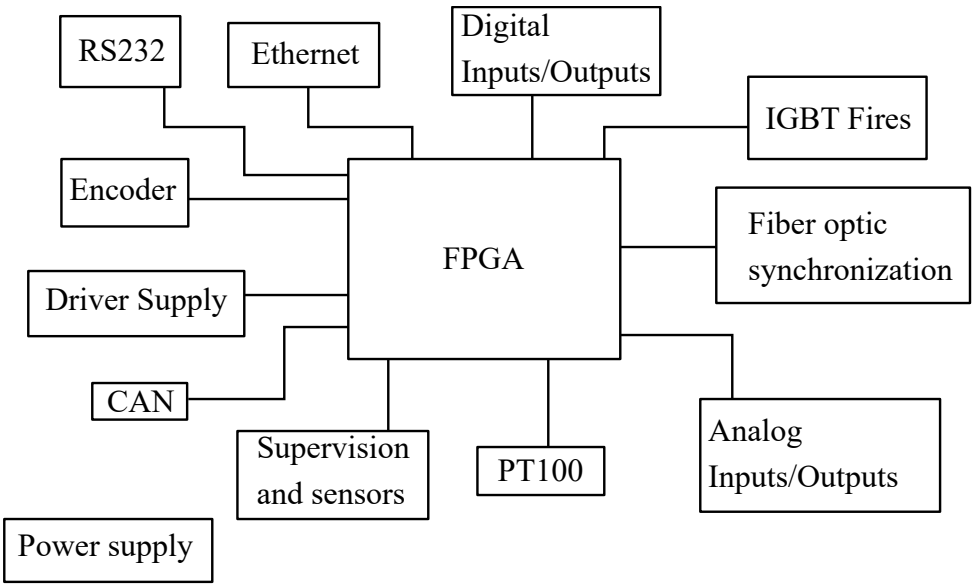


Figure 4-2: Architecture of the Electra

4.3.1 Power Supply

Electra has several components with different requirements of voltage supply, but this does not mean that the PCB should be fed with external voltage sources set at those

voltages. Instead of doing that, a unique voltage source of 24 V is needed, and using this voltage, the rest are generated.

To generate the different voltages, two kind of converters are needed: DC/DC Buck converter or linear regulators.

The main reason for doing that is to reduce the number of external signals. Furthermore, low levels of voltage are used (typically lower than 5V), this will lead to a reduction of the power dissipated and also in the time to swap the state of the system.

4.3.2 Digital Inputs/Outputs

The reference of the digital signals must be provided externally, doing this, the read signals can be compared with the generated ones. Then, an error can be detected easily if there is a mismatch in the results.

4.3.3 Analog Inputs/Outputs

The digital signals generated by the FPGA cannot be used by the analog components; in order to use a digital signal a Digital to Analog converter (DAC) is used. These Inputs/Outputs are often used to track the control at some points. Also they are involved in some Electra drivers.

4.3.4 Encoder

Encoders are used to measure the speed of the motors. The encoder used provides a differential voltage that is later converted into a digital level. The digital output is read by an electronic device which knows how to interpret those signals.

This part is critical, because with the speed of the motors, the speed of the train can be calculated and this speed is the one used in the speed control.

4.3.5 Fire of the IGBTs

This part is very important since the inverter which provides the voltage to the motor is controlled here. The IGBTs fires have two different parts: the fire itself and one

receptor to ensure that the fire has been activated properly. The material used to interconnect the Electra and the inverter is optic fibre because it is faster, safer and immune to Electro Magnetic Interferences (EMI).

4.3.6 External communications

The converter must be able to communicate itself with the outside, and this is done in several ways. Each part will constitute a single unit for the hierarchical design. The different types of communication are:

- RS-232
- TCN
- CAN
- Ethernet

4.3.7 Programmable logic

All the control is done by the following three parts, so they are the most important parts of the Electra.

- Field-Programmable Gate Array (FPGA): it is mainly the coordinator of the control and management of all the signals, since all of those are processed by it.
- Digital Signal Processor (DSP): the signal processing is done by the DSP. Furthermore, it gives a reply for those signals when needed.
- External card: not designed by the company but bought to an external maufacturer. Inside, several protocols such as I2C, CAN, and so on are implemented.

4.3.8 Temperature sensors

In order to ensure safety limits of operation, and also secure the efficiency of the converter, the temperature inside is measured.

Temperature is an important factor to have into account, since the converter is an hermetic box and all the components inside it are dissipating power, that means heat generation. If the heat cannot be dissipated correctly the components could be damaged. The biggest point of heat generation corresponds to the IGBTs because they have two kind of losses, the switching losses due to fast commutation and the power losses.

Chapter 5

Hierarchy systems design procedure

5.1 Introduction

In this chapter the working methodology is going to be described. This section is very important to understand how the whole project has been designed, it is quite difficult summarise the project in a linear description since it is based in a trial and error system, it means that several times a redesign of some components or also the hierarchy must be done. With this chapter is intended to clarify the main structure that has been followed.

5.2 Work-flow

As it has been said above in the introduction of the chapter, there is not a linear work-flow in this project. Figure 5-1. shows a flowchart with the work-flow of the system.

The working methodology is the one shown in the flowchart, as it can be seen there are two main actions, which are identify the different parts in which the Electra can be divided. These parts must be clearly identified, because if this is not done, the hierarchical design will not have a solid structure. Simultaneously to identify the

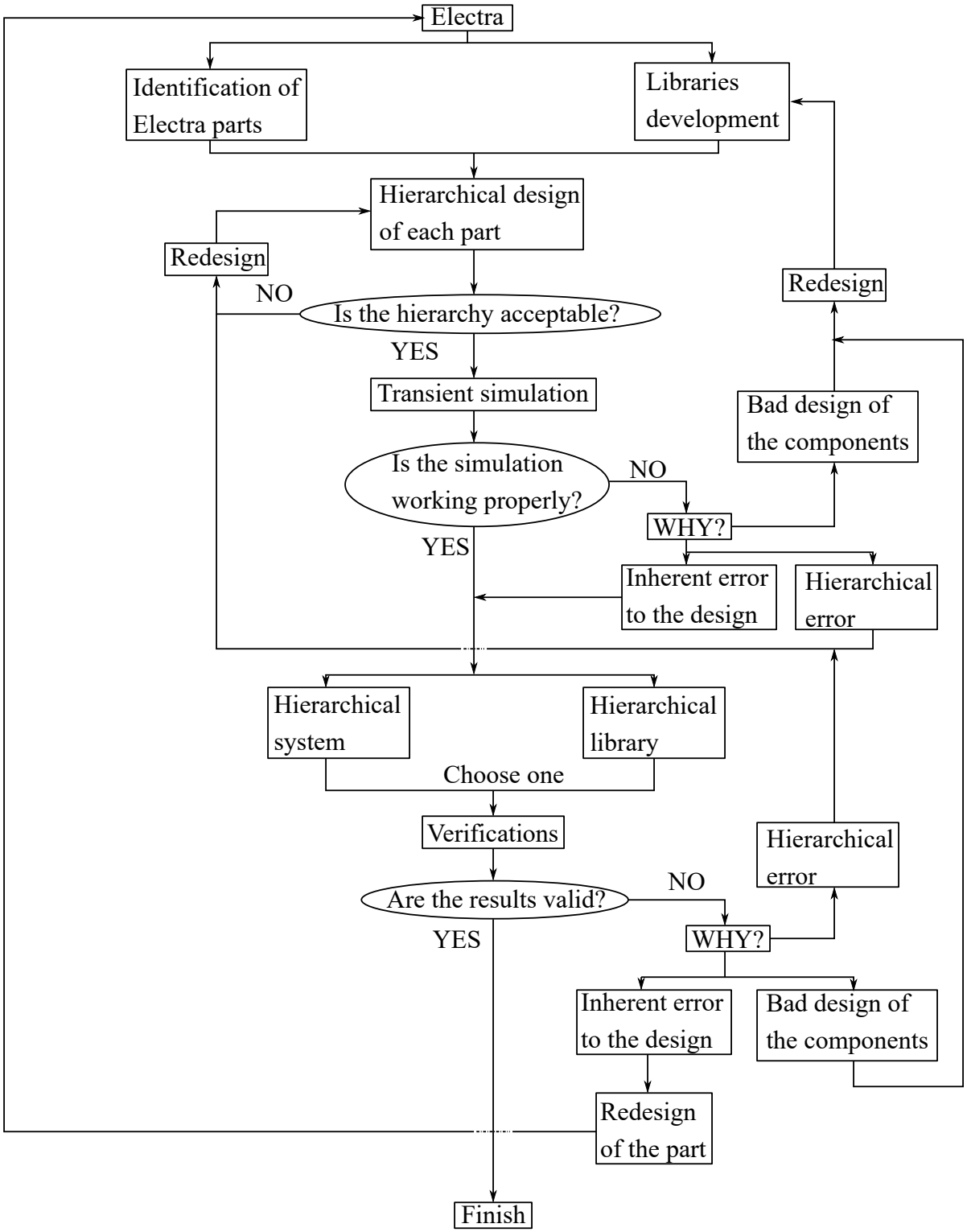


Figure 5-1: Flowchart showing the design procedure followed in the project.

parts consists on developing a library formed by all the components of the Electra. This will facilitate later doing the design, how the libraries have been developed will be explained in the chapter *Libraries*.

After completing both steps, a hierarchical design of one part must be achieved. Once the design is finished it should be see if it is right to its purpose, in case that it is not, they a redesign must be done until it is acceptable.

Having the design, the simulation stage can be started, and again exits the possibility of having errors in the system. However, this errors could came from three different paths.

- Bad design of the hierarchy: the procedure to fix this error is the same that the one mentioned above, doing a redesign of the hierarchical system.

- Bad design of any component: in this case the components which are not behaving as it expected should be replaced or redesigned by others which works correct.

- Bad design of the PCB: if the other errors have been checked and they are not the problem, it is possible that the original system have some error. Hence, at this point for this moment there is not any possible solution, and the working flow must continue to the next stage.

The last stage consist on doing the verifications test, but at this point the same errors that have been seen for the simulation could appear. However, at this point thanks to the verifications test, it is possible to see what are the problems of the PCB, thus, at this point a redesign of the PCB can be done.

Chapter 6

Libraries

6.1 Introduction

This chapter will explain one of the critical parts of the project, because if the components are not designed correctly, the results obtained will not be valid. However, as it has been explained in the chapter *Hierarchy systems design procedure*, every component can be upgraded if a better model can be achieved or even if it needs replacing. These actions will be done with the minimum effort, because the project has been designed taking those problems into account.

6.2 Creation of the components

The first step to create the components was to identify all the components required and to classify them into families. This families are the base of the libraries, but this will be explained below, this section is focused in the development of the components.

It should be clarified that all the components are known, there is not any stage of design. Then, only the creation of the libraries and the simulation of the real case are the goals of this project. Several components have been obtained from the PSpice library, others have been obtained from the manufacturer and when not any model was found, they have been created from zero.

There is an important part that should be understood before continuing: the

PSpice components comprise two parts. The schematic is the visible part, how the components are represented, they could include some parameters that define their behaviour, but they cannot be simulated. The second part is the most important one, and it is the model, it defines the behaviour of the component. If this model is wrong, the simulation will fail, then, if an error takes place, the first step should be reviewing the model.

There are two kind of models:

- **Model**: this file is the basic unit. Inside it, it is possible to see the characteristic parameters of a component such as: the tolerance for the resistors, the breakdown voltage of the diodes and so on. Each component has its own characteristic parameters that can be extracted from the manufacturer's data-sheet or with specific equations.

- **Subcircuits**: as it names indicates, it is a model set. It is used for systems with a high level of complexity in which only the input and the output is desired, also it could be used to design a new component based in less complex elements.

Inside the model the limits for the smoke analysis should be included. It does not matter if there is a model or a subcircuit. However, it should be taken into account that not all the components have the option to do the Smoke Analysis e.g. solid state relays are not allowed in this kind of analysis. This will be explained in the chapter *Verification methods*.

Not all the components are going to be explained, since most of them have been found in the PSpice libraries or the model has been given by the manufacturer. Other models have not been created yet because they are not needed for this project.

Only the components of the TB0107, TB1350 digital I/O and encoder will be explained, since they are the only ones which will be used.

6.2.1 Resistances

The basic element of the PSpice library has been used. In this case the model has all the relevant properties. The model of the resistor has been configured as equation

(6.1) shows:

$$\begin{gathered} .model \quad R\text{^}@REFDES \quad RES \quad R=1 \quad DEV=@Tolerance\% \\ TC1=@TC1 \quad TC2=@TC2 \end{gathered} \tag{6.1}$$

This sentence is the most important part of a component because it establishes a relation between the model and the schematic. All the models have the same structure, then, knowing its meaning, the rest of models can be linked.

It can be translated as: The model of the resistor R with the reference REFDES (this represent the name given in the schematic e.g. R1, R2 and so on) modelled as a fixed resistor (R=1) has a deviation DEV and a linear and quadratic temperature coefficient (TC1 and TC2) of '*@Tolerance%*','*@TC1*','*@TC2*' respectively.

Paying attention to the equation (6.1) it is possible to see that there is not any value inside it, this is because there are two ways of defining those values. The first one consists on defining inside the model and when the simulation is executed the programme will search those values, the second one is based on creating a field inside the element and giving the values in that field.

Ascertaining the best method depends on the component. In this project a combination of both methods has been used, defining inside the model those values which are fixed and are not going to vary and those ones which can vary use a field inside the schematic. The advantage of doing this is that elements such as resistors, capacitors and so on will have a generic model and characteristics.

6.2.2 Capacitors

There are three types of capacitors: ceramic, electrolytic and tantalum.

Ceramic Capacitors

Ceramic capacitors have been modelled as the resistances. The model has been configured as equation (6.2) shows.

$$\begin{aligned} &.model \quad C\text{^}@REFDES \quad CAP \quad C = 1 \quad DEV = @Tolerance\% \\ &TC1 = @TC1 \quad TC2 = @TC2 \quad VC1 = @VC1 \quad VC2 = @VC2 \end{aligned} \tag{6.2}$$

For this model two new characteristics have been added to the model. Those ones are *VC1* and *VC2* which represent the linear and quadratic voltage coefficient respectively. These values represent the variation of the the voltage at different temperatures of the capacitor. Furthermore, the initial voltage across the capacitor can be defined adding a property labelled *IC* which means Initial Condition.

Electrolytic

The model used is the same that the one used for ceramic capacitors. It should be known that capacitors behaviour is directly related with the frequency at which they are working. This fact is shown in Figure 6-1b. Since, $\omega = 2 \cdot \pi \cdot f$, and also it can be demonstrated with the equations (6.3) and (6.4). In this case a simplified model is being used since the frequency is not a fixed value[1]. Nevertheless, a general model with a script file done in Matlab has been developed, in case that the circuit is simulated under a certain frequency. The equivalent circuit of an electrolytic capacitor is shown in Figure 6-1.

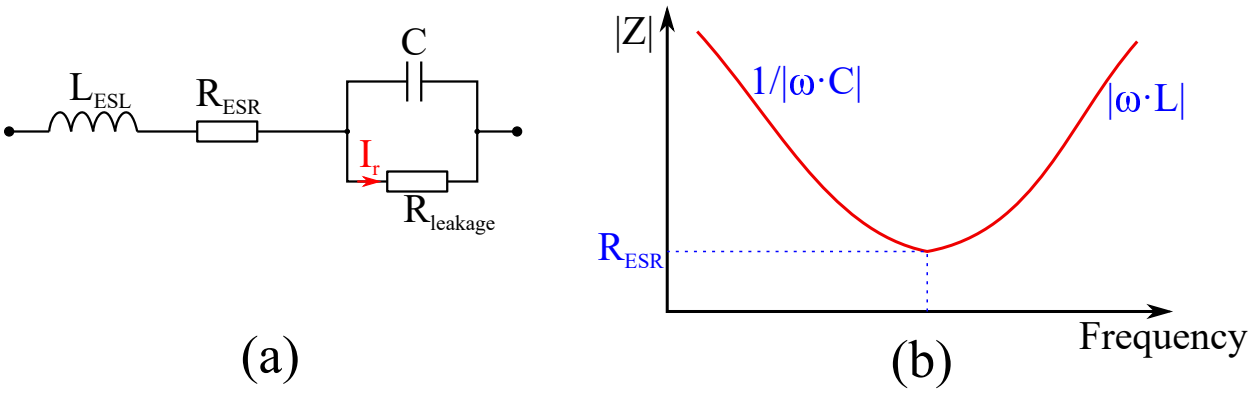


Figure 6-1: (a) Equivalent circuit of a real capacitor. (b) Capacitor impedance against frequency curve.

[1]Using an accurate model which shows the inductive or capacitive behaviour at different frequencies does not make sense because the model will only be valid at this frequency.

Where:

- ESR is the equivalent series resistance. This resistance represents the variation of voltage between the terminals of the capacitor. Typically, manufacturers offer capacitors with low values of ESR because depending on the circuit this value could affect its performance. The equation (6.3) models the ESR is:

$$ESR = \frac{D_f}{2 \cdot \pi \cdot f_0 \cdot C} \tag{6.3}$$

  Df being the dissipation factor, f_0 the resonant frequency and C the capacitance.

- IR is the leakage resistance. It is used to represent the path of the discharge current (Leakage current). It is given by the manufacturer or can be calculated from the ripple current using Ohm's law.

- ESL is the series inductance typically calculated from the total series impedance of the equivalent capacitor model. The equation (6.4) is used to calculate the ESL.

$$ESL = \frac{1}{(2 \cdot \pi \cdot f_0)^2 \cdot C} \tag{6.4}$$

If this procedure is followed, the model should be built as a Spice Macro Model.

Tantalum

The way of modelling is the same that the one seen for the electrolytic capacitors. The only difference between them is the range of use of each one.

6.2.3 Light-Emitting Diode

There are two different LEDs inside the circuit, one of them has been found in the manufacturer's libraries, the other has been developed from the equivalent circuit.

A LED is equivalent to a constant voltage load, Figure 6-2. shows the equivalent circuit[4].

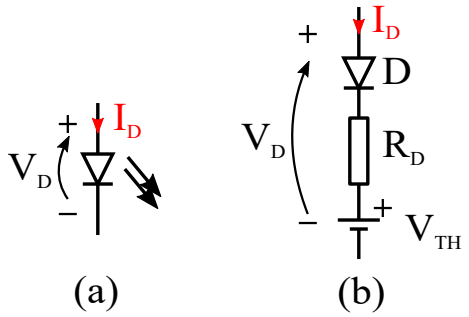


Figure 6-2: (a) LED and its characteristic measurements. (b) Equivalent model of a LED.

Where I_D

- I_D is the forward current, it can be computed by the Shockley equation (6.5).
- V_{th} is the threshold voltage that can be calculated from the gap energy (6.6).
- R_D is the equivalent resistance that is calculated from the voltage of the diode V_D and I_D as equation (6.7) shows.

The diode has not been modelled since one with similar characteristics has been found. The equations which models the LED are the following:

$$I_D = I_S \cdot e^{\frac{eV_D}{\eta KT}} \tag{6.5}$$

$$V_{th} = \frac{E_g}{e} \tag{6.6}$$

$$R_D = \frac{\partial V_D}{\partial I_D} = \frac{\eta KT}{e} \cdot \frac{1}{I_D} \tag{6.7}$$

The parameters that model equations (6.5) to (6.7) are:

- I_S: reverse saturation current.

- E_g: gap energy of the junction.
- e: electron charge $1.6022 \cdot 10^{-19}$.
- k: Boltzmann constant $1.3807 \cdot 10^{-23} J/K$.
- η: ideality factor, 1 for ideal diodes and from 1 to 7 to real diodes.
- T: temperature measured in Kelvin.

These equations are the basic equations used to model a LED, it is true that the parasitic resistance and the effective series resistance at high currents have not been highlighted. Furthermore, the easiest way to model the LED is to do this graphically from the I-V characteristic curve.

The model achieved is very accurate, but the same problem that happens with the capacitors arises, there are some parameters that change with temperature. Hence, if a variation of the temperature is produced, the model will not be valid. Then, that model is included in the libraries but one with similar characteristics is used. In addition, this is not an important part of the circuit in this simulation[2].

6.2.4 Elements not modelled

The rest of elements such as Transient-Voltage-Suppression diodes (TVS), Zener diodes and the Schmitt-Trigger Inverter have been found in the manufacturer's library. Then, only the schematic has had to be drawn.

6.3 Libraries types and structure

Once all the components have been created, they must be organized in different libraries. Three type of libraries from the most general to the most specific are going to be done, even the libraries are explained in this chapter, some of them cannot be built right now, a process of validation must be done, but this is going to be explained later.

[2]It is used to identify if the optocoupler output voltage is 0 or V_{High}.

6.3.1 General libraries

This libraries are based on their functionality, the elements are separated in big groups which are independent from the PCB. This library has been made-up with the final objective of validating the components developed. However, due to the lack of time this part cannot be done.

6.3.2 Specific libraries

In this part the libraries maintain the elements in their functionality, however another grade of classification is added. This is the PCB location and also the functionality. Figure 6-3. shows the structure followed to develop the libraries.

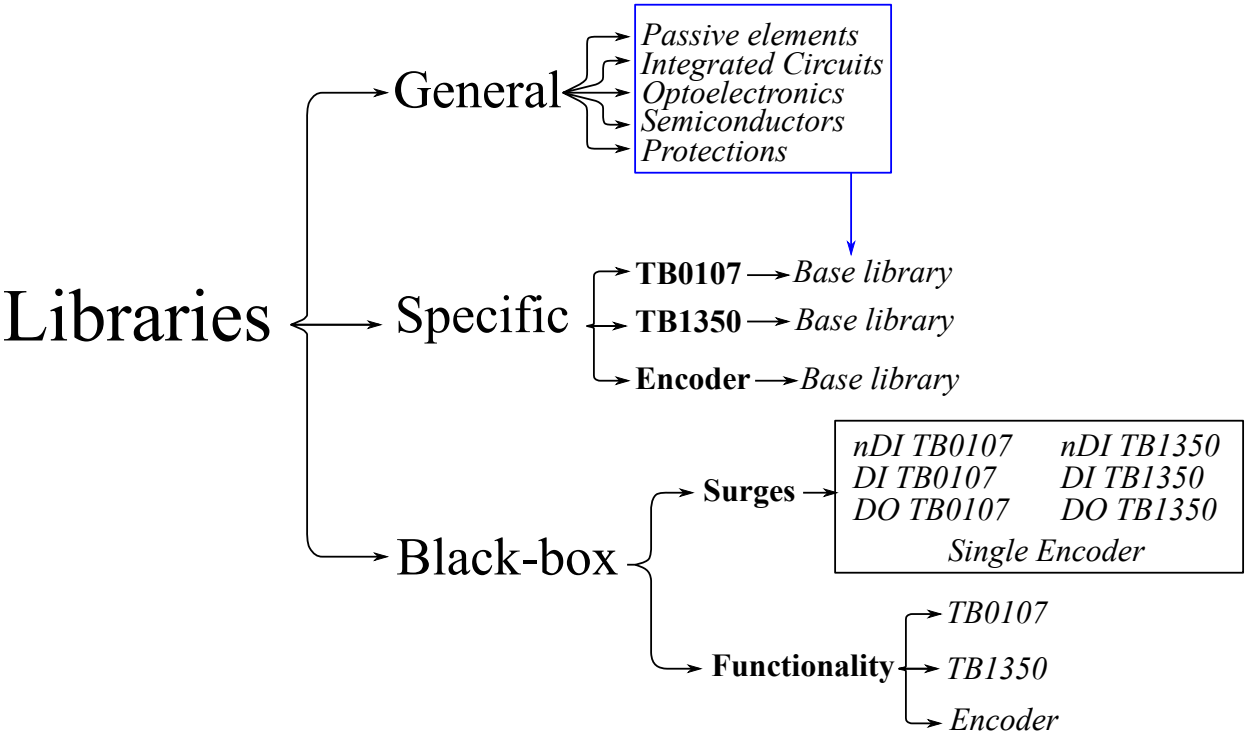


Figure 6-3: Organization of the project libraries.

The main objective of these libraries is to classify the elements based on the part of the circuit to be simulated. This will facilitate the stage of drawing the schematic.

6.3.3 Black-box libraries

All the libraries seen above are the base of the project. Thus, they must be developed at the beginning of the latter. However, this kind of libraries are considered the final project, as it has been seen in Figure 5-1. Once the schematic has been tested and the simulation is considered valid, this kind of libraries can be built but previously, it is important to define the concept of a black-box design. A black-box design is a common strategy used in simulation software in which once an element is tested and it is proved that its functionality at different scenarios is the appropriate one, a new element which contains the whole functionality is made. This has the advantage of reducing the design time, and it is also a simplification for the user because the most important part of the component is not how it has been made, but its whole functionality.

These libraries, as it has been said, are the final objective together with achieving a valid simulation. They are based on having inside the library several stages (hierarchical design) of the Electra and using those elements instead of building the circuit. In order to understand it better, this idea will be compared with other well-known software , Matlab-Simulink.

In Simulink there are two possibilities to build a PI controller: with the use of gains an integrator and an addition block or with the use of a block called PID controller in which that simple structure is included (this block is also known as a black-box design). Extrapolating this idea to this project, e.g in the TB0107, the simple structure will be the one which has been made with the specific libraries and the block with the functionality will be the elements of the new library. These new elements could represent a part of the TB0107 or even it is possible to achieve a simple element with the whole functionality of the TB0107 thus achieving a black box design.

Chapter 7

Hierarchical design

7.1 Introduction

This chapter is focused on explaining what is a hierarchical design and the different methods that exist to make it. Later, the final hierarchical design will be explained and also how the *black-box libraries* explained above are built.

7.2 Definition

As it has been said in the objectives, one of the main goals of this project is managing the complexity of Electra, this can be done by using a hierarchical design. This type of designs are essential in projects with a huge amount of information, normally the concept of hierarchical design is used for Computer Science and Engineering [5]. This kind of design is very useful when it comes to understanding a system, in other words, the system is reduced to systems with less information in order to identify its different parts. This division is set by the user and is different depending on who is doing the hierarchy, then, several possibilities can be achieved and all of them could be valid. A system which does not have levels is labelled as flat system, this one is the starting point of the project.

When a hierarchical design is used, the complexity and the size of the project are relegated to a second place because the main characteristic of a hierarchical design

is to divide the systems in simple units in order to have a better knowledge of it. Nevertheless, there are some critical factors that should be taken into account to achieve a good hierarchical design, those factors are shown hereunder.

Hierarchy

Hierarchical designs are useful high-level tools used to break the complexity of the project into small pieces that are more understandable and can be interconnected.

Modularity

Identify the different functions of the system in order to separate them in different modules. This part is one of the most important, since at this point the system must be understood to establish the different relations. This is critical since there are some excisions that can be done in the software, but in a real implementation does not make sense as it will be seen below.

Resiliency

The system must be prepared for working at his equilibrium point and also under abnormal conditions at least for a short period of time[1]. This characteristic strongly depends on the kind of system and the conditions under which it has been tested.

Flexibility

It consists on giving the ability to modify portions of the system in a short period of time, this can be done because a hierarchical system is based on making only one module and copying that module. These modules are interconnected, thus if a change is applied to any of them, this change will be automatically reproduced in the rest of the modules. Although this characteristic is very useful, it has a clear handicap, that is, if only one module is desired to be modified it cannot be done, and a new module which is not related with the other must be done.

[1]For this reason some models explained above such as capacitors or LEDs are not valid, because they will lead into a bad behaviour out of their equilibrium point.

Previous to explaining the strategies it is important to define the levels of a hierarchical system.

7.3 Levels in a hierarchical system

To prioritize a system there are not any defined rules or methods, because the hierarchy is based on the preferences of the person who is developing it. However, there are two consolidated strategies, both are very basic and have the same objectives: obtaining a modular functional design.

There are several levels in a system, but the most basic is the first level, also known as primitive. The primitive elements are those ones which cannot be decomposed in more elements, this can be clearly understood looking at Figure 7-1.

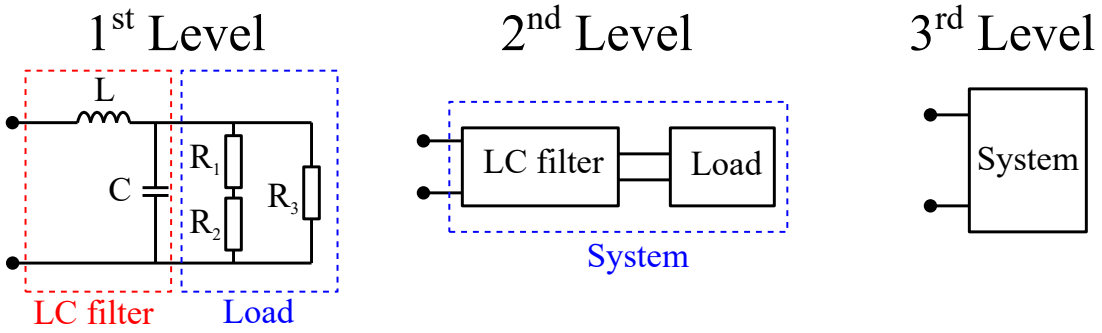


Figure 7-1: (a) Primitive elements. (b) Second level of the hierarchy. (c) Third level of the hierarchy.

Heeding the figure, it is possible to identify several levels, the LC filter and the load are both first levels. This is because they are formed by simple items which are the inductor L, the capacitor C, and the resistances of the load R_1, R_2 and R_3. If the LC filter and the load are included inside a subsystem each of them are a second level, and if the load with the LC filter is included inside another system a third level will be achieved. There is not any limitation of levels, and it should be clarified that different levels can be interconnected. Summarizing, the most important part consists on identifying the primitive elements of the system in order to build the different levels around them.

7.4 Design Strategies

As it has been said above there are two kinds of strategies: the Bottom-up method and the Top-Down method.

7.4.1 Bottom-Up method

This method is the most widely used given its simplicity. The Bottom-up method is based on starting the design from the bedrock of the system, i.e., starting the design from the primitive elements and later ascending to the most complex systems.

First of all, the simpler systems should be identified, then an ascendant hierarchy should be established by adding complexity to the system.

7.4.2 Top-Down method

This method is the opposite of the previous one, it is more complex because a general vision and a high level of knowledge of the system are required. The system hierarchy is built from the most complex structure and it is decomposed into a descendant hierarchy until the primitive elements are reached.

7.4.3 Practical example

Using the example to identify the levels shown in Figure 7-1. To support the explanation both methods has been done based on the example as Figure 7-2. shows.

As it can be seen in Figure 7-2. both methods reach the same solution by following different paths, this is very important since it gives the designer some degrees of freedom at this stage.

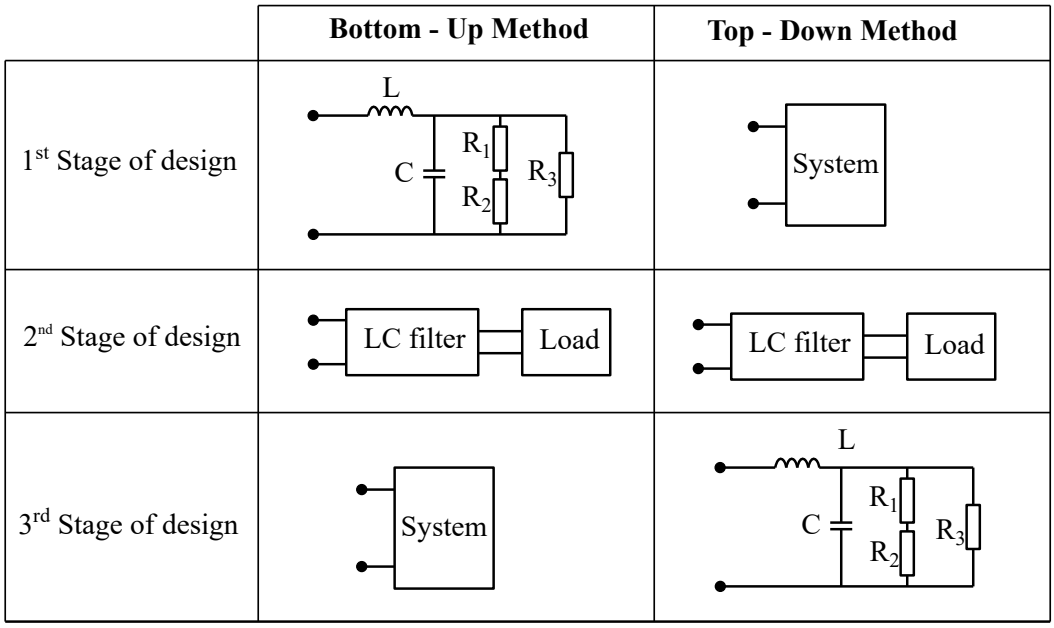


Figure 7-2: Hierarchy methods and their metodology: left side Bottom-Up method. Right-side Top-Down method.

Chapter 8

Versions of the hierarchical model

8.1 Introduction

This chapter will explain all the versions that have been achieved previously to the final version which was validated by the company. All the errors that were found will be exposed and the improvements made will be discussed.

8.2 Digital Inputs/Outputs

As its names indicates, the TB0107 is a PCB which is only composed by Digital Inputs and Outputs (I/O). Heeding the schematics given by the company, three different circuits can be distinguished: the digital inputs, the fast digital inputs and the digital outputs. Figure 8-1. shows the schematic which corresponds to the aforementioned parts.

Once these three different circuits were identified, the hierarchical design could start.

8.2.1 Digital Input and Fast Digital Input

Since they are quite similar they were treated as only one schematic. In the first design, this characteristic was the base of the hierarchical design, the circuit was

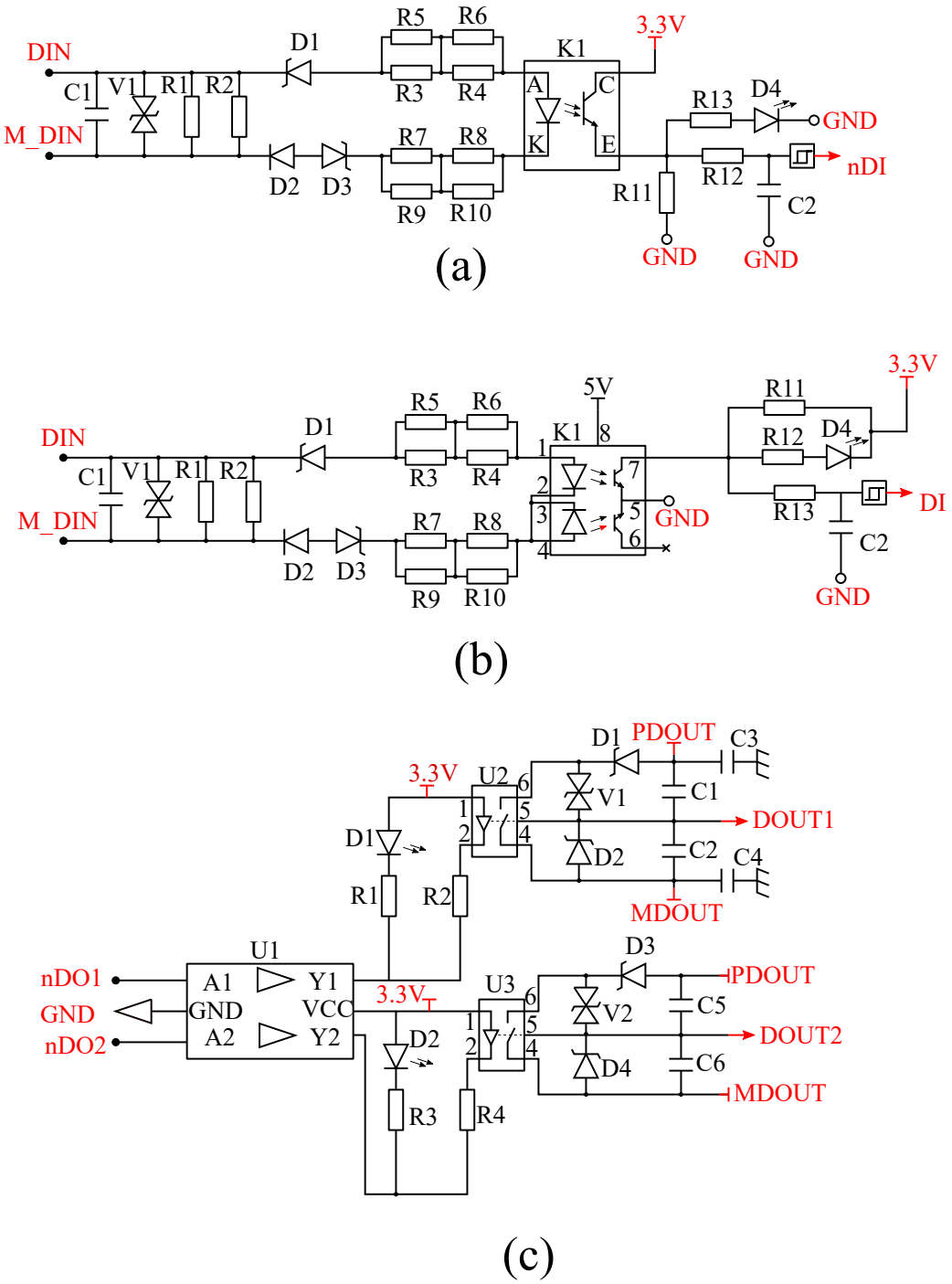


Figure 8-1: (a) Digital Inputs TB0107. (b) Fast Digital Inputs TB0107. (c) Digital Output TB0107.

divided into the common parts of both circuits in order to create the lowest number of modules possible. The configuration is shown in Figure 8-2.

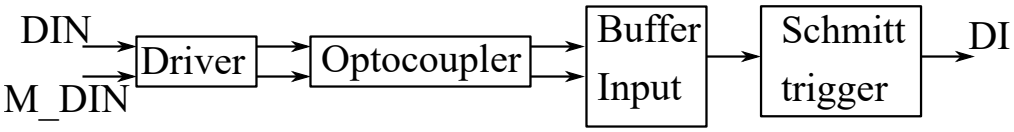


Figure 8-2: First hierarchical design for the Digital Inputs.

As it can be seen in the figure the idea was to create several modules which make the system able to perform any change in the easiest possible fashion. There are four stages defined clearly.

- Driver: this part is responsible of adapting the input signal to adequate levels of voltage and current. This is done because the optocoupler uses a LED and they cannot be fed at high levels of voltage or current, thus the driver is a junction of resistances, capacitors and so on used to protect the optocoupler.

- Optocoupler: the optocoupler is an element used to provide isolation to the circuit. This kind of elements is very useful to avoid Electromagnetic Compatibility (EMC) problems, this is done by isolating the grounds of the input and the output of the optocoupler. This is also done because they are fed by a DC/DC voltage source which generates its own zero voltage.

- Buffer Input: this part is used to correct the voltage level given by the output of the optocoupler to certain values; these values are defined by the data-sheet of the Schmitt trigger.

- Schmitt trigger: it is used to convert the analog voltage into a digital signal which goes to the micro-controller in order to test if everything is working properly.

These parts in which the system was divided will be the base at any point. The design was not a bad idea, and it easily gives the system a wide range of possible configurations. However, the advantage of this design is also its biggest disadvantage: due to the amount of modules that were needed to build a single schematic, this idea was discarded, because when the rest of inputs were implemented a huge number of

levels were going to be achieved. This will make a design quite difficult to understand. Furthermore, if an error is produced, it will be very difficult to find and fix, thus, a simple design was implemented.

The second design was focused in the whole input as it can be seen in Figure 8-3.

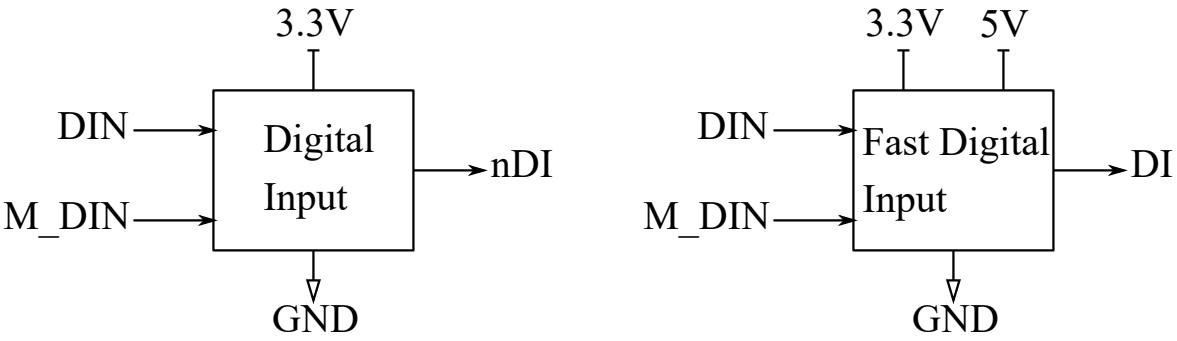


Figure 8-3: Second hierarchical design for the Digital Inputs.

This configuration gives simplicity to the system, and it is the version which has been used to make the simulation. Nevertheless, it poses a risk: the Schmitt trigger. This error is not a functionality error, it is related with the Bill Of Materials (BOM).

Inside the components several properties can be defined, and those properties can be extracted to an Excel document (label, manufacturer and so on). But one of the most important properties is the quantity of the components. This design represents a problem in this aspect, because the proposed hierarchical system does not identify parts of the components. In the schematic one input only uses 2 pins (I/O) of the Schmitt trigger, but it is a DIP-7, hence the other pins are used for the rest of the digital Inputs. As it has been said above, this hierarchical design does not detect the parts of the Schmitt trigger, hence if this module is copied, for example three times more, a total of four digital inputs are achieved, but there will not be a single Schmitt trigger, four Schmitt triggers are going to be found in the BOM. From the point of view of functionality, this does not represent any problem, but for the company it is a big deal, since they extract the list of materials from the schematic.

At this point a valid design for the simulation was achieved, but it was not valid in all the aspects, thus two ways of hierarchical design were achieved. These two

models are the ones used to make the black-box libraries. Since it is not complex, this process has been adopted for the digital output and also the encoder. Both models are summarised below.

Simulation models

These are the models proposed above in Figure 8-3. They will be used to do fast simulations. They are less complex than the rest of the models and will be useful for certain tests such as the surges test.

Final design

This model is based on the *simulation model* but it fixes the problem with the BOM, just by separating the Schmitt trigger and generating a module with all the inputs and outputs. This will separate the analog part which is the driver, the optocoupler and the buffer input from the Schmitt trigger, avoiding the aforementioned problems. Figure 8-4. shows the new and definitive configuration that will be applied to the rest of circuits.

8.2.2 Digital Outputs

Even if the schematic is different, the same procedure can be applied to the Digital inputs. Two models are achieved, one for simulation purposes and other in which the analog components are separated from the digital ones. Figure 8-5. shows both hierarchy modules.

8.2.3 Final design

Until now only the basic modules of the inputs and outputs have been achieved. In order to have the whole PCB, those different modules must be interconnected. Since the number of inputs and outputs are the property of Ingeteam Power Technologies, only a reduced version is presented in this project as Figure 8-6. shows.

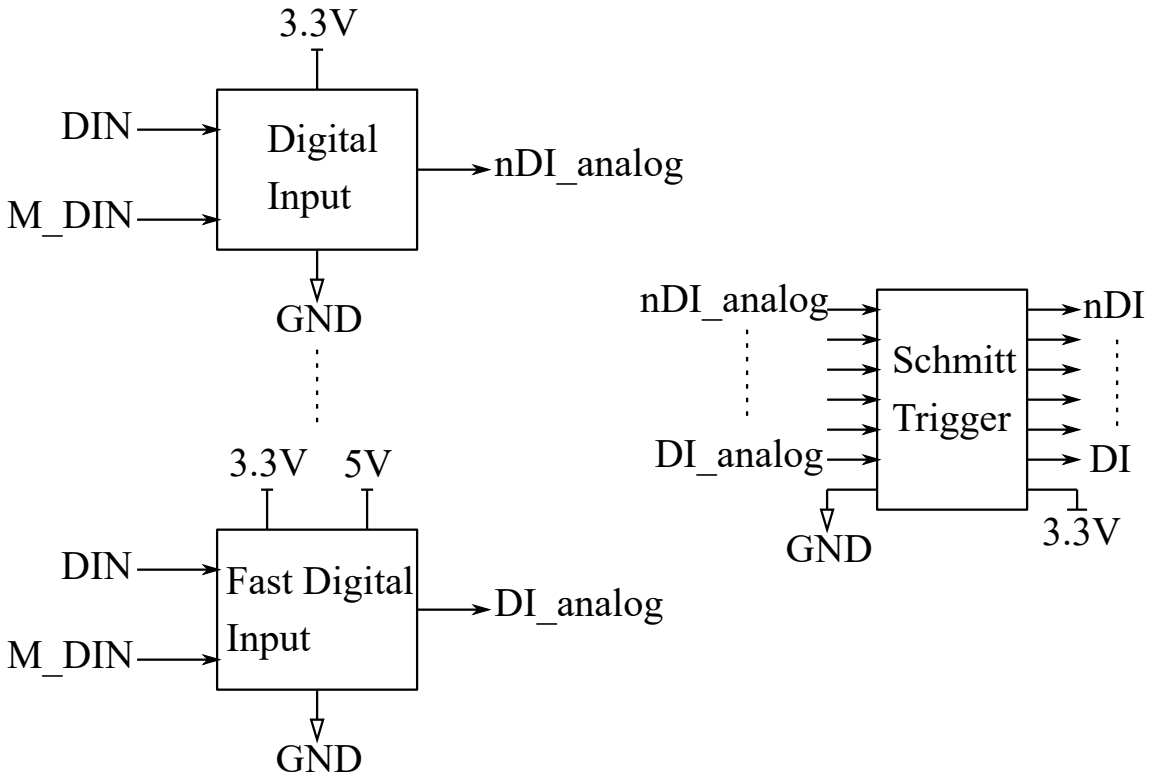


Figure 8-4: Final hierarchical design for the Digital Inputs.

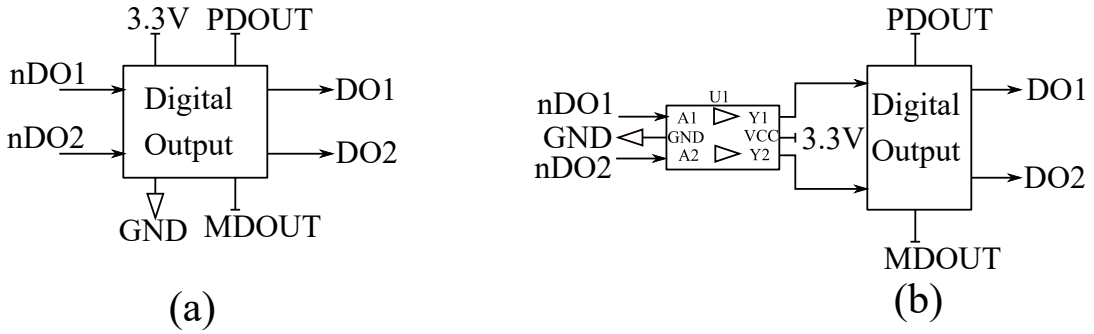


Figure 8-5: (a) Digital Output used for simulations. (b) Completely functional Digital Output.

This will be the whole hierarchy for the digital I/O. This process is identical for the digital I/O of the TB1350, but it cannot be copied from the TB0107 since there are some changes in the schematic.

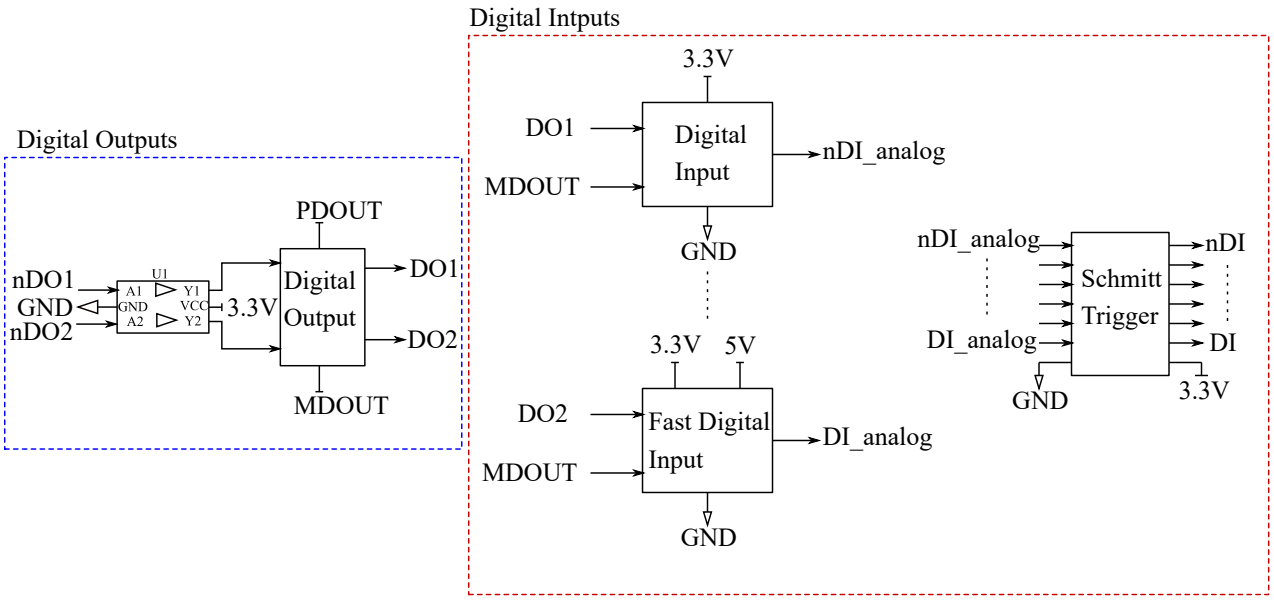


Figure 8-6: Final hierarchical design for the TB0107.

8.3 Encoder

The encoder was other of the units that have priority to be simulated. The schematic of the encoder is shown in Figure 8-7.

Heeding Figure 8-7., it can be seen that the encoder has the same schematic for measure A and measure B, thus the most reasonable procedure will be to reproduce only one schematic and to generate the rest of the modules from it by indicating if it is the part A or B of the encoder 0,1,2 and so on. However, as it has been seen above in relation to the digital inputs, this will generate a huge number of modules, then, it was decided to group the encoder as it can be seen in Figure 8-7., having as an output: A, nA, B, nB.

Again the difference between the simulation and the BOM has been established. The design is identical to the one made for the fast digital inputs. With the encoder all the hierarchical designs are made.

Right now it can be confirmed that these hierarchy structures are the final version, even if the components are not working as it is expected.

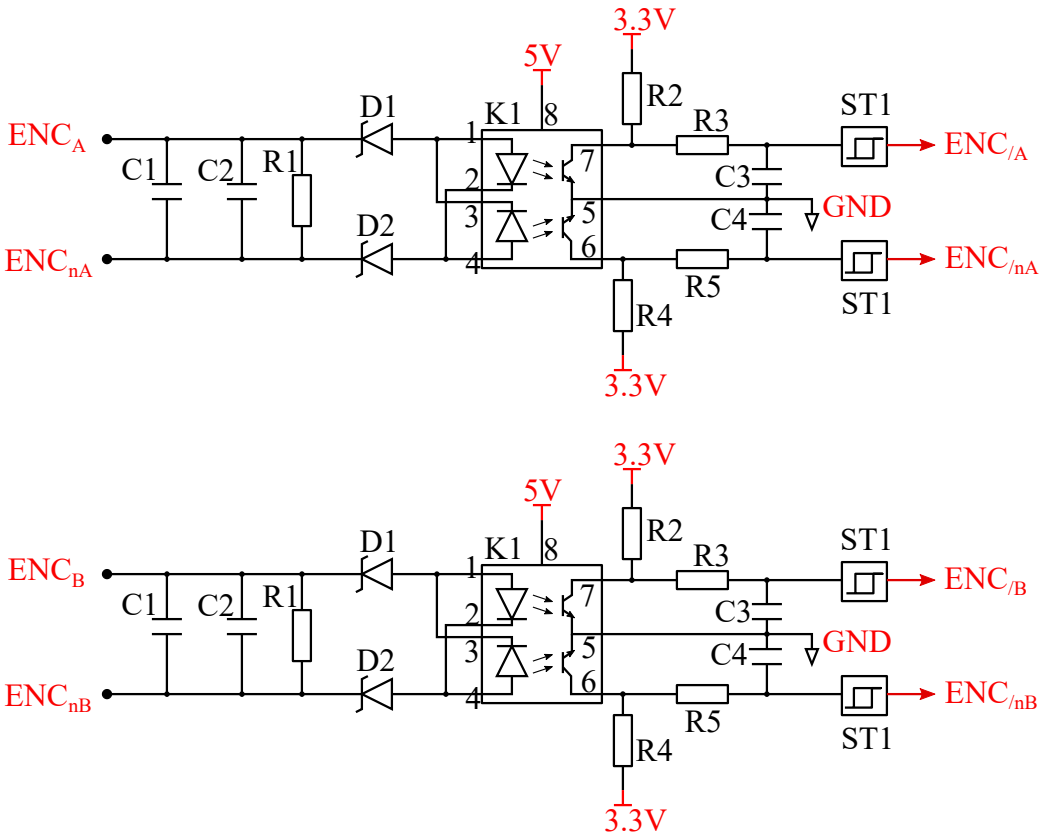


Figure 8-7: Schematic of the Encoder

Chapter 9

Verification methods

9.1 Introduction

This chapter will explain the different tests that the system will undergo, plus some considerations that should be taken into account when the system is simulated.

9.2 Transient analysis

This part is critical since the behaviour of the system is going to be tested here. There will be several steps, and not all of the simulations will be included in the memory, they will be included in the annexes. The simulations can be classified as the following subsections show.

9.2.1 Operation point

This simulation consists on introducing an input voltage which varies from 0 to 30V very slowly. This is done by using a big period of time and also the rising and falling time will be exaggerated.

The important part of this simulation consists on identifying the operation points of the circuit so that these results can be later compared to the real behaviour.

9.2.2 Variation of the operation points

In the simulation the components are fed by ideal DC voltage sources, but in the real case this is not done. The digital I/O are fed by a battery of 24V of rated value, however, this voltage is not constant and can decrease to 16.8V or increase up to 30V. Hence, the system should be tested under these conditions.

The same procedure is done with the encoder, although in this case this does make not sense since it is fed by a power supply. This is done because we want to show that, under a certain voltage, the encoder will not work.

9.2.3 Frequency analysis

In the frequency analysis, as its name indicates, the frequency of the input waveforms will vary. This analysis is quite interesting because it indicates at which point the model will stop working correctly.

9.2.4 Comparison between the real results and the simulation results.

Several tests will be performed but this one is critical since the results are compared with the signals achieved in the Electra. Several points have been measured and their data have been exported as a *csv* file. The same points have been measured in the simulation and again they have been exported as a *csv* file.

Once all the files needed have been obtained, they have been plotted with the help of the software Matlab and they have been compared. As it has been said above this procedure shows if the simulation has any problem and where it can be found.

This test is done by introducing several digital signals[1] to the Digital Outputs, these digital signals are processed and transformed into an analog signal which feeds the digital Inputs. The digital input is again transformed into a digital signal which is introduced in the FPGA. The points measured during the test are the inputs of

[1]These signals are generated by a computer with an specific software property of Ingeteam Power Technologies. The main goal is to simulate the control stage, i.e., the Field Programmable Gate Array (FPGA).

the Digital Outputs, the output voltages generated by the Digital Outputs which are the input voltages of the Digital Inputs. In the Digital Inputs the output voltage of the optocoupler is measured and compared with the voltage of the input buffer. This voltage is the same, but it has been filtered by a RC filter. And the last measurement is the output voltage of the Digital Inputs, which will be introduced in the FPGA.

This procedure cannot be applied to the encoder since there are not any tests to check its behaviour. Nevertheless, by analysing the circuit and comparing the theoretical waveforms with the ones obtained from the simulation, it is possible to see if there is a problem in a first approach.

9.3 Surge test

This test checks the robustness of the Transient Voltage Suppressor (TVS). Heeding Figure 8-1. it is possible to see at the beginning of the driver this type of devices for the digital inputs and in the output of the Solid State Relay in the digital outputs.

A surge test is a real test which consists on introducing a peak of voltage 1kV for differential pair operation and 2kV when phase to ground needs to be tested. To perform that test in a real environment, a specialized equipment is needed, which includes a manual with all the information of the components inside and a schematic. Then, it has been quite easy to implement it in the simulation. Figure 9-1. shows the schematic used to do the surge test.

There are several parts inside the figure, they represent the following.

1. **Surge**: It represents the peak voltage, this peak voltage has been modelled as the normative indicates. The surge must reach its maximum value at 1.2μs and later it should decrease to the 50% of the maximum value at 50μs. In this case only the differential behaviour is desired, then, the maximum voltage will be 1kV. Figure 9-2. shows the surge waveform used to do the simulations.

   It is necessary to test both kind of surges, positive and negative, in order to ensure a complete protection of the system.

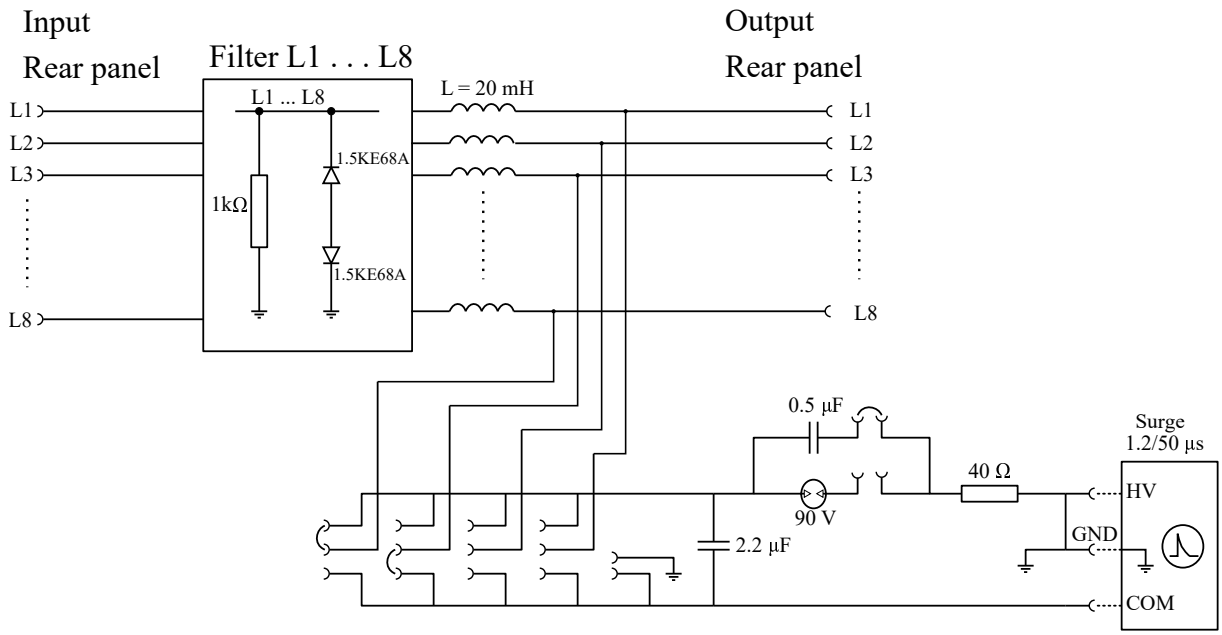


Figure 9-1: Surge Test schematic given by the manufacturer.

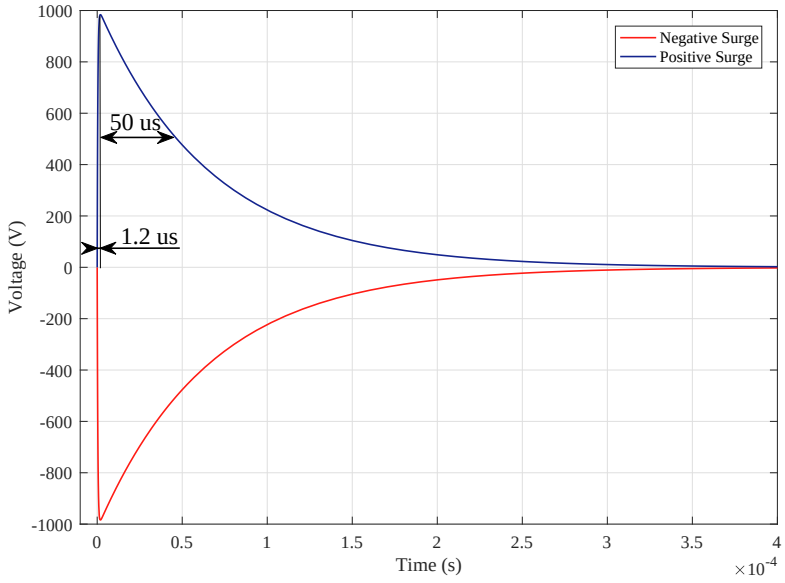


Figure 9-2: Voltage surge positive and negative used in the test.

2. **Connection between the filter and the surge**: This part of the circuit is used to set different configurations, because more than one test can be done with the same equipment.

3. **Filter from line 1 to 8**: This is the decoupling part, as its name indicates, it is used to decouple the power sources from the point in which the surge is produced. This will ensure that if the protection of the circuit is not well designed, the damage will not spread to the rest of the circuit.

This test will affect the digital I/O of the TB0107 and TB1350. The encoder does not have any protection at the entry, then it will not be simulated.

9.4 Advance Analysis

PSpice Advance Analysis (PSAA) is a powerful tool that allows the user to have a general vision of the system performance and improve it. Typically, this is done by showing graphically the state of the components for the selected analysis. PSAA has five powerful tools:

- Smoke Analysis.
- Sensitivity Analysis.
- Optimizer Tool.
- Monte Carlo.
- Parametric Plotter

Their execution process is common to all of them. This can be summarised in the flowchart shown in Figure 9-3.

One of the aims of this project consists on having a valid model to do the Smoke Analysis. However, Sensitivity Analysis and also Monte Carlo could be interesting in a near future, hence, the components have been designed taking this fact into account.

Previous to explaining the whole process and showing the results obtained from the simulations, a definition of the different tools labelled abroad is needed.

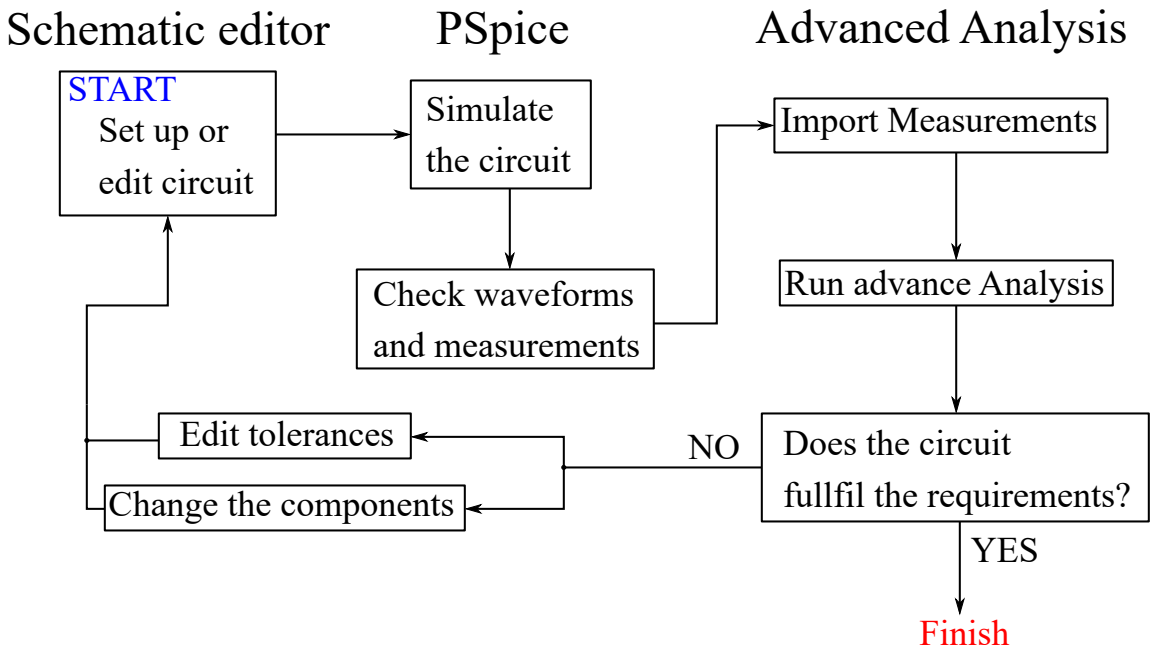


Figure 9-3: Flowchart to redesign a circuit using PSpice Advance Analysis [6].

9.4.1 Sensitivity Analysis

Sensitive Analysis identifies which are the components of the circuit that have critical parameters that affect the measurements goals defined.

This tool is a measure of how much a component could affect the performance of the system comparing it with the rest of them. It also allows to create the worst-case scenario by varying the tolerance of the components.

Typically this analysis is combined with the optimizer tool, which modifies the component to achieve a better performance of the system.

9.4.2 Monte Carlo

Monte Carlo Analysis is based on modifying the tolerances of the components to have a statistical circuit behaviour, it also can calculate yield which is very interesting for mass manufacturing predictions.

9.4.3 Smoke Analysis

As it has been said above one of the final aims of the project is to perform an Electrical Overstress (EOS) analysis to observe the behaviour of the circuit at different operation points. Smoke Analysis is used to detect component stress due to power dissipation, increase in junction temperature, secondary breakdowns or violations of voltage or current limits defined in the model of the components. This allows the user to have an idea of the performance of the circuit, to estimate the lifetime of the components and also to foresee possible failures in the future.

The Smoke Analysis must be executed after a transient simulation since it compares the values obtained from it with the limits imposed in the model. After that, it shows graphically the state of that component in relation to the limit to indicate if the component is working under the Safe Operating Area. It should be taken into account that some parameters depend on time, hence the time of simulation will be a critical point.

The Smoke Analysis uses the Maximum Operating Conditions (MOCs), supplied by manufacturers and the de-rating factors imposed by the user. An important restriction should be considered: not all the components can be included into this analysis. The components allowed to run a Smoke analysis are: Resistances, Capacitors, Inductor, BJT, MOSFET, SCR, Diode, Diode Bridge, Zeners, Dual MOS, JFET, MESFET, Optocouplers 4 pin, Switches, Operational Amplifiers, Varistors, LEDs and Linear Voltage Regulators.

De-rating Factors

De-rating is a design process that can make a significant contribution to reliability; it is defined as 'a policy of deliberately under-stressing components to provide increased reliability'[7].

Stress rating is defined as the ratio of applied stress to rated stress. Normally, the higher the stress, the higher the probability of failure; hence, the importance of this kind of analysis. However, having a low stress is also a problem, since at very low

values the failure of the components could also appear.

Most of the failures caused by stress are caused by a bad designing stage, this method tries to avoid this. By doing a previous simulation and then running a smoke analysis, a preview of the behaviour across time could be achieved.

Before, the stress of the components has been mentioned, but until this point it is a bit fuzzy. Electronic components have in general two levels of stress, the electrical stress and the thermal stress.

Electrical stress is produced by a current, a voltage or a power over their design limits, this increases the probability of having a failure due to breakdown. Thermal stress is produced mainly due to the power dissipation of the component. This power dissipation will depend on the component e.g. the resistors will only have one kind of losses which will be electrical, but semiconductors will have two kind of losses, one due to the dissipation of power and the other due to the switching (switching losses) and so on. Other parameter that affects the thermal stress is the placement in the PCB, because the heat dissipated by closest components will increase its own temperature. Furthermore, the routing (quantity of copper, size of the pad, clearance, the size and shape of the heat sink, age and so on) will also be an important factor.

All these problems can be avoided in the designing stage, that is because having a simulation is very important and will reduce the cost of a project. Something remarkable is that by reducing the electrical stress, the thermal stress will also be reduced, and by having a good layout most of the problems can be avoided. In addition, PSpice can run a simulation under different temperatures, hence, different operating conditions can be tested.

There are several options when a de-rating analysis is desired:

- Mathematical models containing a stress de-rating factor for calculating component failure rates.

- Graphs relating stress to percentage of maximum rating and a zone in which the component should be operated. These curves can be typically found in the data-sheet of the components.

- Graphs relating stress to percentage of maximum rating defining the different operating zones in which the component could be operated.
- Individual de-rating factors for each component related to a critical stress condition.

The last option mentioned above is the one that has been used. At a first moment the de-rating factors were developed as it is shown in [7]. Since these values were later substituted, the first way in which the de-rating factors were developed will not be explained, but it is considered recommended literature as a starting point. In Table 9.1. the de-rating factors for the different components are defined:

Table 9.1: De-rated Factors of the components.

Element	Field	De-rated Factor
Ceramic Capacitor	Voltage	80%
	Current	75%
Tantalum Capacitor	Voltage	75%
	Current	75%
Electrolitic Capacitor	Voltage	75%
	Current	75%
Schottky Diode	Forward Current	75%
	Reverse Voltage	75%
	Dissipated Power	75%
	Junction Temperature	110 ^oC
Zener Diode	Dissipated Power or current I_{zm}	65%
	Junction Temperature	110 ^oC
Diodes and LEDs	Forward Current	50%
	Reverse Voltage	75%
	Dissipated Power	50%
Inductors and Transformers	Voltage	50%
Integrated circuits: linear	Supply Voltage	90%
	Input Voltage	70% OP 100% Comparators 90% Regulators
	Output Current	100%
	Transients	80%
	Juction Temperature	110 ^oC
Resistors	Voltage	80%
	Dissipated Power	50 % up to 125 ^oC Decreasing to 0 % at 150 ^oC
Bipolar Transistors	Collector-Emitter Voltage V_{CE}	75%
	Collector-BaseVoltage V_{CB}	75%
	Emitter-Base Voltage V_{EB}	75%
	Collector Current	75%
	Base Current	75%
	Dissipated Power	65%
	Junction Temperature	110 ^oC
FFT transistors	Drain to Source Voltage V_{DS}	80%
	Gate to Source Voltage V_{GS}	75%
	Drain Current	75%
	Dissipated Power	65%
	Junction Temperature	110 ^oC
Optocouplers	Forward Current	50%
	Reverse Voltage	75%
	Collector Current	80%
	Collector-Emitter Voltage V_{CE}	75%
	Junction Temperature	110 ^oC

Chapter 10

Analytical results

10.1 Introduction

In this chapter the results obtained from the simulation will be discussed. The simulations have been divided as follows:

- Digital Inputs for the TB0107 and TB1350.
- Fast Digital Inputs for the TB0107 and TB1350.
- Digital Outputs for the TB0107 and TB1350.
- Comparison between the real results and the simulation.
- Encoder.

Inside every section, the analyses that have been done are those ones mentioned in Chapter 9 *Verification methods*. Since all the procedures have been explained above, this section will focus only on the results.

10.2 TB0107 Digital Inputs

10.2.1 Operation Point

Figure 10-1. shows the operation of the TB0107 Digital Input (nDI is the name given to these inputs by the Company).

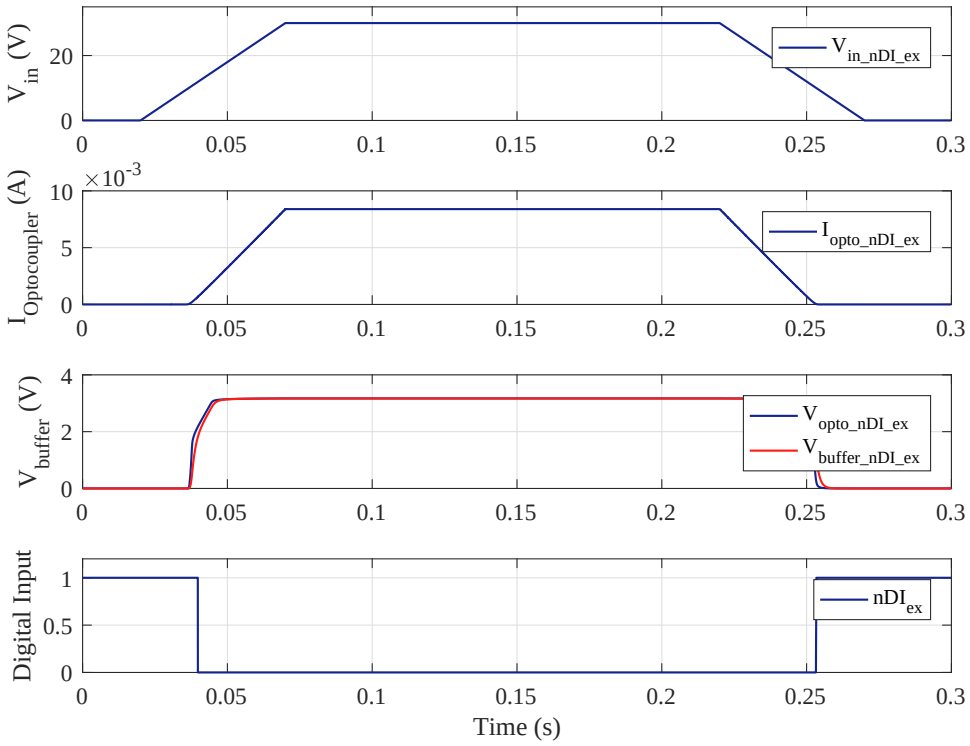


Figure 10-1: Operation point of the nDI of TB0107: (a) Input voltage. (b) Current flowing through the optocoupler's LED. (c) Voltage at the ouput of the ouptocoupler and the voltage resultant after applying a RC filter. (d) Digital output nDI.

In a first approach the behaviour of the nDI seems to be correct. In this case, since the company does not provide any measurements of the operation point, only the behaviour and certain measurements are relevant.

If the circuit is analysed the following behaviour will be achieved. Firstly, the input voltage is introduced, however, the system is not conducting any current through the optocoupler since the top and bottom zeners must reach a differential voltage of 10V

to conduct. Once the voltage is higher than 10V, the optocoupler must start to increase its current. At the same time a voltage must appear in the output. The output voltage of the optocoupler and the current flowing through the optocoupler LED are directly related.

Secondly, the output voltage must be between 0V and 3.3V which are the values needed by the Schmitt trigger. Since this output voltage has been modelled as a real component, the effect of the capacitance that appears in the IGBT between the Collector and the Emitter can be noticed. This effect occurs in the falling due to the discharge of the capacitor and in the rising due to the charge of the capacitor. This signal is smoothed by a RC filter; the resultant voltage, after being filtered, will be labelled as input buffer voltage.

Thirdly, the input buffer voltage is introduced into the Schmitt trigger in order to achieve a digital output signal. The Schmitt trigger is an inverting device, then, the output should be the inverse of the input.

In Figure 10-1b. the current through the optocoupler starts to flow when the input voltage is around 10V as it is expected, this one increases until the input voltage reaches the maximum value and it becomes zero when the input voltage is lower than 10V.

In Figure 10-1c. it is possible to see when the output voltage of the optocoupler is activated at the same time that the current is flowing through the LED of the optocoupler. The charge and discharge of the voltage in the rising and the falling because of the capacitive effect in the IGBT can be clearly seen. Furthermore, the voltage goes from 0 to 3.3V as it is expected.

Finally, the inverse digital signal can be achieved. This is represented in Figure 10-1d.

10.2.2 Voltage Variation

Figure A-1. of appendix A shows the behaviour of the nDI when the input voltage varies. It can be seen how the circuit exhibits the same behaviour. It makes sense that there is a variation in the current through the LED of the optocoupler since the

input voltage is different in the three cases. Nevertheless, it is enough to activate the IGBT. Since the current does not affect the output due to the isolation, the output is practically the same, only there is a little variation because of the activation of the LED.

10.2.3 Frequency Analysis

In Figure A-2. of appendix A it is possible to see the behaviour of the nDI at high different frequencies. Table 10.1 summarizes the delay between the input and the output.

Table 10.1: Phase shift of nDI TB0107 at different frequencies.

nDI TB0107	
Frequency (Hz)	**Phase Shift (us)**
50	1260
200	1156
500	932
2.5k	Uncorrect behaviour

It should be said that the output signal labelled as nDI is a digital signal, that means this signal can only achieve values of 0 or 1. However, to see clearly the effect of the frequency, as it has been said, it is necessary to compare the digital input with the input voltage which goes from 0V to 24V, then it has been multiplied by a gain in order to observe easily the behaviour of both signals.

In Figure A-2a. and A-2b. two different frequencies are tested in order to prove that the delay is independent from the frequency. This is confirmed in Table 10.1.

Figure A-2c. and A-2d. shows the behaviour of the system at the boundary condition and over the boundary respectively. In the first one it can be checked that the delay remains constant. However, when the frequency increases, it can be seen that the Schmitt trigger is not fast enough to track the input signal and as a consequence its behaviour is not the one desired.

10.2.4 Surge Test

Having a protection at the input which limits the maximum voltage of the circuit is crucial. Only in this case two kinds of test will be done, in order to prove the importance of the TVS protection. The first surge test has been done removing the TVS, then the effect of a surge in the system could be seen. After that, the TVS has been included again and the surge test is repeated and both systems are compared.

Without TVS

Figure A-3. of the appendix shows the surge test without any protection. As it can be seen in Figure A-3a. the voltage reaches the maximum value. Furthermore a smoke analysis has been performed in order to see the effect in the components.

The smoke analysis reveals that most of the components have exceeded its maximum values by far. In terms of power, several components are over the maximum value in a 300% and in terms of temperature they have reached values of 38000 ^{o}C.

With TVS

Figure A-4. of the appendix shows the surge test with all the protections included.

As it can be seen the voltage peak has been reduced significantly, the maximum value achieved is 50V, which is the limit of the TVS. It should be said that the system is not fully isolated since there is a problem related to the grounds and the software. It does not allow to have several grounds, hence all the system has been referred to the same ground. Due to that reason there are oscillations at the input voltage. This, in a real case in which the grounds are well designed, should not occur. The TVS will reach the value of $\pm$50V in case of having a positive or negative surge, and later it will decrease to zero.

A smoke analysis again has been done and it is possible to observe that most of the components have not reached their maximum values, what is more, the nDI is working in steady-state. Only a small number of resistances have overpassed their limits in temperature, but it is not the average value it is the peak value. This is

because at the first moment, some resistances have a peak of power due to the surge. However, the mean value and the average are working under the rated value.

10.2.5 Smoke Analysis

Smoke Analysis, as it has been said in Chapter 9 *Verification methods*, is a very useful tool to identify the critical components of the circuit. Instead of measuring all the characteristics, this analysis shows the critical aspects of the components and it shows graphically their state. As it has been explained above the EOS is included in this analysis through the De-rated factors. The usefulness of a simulation and this analysis will be discussed, since two versions of this part of the circuit have been done. The first one is the first version designed by Ingeteam Power Technologies which exhibits high temperatures and power dissipation, and the second one is the current version. There is an error with the TVS because its analysis is not allowed, it has been treated as a Zener diode, but its reverse current in this case is the main current, as a consequence it is over the limits all the time. Hence, it should not be considered.

It should be said that the smoke analysis will only be addressed for the nDI TB0107, since it is the most interesting case.

10.2.6 nDI TB0107 first design

PDF of Appendix A.5.1 shows the results obtained of the Smoke Analysis applying the de-rated factors for the first design of the nDI TB0107.

As it can be appreciated, there are several elements over the limit, there are some resistors dissipating a power of 160mW each one and their temperature is more or less 155^{o}C. These measurements coincide with the problems detected years ago by Ingeteam. Heeding the last column, it is possible to see the utility of the smoke analysis, it provides information graphically of the state of the circuit instead measuring element by element. The TVS measurements have not been neglected since it is useful to see what the currents, the voltages and the power dissipation of that element are.

10.2.7 nDI TB0107 current design

PDF of Appendix A.5.2.1 shows the results obtained of the Smoke Analysis without applying the de-rated factors for the current version.

In this case the de-rated factors have not been applied and at this point the measurements are compared with the rated values which cannot be overpassed. It can be clearly seen that there is not any component over the limit even when the de-rated factors have not been applied. Remembering that the de-rated factors will restrict the conditions of the circuit, some components can be compromised. But the most important fact is the utility of a simulation in which it has been seen how a simple simulation can show the problems that could appear inside a circuit. There are several tables that have been used to compare the behaviour of the nDI TB0107 (both the current PCB and the original with problems) and it should be said that it matches perfectly. This information is property of Ingeteam Power Technologies and cannot be shown in this version.

PDF of Appendix A.5.2.2 shows the results obtained of the Smoke Analysis applying the de-rated factors for the current version. As it can be seen even if the limits have been reduced, the circuit works under the limits.

10.3 TB0107 Fast Digital Inputs

10.3.1 Operation Point

The Fast Digital Inputs are labelled as DI, their behaviour is the same as the described for the nDI, but there is a difference and it is the optocoupler. This optocoupler has its input negated; this means that the voltage will be opposite to the current unlike the nDI. Figure 10-2. shows the operation point for the DI.

Heeding Figure 10-2. it can be seen that the operation of the circuit is the correct one. The threshold voltage of the LED current is around 10V, the maximum output voltage is 3.3V and the output is inverse in relation to the input buffer voltage.

One aspect which should be noticed is the capacitive effect which in this case does

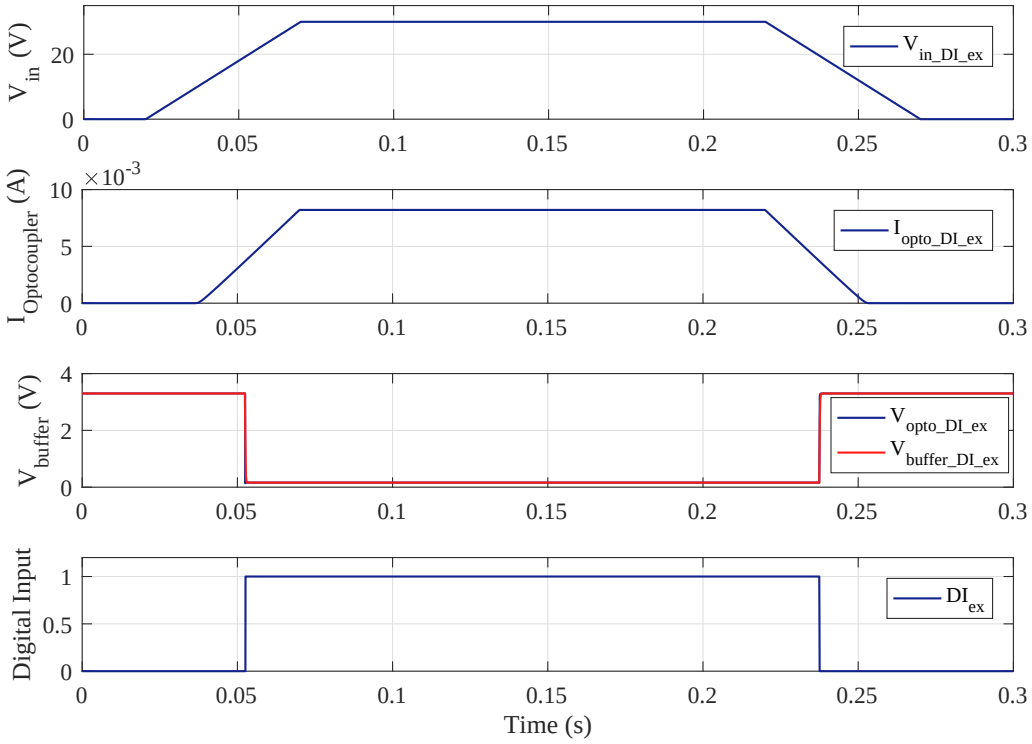


Figure 10-2: Operation point of the DI of TB0107: (a) Input voltage. (b) Current flowing through the optocoupler's LED. (c) Voltage at the ouput of the ouptocoupler and the voltage resultant after applying a RC filter. (d) Digital output DI.

not appear. This is because the optocoupler used is a fast optocoupler. Hence, the charge and the discharge of the capacitive effect is very fast and because of that it seems that this effect does not appear. Nevertheless, if a zoom is done at on/off this effect can be appreciated, but as it has been done, it can be neglected since it is charged and discharged in 450μs.

10.3.2 Voltage Variation

Figure B-1. of appendix B shows what happens when the input voltage varies. As it can be seen, unlike the nDI, this digital input has a problem with the minimum voltage of 16.8V. This is because the current through the LED is not enough to activate the receptor and as a consequence the IGBT does not deactivate, it should

be remembered that the output voltage is inverted.

10.3.3 Frequency Analysis

Figure B-2. of appendix B shows the behaviour of the system at different frequencies. Table 10.2. summarizes the results obtained.

Table 10.2: Phase shift of DI TB0107 at different frequencies.

DI TB0107	
Frequency (Hz)	**Phase Shift (us)**
50	80
250	83
4083	55,5
6000	Uncorrect behaviour

It must be noticed that this system is faster than the nDI, as a consequence this Digital Inputs can work at high frequencies as it can be checked by comparing Tables 10.1. and 10.2.

10.3.4 Surge Test

Figure B-3. of appendix B shows the surge test for DI. As it can be seen it is possible to see that the system is protected against over-voltages. Nevertheless, the operation is varying even when this is not supposed to happen. As it has been commented above, this is produced due to the isolation which is not well designed.

The smoke analysis reveals that the system is not being affected in a high manner by the surge. Again there are a few resistances affected but there are not several damages in the circuit.

10.3.5 Smoke Analysis

PDF of Appendix B.4 shows the results obtained of the Smoke Analysis applying the de-rated factors for the DI TB0107.

Again the same problem related with the TVS appears, but as it has been said, it should be neglected. It can be seen that the circuit is working as expected.

10.4 TB0107 Digital Outputs

In this section the results of the Digital Outputs also labelled as DO will be discussed. It should be said that the solid state relay model did not work as expected. As a solution, an optocoupler with similar characteristics is used. In this chapter no problems will result with this change. However, the effect of this change will be noticed when a comparison with the real behaviour of the TB0107 is made.

10.4.1 Operation Point

The behaviour of the DO is the following: firstly the digital input is transformed from the digital domain to the analog domain, this is done using a non-inverting device. This voltage is applied directly to the optocoupler's input. When the voltage is high, the current through the led is zero, and when the voltage is zero the current flows through the LED.

The optocoupler's output voltage circuit is fed by a battery with a constant voltage of 24V. Nevertheless, as it has been seen above, the voltage can vary between 16.8V and 30V, this output voltage will be the input for both Digital Inputs, the nDI and DI. The switching of the optocoupler is the one which indicates the switching of the output voltage. Figure 10-3. shows the behaviour for 24V of power supply.

Heeding Figure 10-3. the behaviour mentioned above can be seen, as well as how the output voltage varies between 0V and 24V. Furthermore, a complete simulation can be done if this output voltage is introduced as an input voltage for nDI and DI. This will be done below.

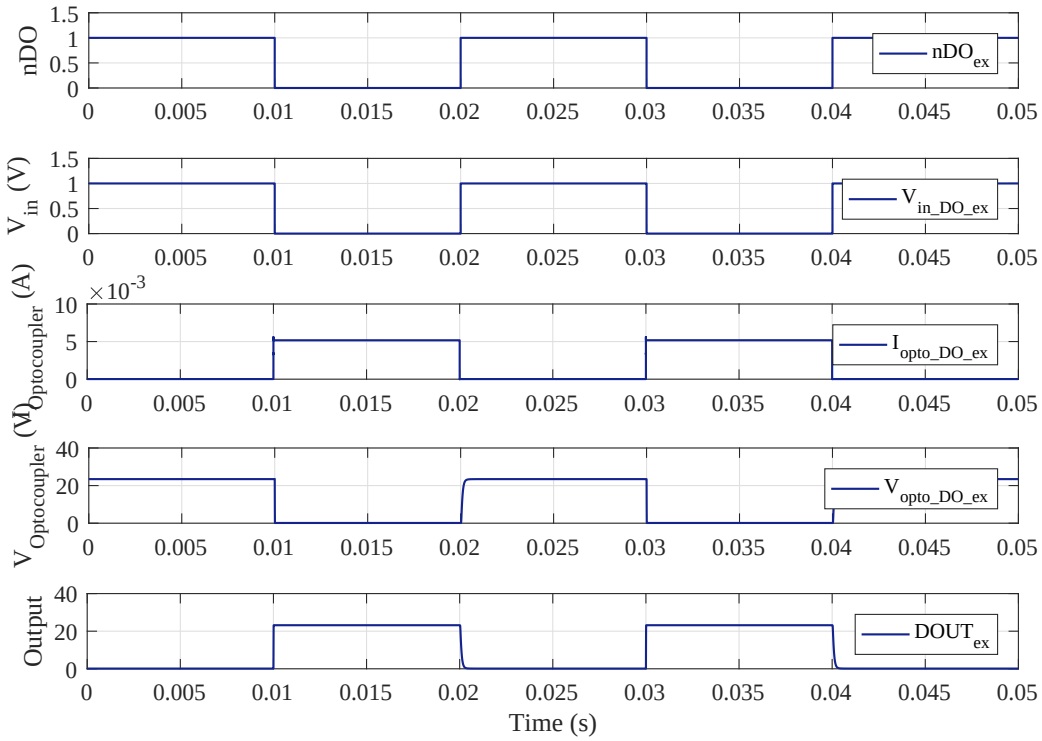


Figure 10-3: Operation point of the DO of TB0107: (a) Digital Input signal nDO. (b) Input voltage. (c) Current flowing through the optocoupler's LED. (d) Voltage at the ouput of the ouptocoupler. (e) Digital output DOUT.

10.4.2 Voltage Variation

As Figure C-1. of appendix C shows, by varying the power supply voltage, the output will vary.

10.4.3 Frequency Analysis

Figure C-2. of appendix C shows the behaviour of the system at different frequencies. It must be remarked again that there is an element which is not modelled. As a consequence, the results obtained have not the desired accuracy. Table 10.3. shows the delay existing between both signals.

This figure intends to show the range of frequencies in which the system could

Table 10.3: Phase shift of DO TB0107 at different frequencies.

DO TB0107	
Frequency (Hz)	**Phase Shift (us)**
10	3
150	27
1500	30
50k	Uncorrect behaviour

work.

10.4.4 Surge Test

To test the digital outputs two configurations must be tried. The first one in which the surge is introduced between *PDOUT* and *MDOUT* and the second one is introduced between the output *DO* and *MDOUT*. They are labelled as 1^{st} Case and 2^{nd} Case respectively.

1^{st} Case

Figure 10-4. shows the effect of the surge.

The digital Input has been introduced as a constant value in order to see the effect of the surge at the output. This output is under suspicion of not being well protected. With this test it has been confirmed, since the output voltage reaches values out of the limit. However, this happens upstream to the surge application point. There are not any problems, the optocoupler, the Digital to Analog device and the FPGA are protected against surges.

2^{nd} Case

Figure 10-5. shows the results of applying a surge between the output *DO* and *MDOUT*.

It is possible to observe that the output again is not protected. However, this problem is produced when there is a voltage in the optocoupler, the surge magnifies

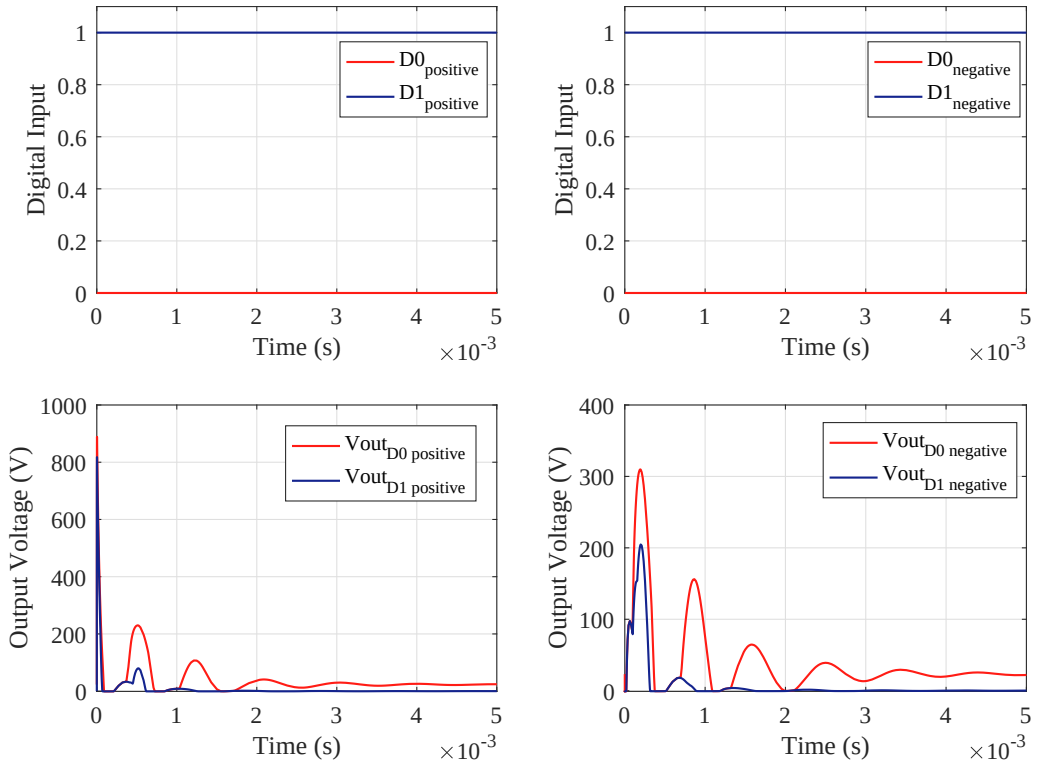


Figure 10-4: Surge Test for the DI TB0107 introducing the surge between *Pdout* and *Mdout*: (a) Digital input nDO for a positive surge. (b) Voltage at the PCC with a positive surge. (c) Digital input nDO for a negative surge. (d) Voltage at the PCC with a negative surge.

this output voltage. It can be observed that there are not any variations when the voltage is zero. It should be remembered that in other cases even when the output voltage is zero the system is affected.

10.4.5 Smoke Analysis

PDF of Appendix C.3 shows the results obtained of the Smoke Analysis applying the de-rated factors for the DO TB0107.

Again the same problem related with the TVS appears, but as it has been said, it should be neglected. In this case more measurements appear since there are two TVS instead of one. Also there is an optocoupler instead of a Solid State Relay, that is

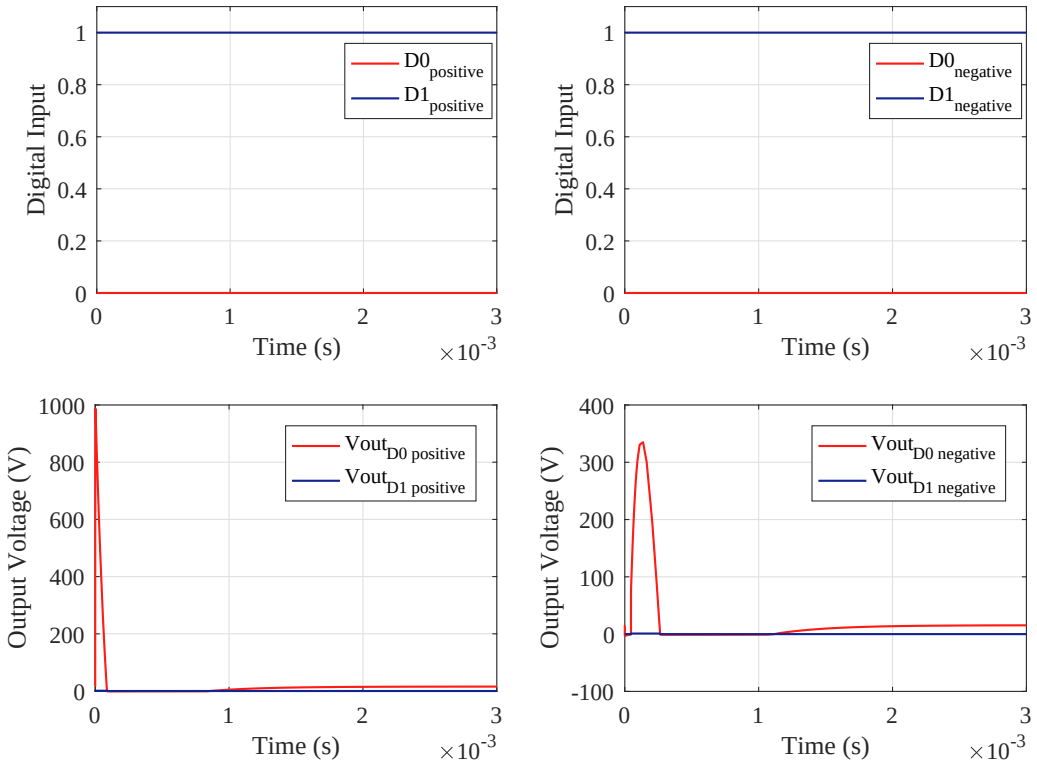


Figure 10-5: Surge Test for the DI TB0107 introducing the surge between *DOUT* and *Mdout*: (a) Digital input nDO for a positive surge. (b) Voltage at the PCC with a positive surge. (c) Digital input nDO for a negative surge. (d) Voltage at the PCC with a negative surge.

the principal reason to achieve a high current between the collector and the emitter thereof. It can be seen that the circuit is working as expected.

10.5 TB0107 Real case vs Simulation

As it has been said in Chapter 9. *Verification methods* this analysis is the most important since the real behaviour and the simulation results are faced against each other. The results of the scopes combine the full operation of the TB0107 mentioned above. Two comparisons are going to be made. The first one facing only the simulation results and the real simulations. The second one is more complex and a special voltage source is needed to do the simulation.

OrCAD allows to introduce external waveforms, then, the input voltage for the DO has been extracted from the scopes and it has been introduced in the simulation. Both DI and nDI have been analysed.

10.5.1 TB0107 Digital Inputs

PSpice simulation only

Figure 10-6. shows the PSpice simulation and the real one.

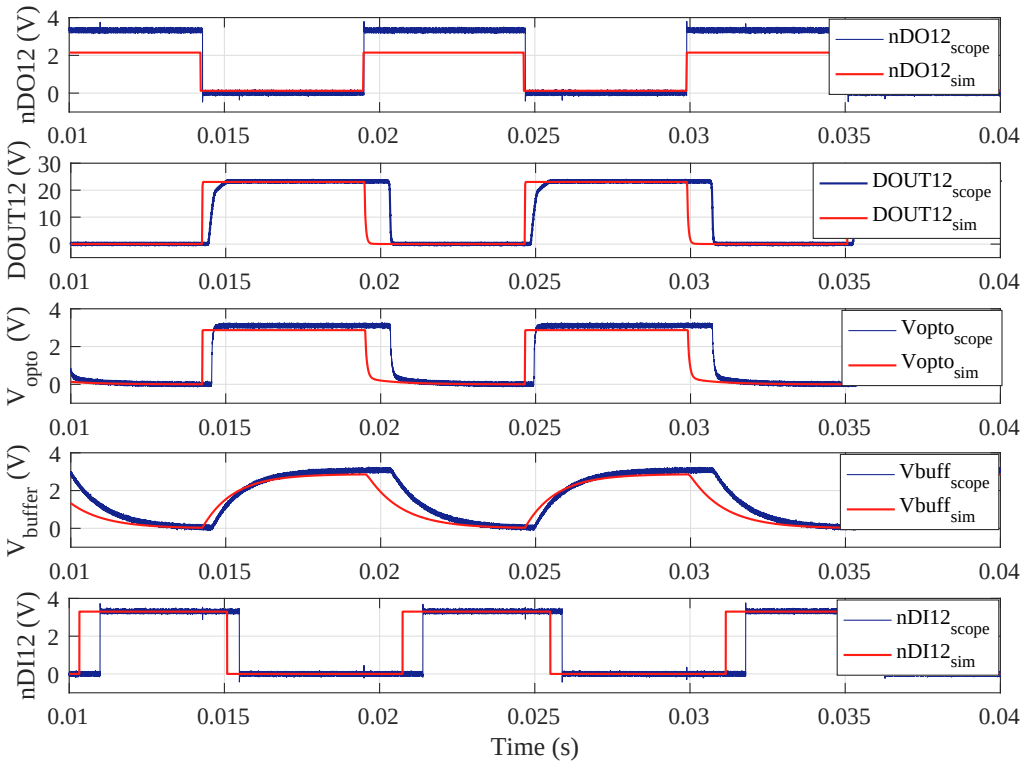


Figure 10-6: Simulation results of the nDI TB0107 compared with the real behaviour thereof: (a) Digital Input signal nDO converted to an analog signal. (b) Digital output DOUT. (c) Voltage at the ouput of the ouptocoupler of the digital input circuit nDI. (d) Voltage of the optocoupler filtered by an RC filter. (e) Digital output nDI.

Heeding Figure 10-6. it is possible that the results obtained are similar to the real behaviour. However, they are not exact because of the solid state relay. This occurs

because the optocoupler used instead of the solid state relays is faster than it should be. Since it occurs at the beginning, this error is hauled to the end of the simulation.

Paying attention to the figures, the waveforms are identical but they cannot be compared because of that error. But, since the plots have been done in Matlab, the results have been modified in order to avoid that mistake. Hence, by shifting the simulation results it is possible to make the rising coincide and also by doing the same the falling of the signals can be equalized.

PSpice simulation with real input voltage

In this case the input voltage is the one provided by the scopes. Figure 10-7. shows the results.

Equal to the previous case, the waveforms do not coincide due to the Solid State Relay. However, the maximum values and also the shapes of the waveforms are identical to the real simulation. Hence, the model can be assumed to be valid.

10.5.2 TB0107 Fast Digital Inputs

This section cannot be tested, because an error in the measurements has been detected. As a consequence this section cannot be tested. However, this measurement will be the same than the analogue of the TB1350, which has been achieved.

Once all the analyses for the TB0107 have been done, it does not make sense to perform some of them in the TB1350, because they are practically identical, the results obtained will be the same. Hence most of them are included in the appendix but they are not going to be discussed since, as it can be observed, they are identical. Then, it does not make sense to repeat the same explanation again. The only case which is interesting to analyse is the surge test for the Digital Outputs since the circuit at the output of the Solid State Relay changes and also the real behaviour.

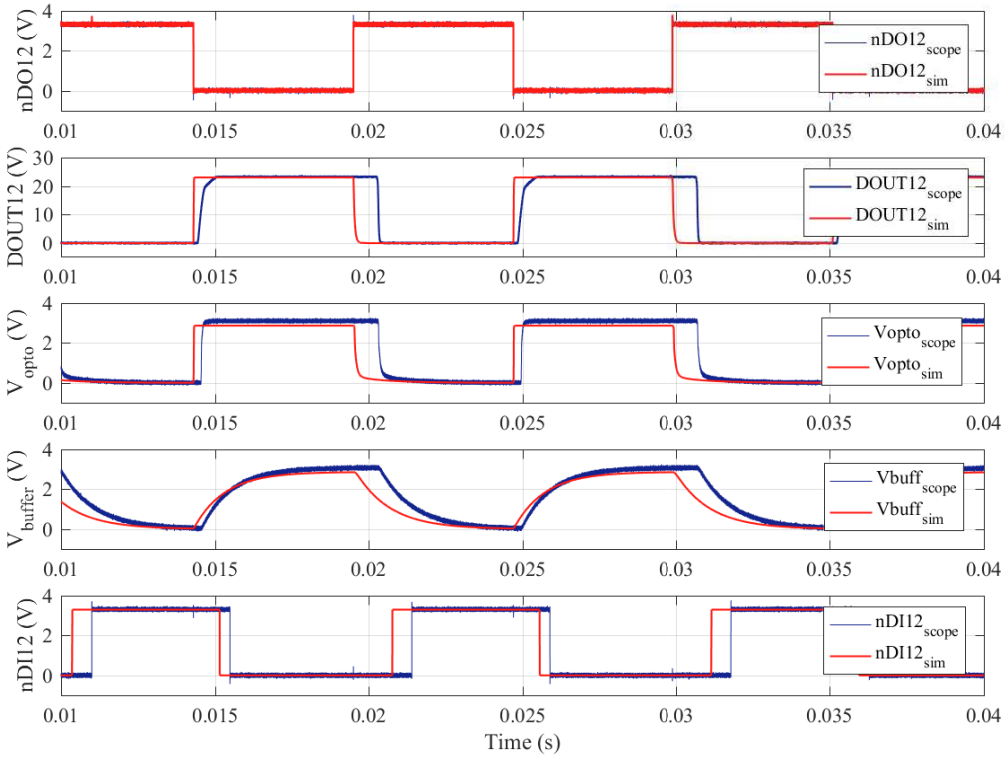


Figure 10-7: Simulation results of the nDI TB0107 with a real input signal compared with the real behaviour thereof: (a) Digital Input signal nDO converted to an analog signal. (b) Digital output DOUT. (c) Voltage at the ouput of the ouptocoupler of the digital input circuit nDI. (d) Voltage of the optocoupler filtered by an RC filter. (e) Digital output nDI.

10.6 TB1350 Digital Inputs

Since nDI and DI of TB0107 and TB1350 the surge test has not been done for this sections. Nevertheless, the DO are different, then, the surge test is very interesting to see the difference between both configurations.

10.6.1 Operation Point

Figure 10-8. shows the operation point of the nDI TB1350.

As it can be seen the results are identical to the ones shown in Figure 10-1.

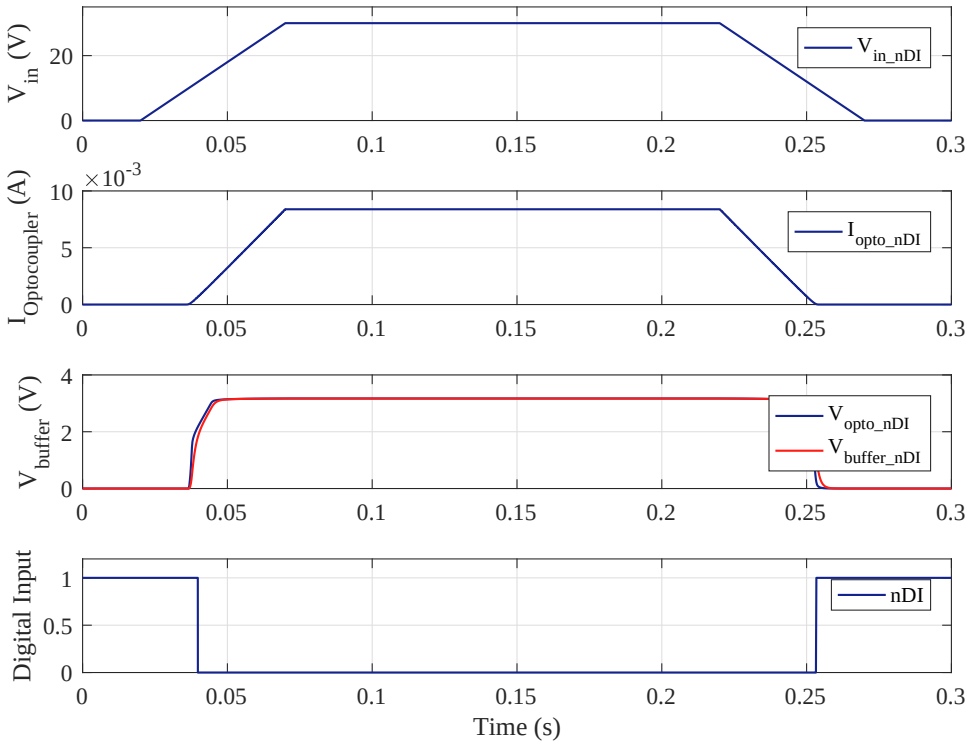


Figure 10-8: Operation point of the nDI of TB1350: (a) Input voltage. (b) Current flowing through the optocoupler's LED. (c) Voltage at the ouput of the ouptocoupler and the voltage resultant after applying a RC filter. (d) Digital output nDI.

10.6.2 Voltage Variation

See Figure D-1. of appendix D.

10.6.3 Frequency Analysis

See Figure D-2. of appendix D. Table 10.4 summarises the phase shift between both signals.

As it can be seen the results are similar to the ones obtained in Table 10.2 since both circuits have practically the same configuration.

Table 10.4: Phase shift of nDI TB1350 at different frequencies.

nDI TB1350	
Frequency (Hz)	**Phase Shift (us)**
50	1250
200	1169
500	781
2.5k	Uncorrect behaviour

10.6.4 Surge Test

See Figure D-3. of appendix D. The results are again similar to the ones achieved for nDI TB0107.

10.7 TB1350 Fast Digital Inputs

10.7.1 Operation Point

Figure 10-9. shows the operation point of the DI TB1350.

As it can be seen the results are identical to the ones shown in Figure 10-2.

10.7.2 Voltage Variation

See Figure E-1. of appendix E.

10.7.3 Frequency Analysis

See Figure E-2. of appendix E. Table 10.5 summarises the phase shift between both signals.

10.8 TB1350 Digital Outputs

10.8.1 Operation Point

Figure 10-10. shows the operation point for the digital outputs of the TB1350.

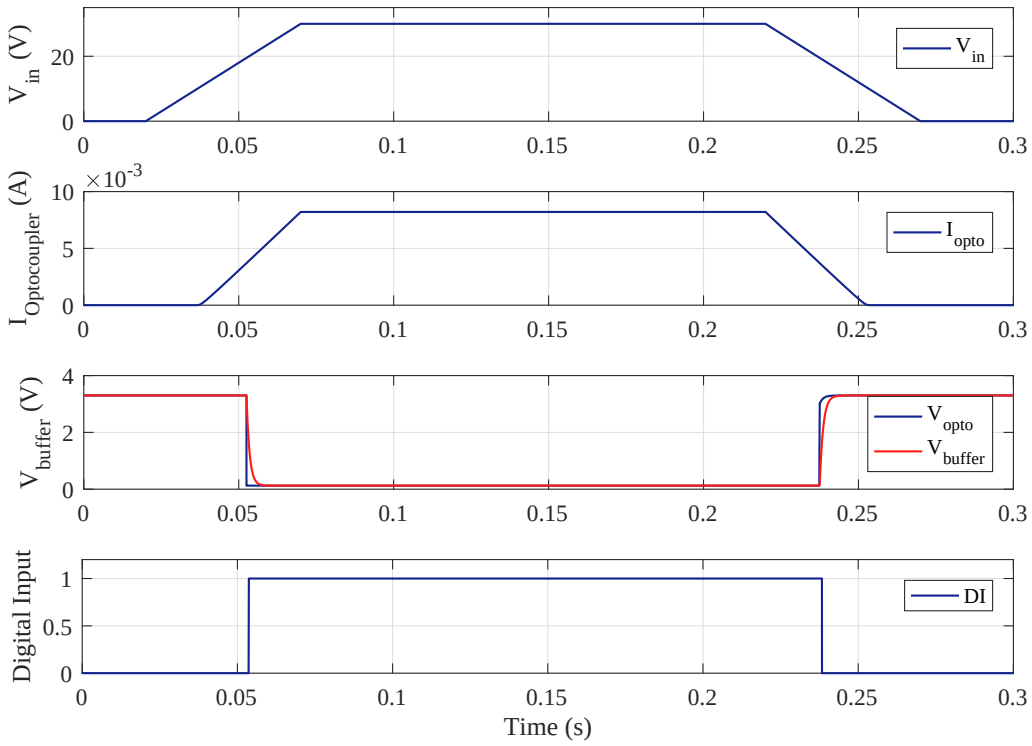


Figure 10-9: Operation point of the DI of TB1350: (a) Input voltage. (b) Current flowing through the optocoupler's LED. (c) Voltage at the ouput of the ouptocoupler and the voltage resultant after applying a RC filter. (d) Digital output DI.

Table 10.5: Phase shift of DI TB1350 at different frequencies.

DI TB1350	
Frequency (Hz)	**Phase Shift (us)**
50	80
250	84
4000	55,5
50k	Uncorrect behaviour

In a first approach, the behaviour of the circuit is similar. But the important part is not the transient behaviour, the differences will be reflected in the surge analysis.

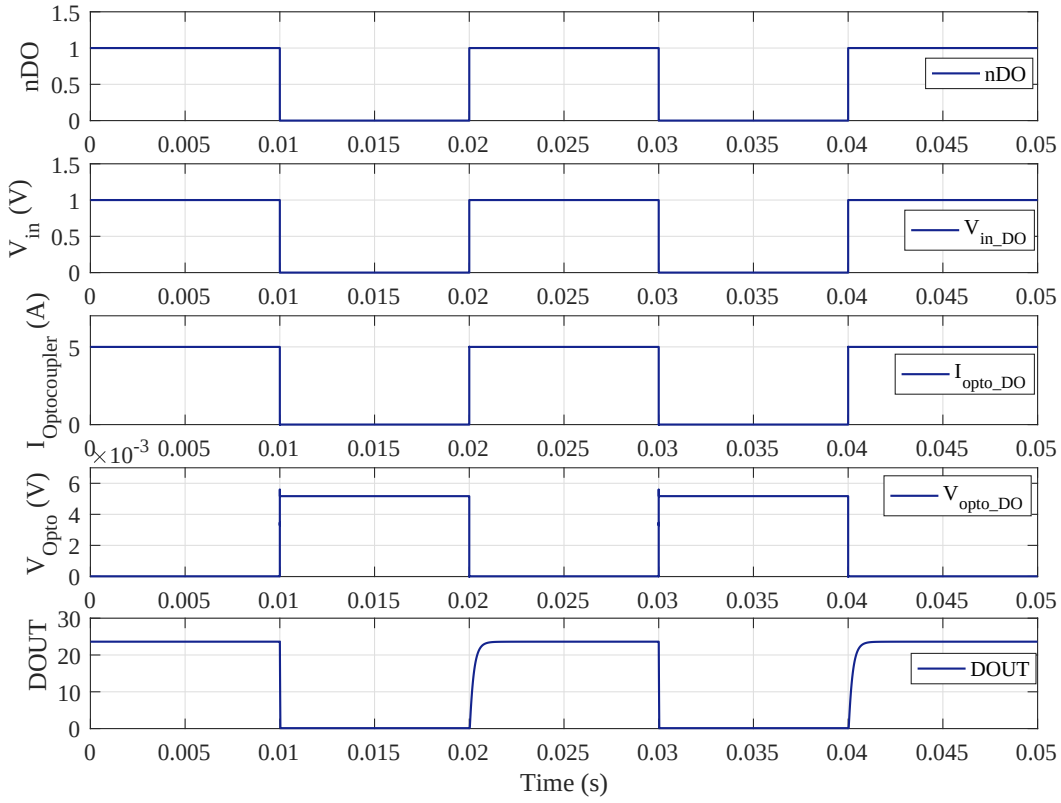


Figure 10-10: Operation point of the DO of TB1350: (a) Digital Input signal nDO. (b) Input voltage. (c) Current flowing through the optocoupler's LED. (d) Voltage at the ouput of the ouptocoupler. (e) Digital output DOUT.

10.8.2 Frequency Analysis

See Figure F-1. of appendix F. Table 10.6 summarises the phase shift between both signals.

Table 10.6: Phase shift of DO TB1350 at different frequencies.

DO TB1350	
Frequency (Hz)	**Phase Shift (us)**
50	30
500	30
1000	30
50k	Uncorrect behaviour

10.8.3 Surge Test

Again there are two cases to test.

1^{st} Case

Figure 10-11. shows the surge test for the first configuration.

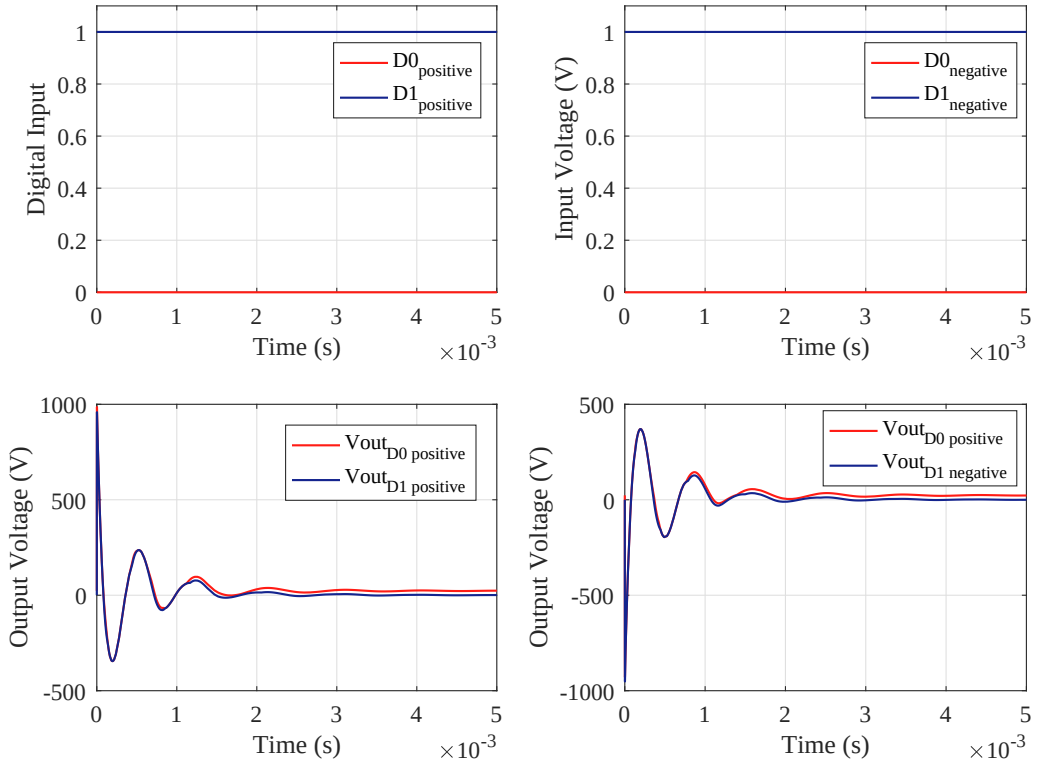


Figure 10-11: Surge Test for the DI TB0107 introducing the surge between *Pdout* and *Mdout*: (a) Digital input nDO for a positive surge. (b) Voltage at the PCC with a positive surge. (c) Digital input nDO for a negative surge. (d) Voltage at the PCC with a negative surge.

Again this configuration does not ensure the protection of the output. However, the input is protected against surges which is the most important part.

2^{nd} Case

Figure 10-12. shows the results for the second configuration.

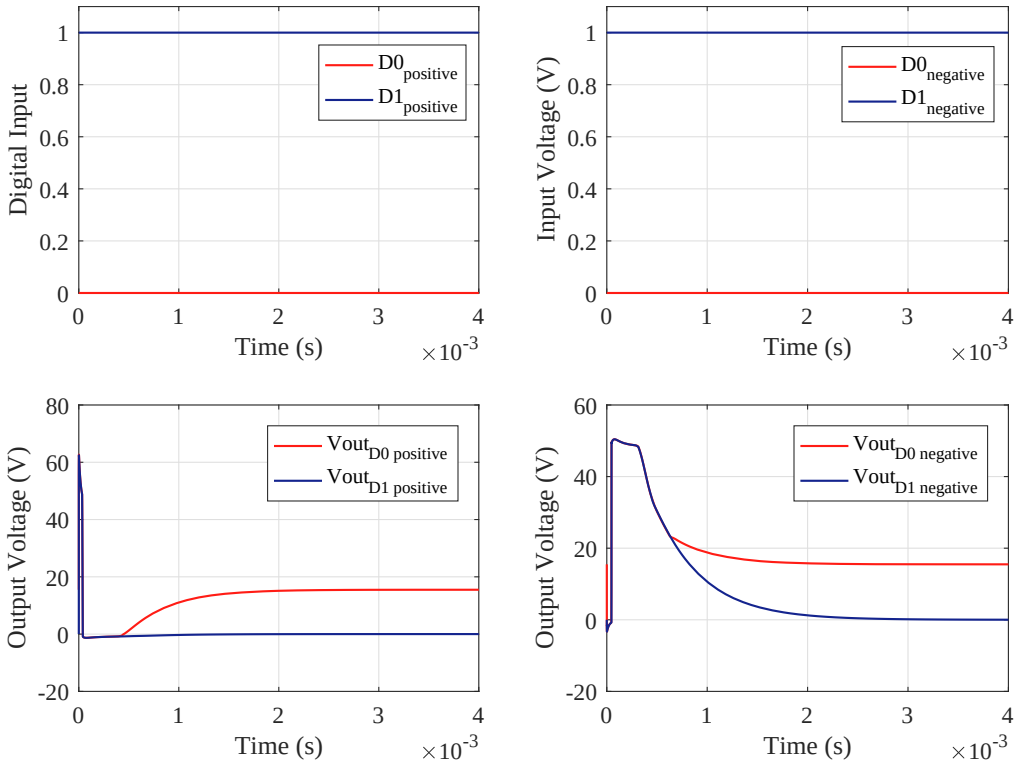


Figure 10-12: Surge Test for the DI TB0107 introducing the surge between *DOUT* and *Mdout*: (a) Digital input nDO for a positive surge. (b) Voltage at the PCC with a positive surge. (c) Digital input nDO for a negative surge. (d) Voltage at the PCC with a negative surge.

Paying attention to the figure it is possible to observe how in this case the configuration protects the system and the voltage does no reach more than 50V. These waveforms observed are the typical waveforms of a TVS, they clamp the peak voltage to a certain value and later it returns the system to the steady-state.

Since in this case there is no problem with the grounds, there is not any oscillation and as a consequence to the surge the system does not oscillate as it occurs with nDI and DI. It can be said that this configuration is the more suitable for the DO.

10.9 TB1350 Real case vs Simulation

Again the real behaviour of the system in this case for the Digital I/O of the TB1350 against the simulation will be discussed. It should be said that this circuit is going to have the same problem that the TB0107, since the Digital Output used an optocoupler instead of a Solid State Relay.

10.9.1 TB1350 Digital Inputs

PSpice simulation only

Figure 10-13. shows the PSpice simulation and the real one.

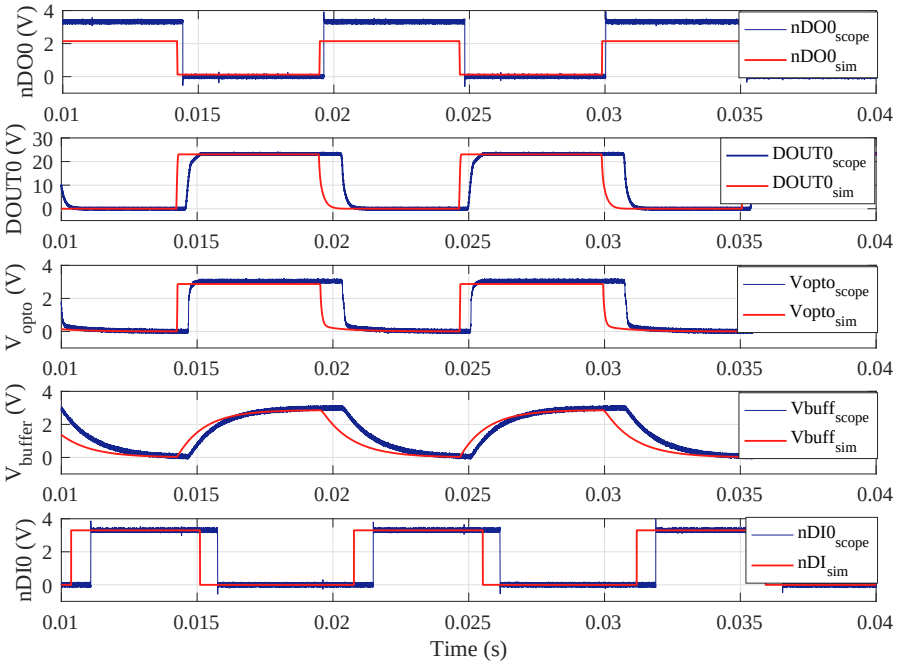


Figure 10-13: Simulation results of the nDI TB1350 compared with the real behaviour thereof: (a) Digital Input signal nDO converted to an analog signal. (b) Digital output DOUT. (c) Voltage at the ouput of the ouptocoupler of the digital input circuit nDI. (d) Voltage of the optocoupler filtered by an RC filter. (e) Digital output nDI.

Heeding the Figure 10-13. it is possible that the results obtained are similar to the real behaviour. However, they are not exact because of the solid state relay again.

Figure 10-14. shows the results of the simulation with the signal obtained from the simulation shifted.

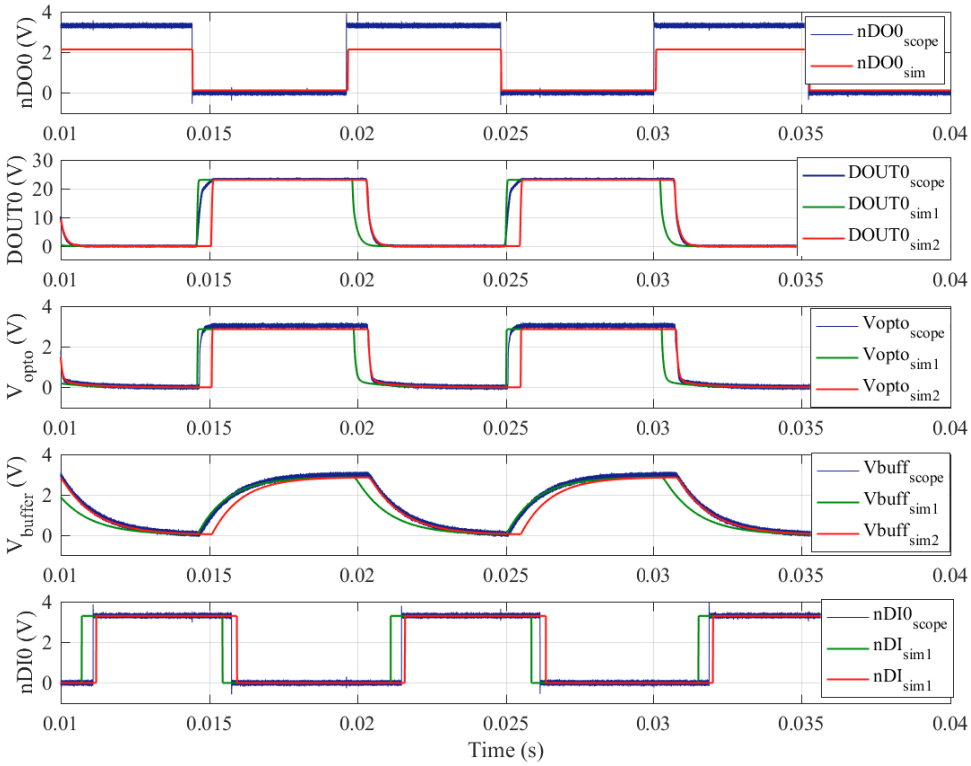


Figure 10-14: Simulation results of the nDI TB1350 with a phase shift compared with the real behaviour thereof: (a) Digital Input signal nDO converted to an analog signal. (b) Digital output DOUT. (c) Voltage at the ouput of the ouptocoupler of the digital input circuit nDI. (d) Voltage of the optocoupler filtered by an RC filter. (e) Digital output nDI.

As it can be seen, the waveforms are the correct ones, then, if a model of the solid state relay is achieved, a simulation with a high accuracy will be achieved.

PSpice simulation with real input voltage

In this case the input voltage is the one provided by the scopes. Figure 10-15. shows the results.

Again the same problem exhibited above is achieved.

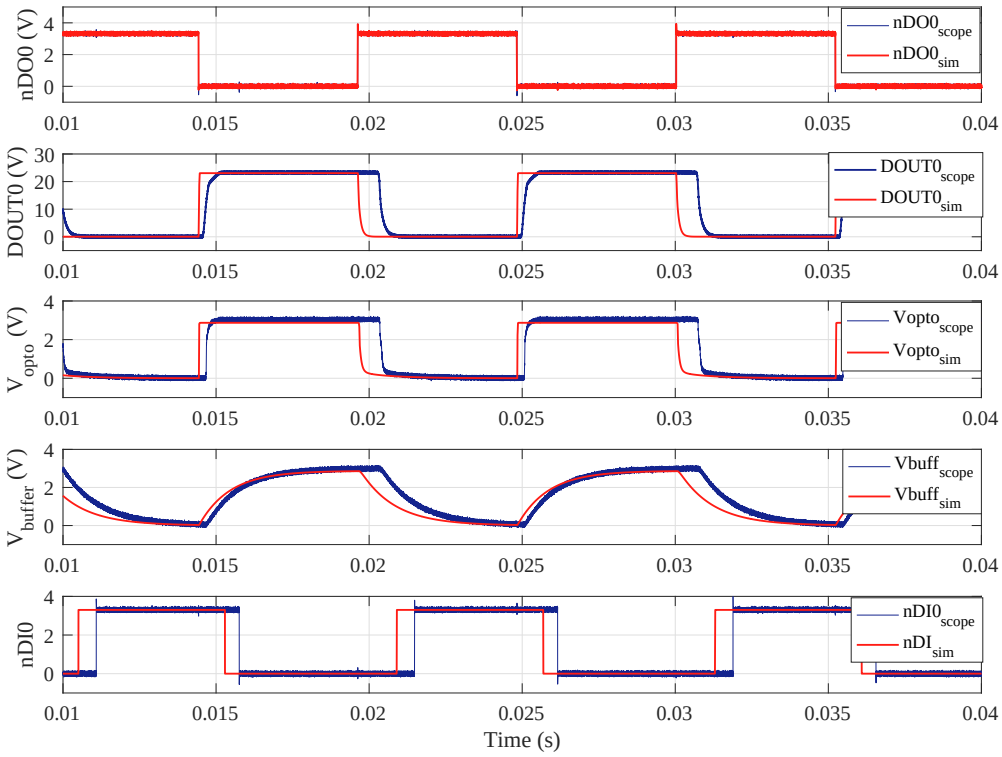


Figure 10-15: Simulation results of the nDI TB1350 with a real input signal compared with the real behaviour thereof: (a) Digital Input signal nDO converted to an analog signal. (b) Digital output DOUT. (c) Voltage at the ouput of the ouptocoupler of the digital input circuit nDI. (d) Voltage of the optocoupler filtered by an RC filter. (e) Digital output nDI.

10.9.2 TB1350 Fast Digital Inputs

PSpice simulation only

The results are shown in Figure 10-16.

Since the design of the DO is the same, the results are going to have the same problem explained above. Although the waveforms are the correct ones as it can be seen if a phase shift is introduced such as Figure 10-17 shows.

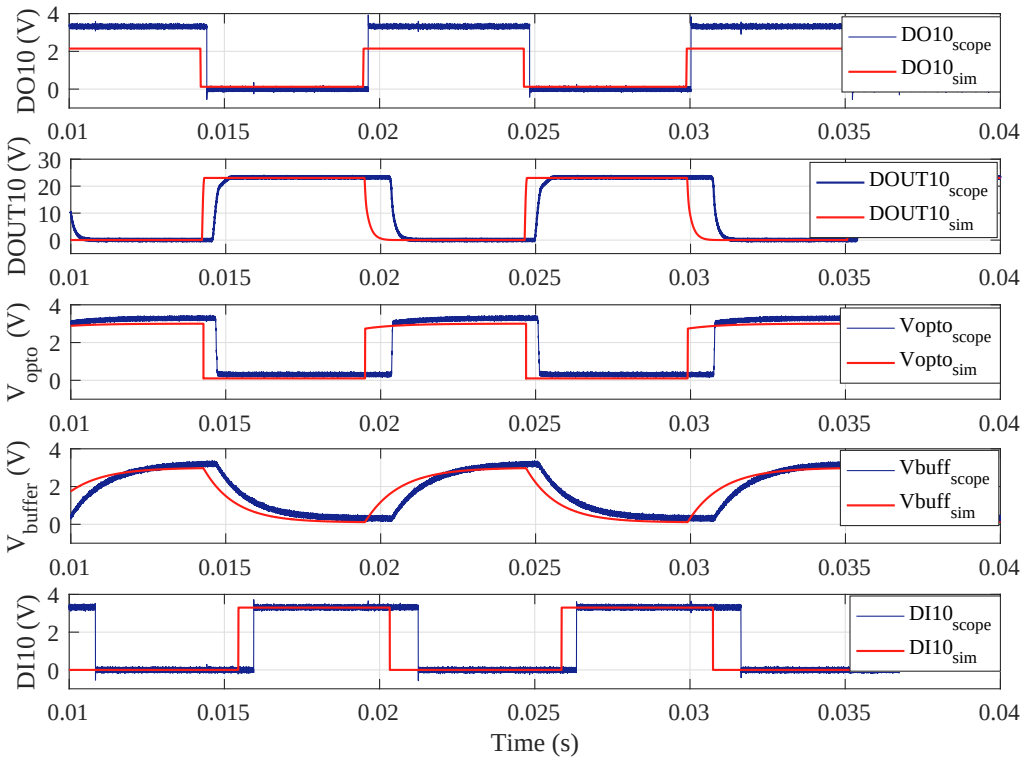


Figure 10-16: Simulation results of the DI TB1350 compared with the real behaviour thereof: (a) Digital Input signal nDO converted to an analog signal. (b) Digital output DOUT. (c) Voltage at the ouput of the ouptocoupler of the digital input circuit nDI. (d) Voltage of the optocoupler filtered by an RC filter. (e) Digital output nDI.

PSpice simulation with real input voltage

Figure 10-18. shows the results obtained for the nDI. This results will show the same error explained above.

10.10 Encoder

The encoder is a device which measures the position of the rotor and also its speed. There are several circuits of the encoder since there are more than one motor, in other words, for each motor a circuit of the encoder can be achieved. The number of motors equal to the number of Digital I/O is property of Ingeteam Power Technology.

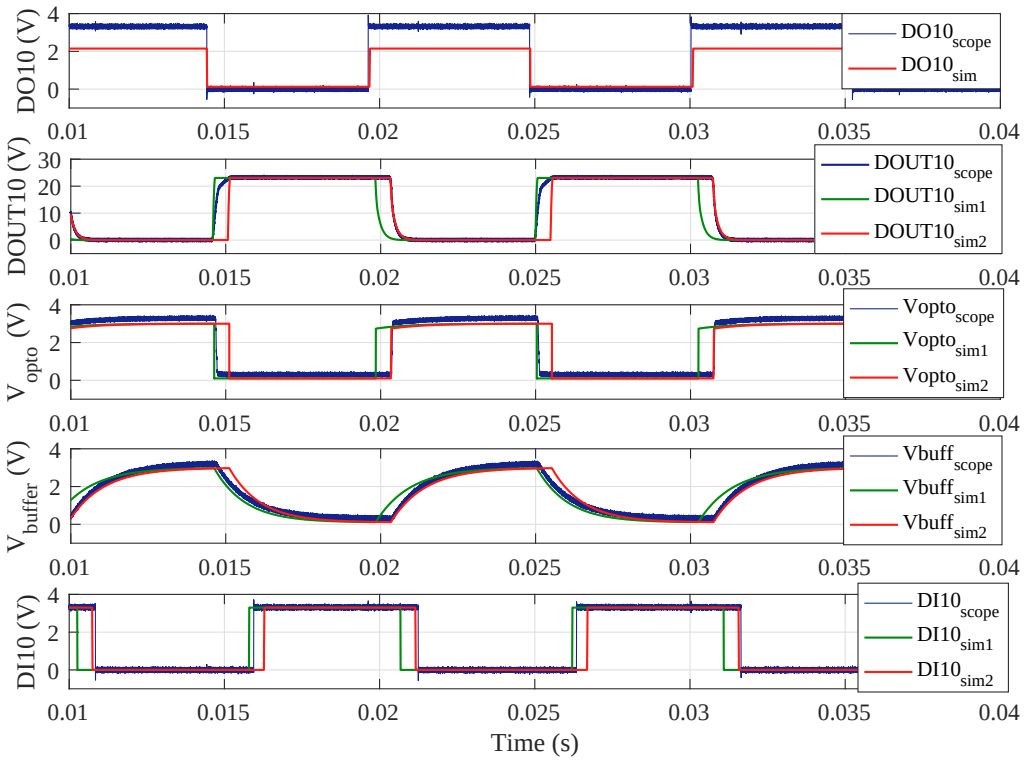


Figure 10-17: Simulation results of the DI TB1350 with a phase shift compared with the real behaviour thereof: (a) Digital Input signal nDO converted to an analog signal. (b) Digital output DOUT. (c) Voltage at the ouput of the ouptocoupler of the digital input circuit nDI. (d) Voltage of the optocoupler filtered by an RC filter. (e) Digital output nDI.

The encoder does not have TVS protections, hence, it does not make sense to perform a surge test.

10.10.1 Operation Point

The encoder used provides the information via two differential wires generating a voltage between ±24V. This input voltage is introduced inside an optocoupler with 4 inputs and 2 outputs. This is done like that because, depending on the value of the voltage, positive or negative, the output voltage will be positive or negative.

At the input of the circuit two Zener diodes can be achieved. In this case they will only conduct if the voltage is higher or equal to ±24V. There are two outputs as

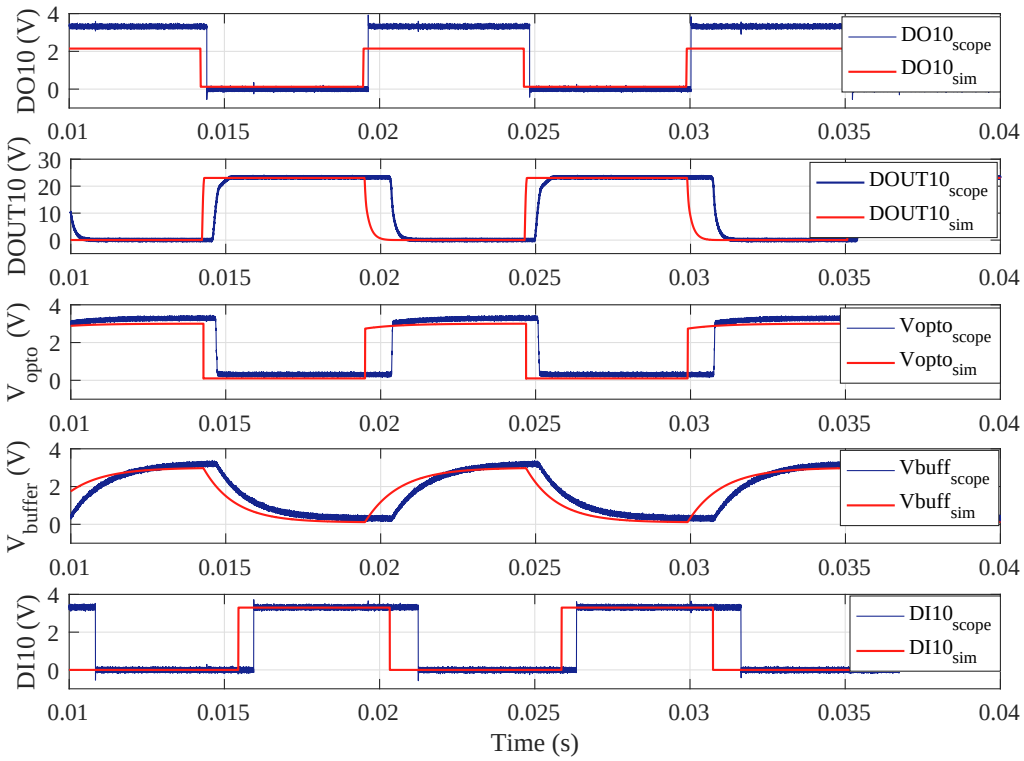


Figure 10-18: Simulation results of the DI TB1350 with a real input signal compared with the real behaviour thereof: (a) Digital Input signal nDO converted to an analog signal. (b) Digital output DOUT. (c) Voltage at the ouput of the ouptocoupler of the digital input circuit nDI. (d) Voltage of the optocoupler filtered by an RC filter. (e) Digital output nDI.

it has been said above, they are complementary to each other.

The output signals are digital signals, both signals are introduced into the FPGA in order to obtain all the parameters needed. Figure 10-19. shows the operation point of the encoder.

Heeding Figure 10-19. an operation similar to the one achieved in the Digital I/O can be achieved since most of the components are the same. Also it can be seen how the output channels are complementary.

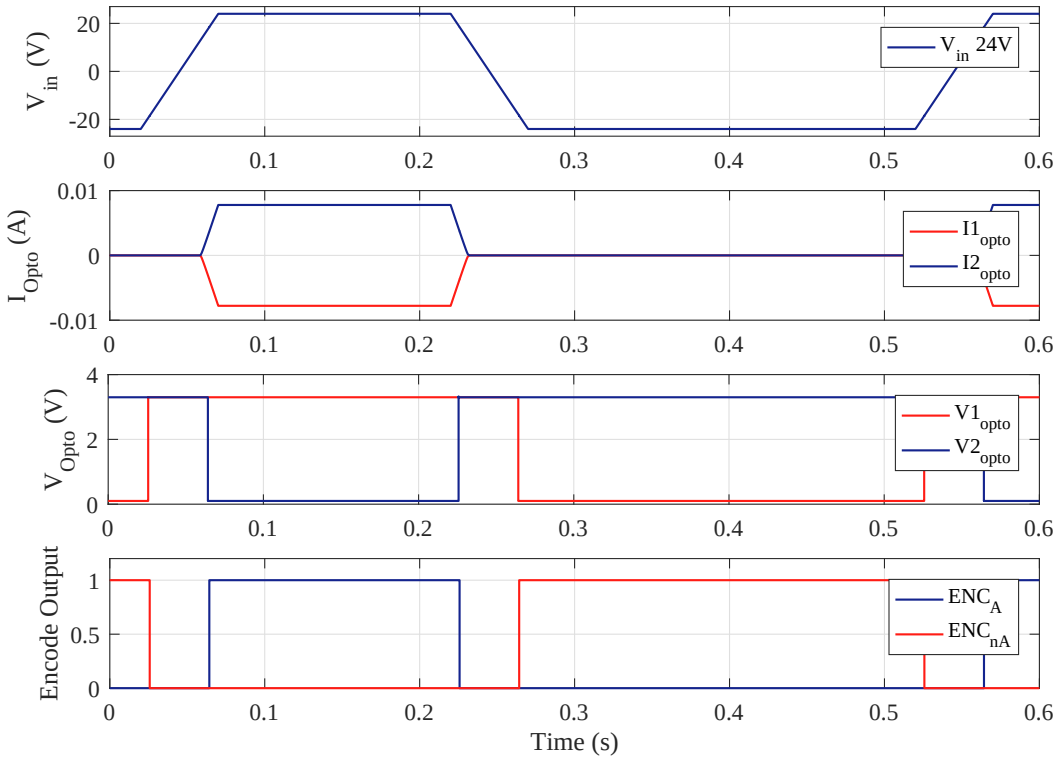


Figure 10-19: Transient simulation of the encoder: (a) Input voltage. (b) Current through the upper and lower LED of the optocoupler. (c) Output voltages of the optocoupler. (d) Two channel digital output of the encoder circuit.

10.10.2 Voltage Variation

Figures G-1. and G-2. of appendix G show the encoder working at different voltages. It should be said that this analysis does not make sense since the power supply of this circuit is constant. It is fed by a power supply instead of a battery, then the voltage does not come into play to vary. However, it is a good practise to see how this will affect the system if the voltage decreases or increases for any reason.

Paying attention to the figures it is possible to observe the effect aforementioned above. At 16.8V the system does not work as it is expected and at higher voltages it works perfectly.

10.10.3 Frequency Analysis

Figure G-3. of appendix G shows the behaviour of the system at different frequencies.It is expected from the encoder to work at high frequencies around 5kHz more or less.

Heeding the figure it is possible to see the operation limit which is 5kHz as it was expected. Table 10.7. summarises the phase shift between both voltages.

Table 10.7: Phase shift of encoder at different frequencies.

Encoder	
Frequency (Hz)	**Phase Shift (us)**
100	1
5000	0.7

Chapter 11

Conclusions

This MTh has been very useful, considerable knowledge has been achieved. First of all, a new tool which allows to make real models and also simulations has been used, this is the software OrCad from Cadence.

Secondly this project allows to combine the different knowledge areas that have been achieved during these two academic terms: from the simulation with real components in the software LTspice to the design of elements and schematics in Altium Designer. Furthermore, the concepts achieved during these years have made understanding the behaviour of the circuits easier.

One of the most complex parts of this project and its turning point is the development of the primitive components. This is because, although the components are well designed, problems with the circuit might still occur, but these problems are usually originated in the company circuit design.

Regarding the hierarchy and the simulations they can be considered one of the easiest parts since the circuits were done and there was no need of looking for the components. All the different grades of hierarchy have been seen throughout the project from making a simple hierarchy to develop hierarchical libraries that include the whole PCB. Even if this type of elements is not the most appropriate to do transient simulations they are useful for other types of analysis such as Montecarlo, Sensitive Analysis and so on.

It should be said that this project does not include the design check rules which

are the conditions of the paths, clearance and so on that must be defined in the stage previous to routing the PCB. However, this is done by an external company, then, it is not an important point.

Being critical there are several errors in the project that must be addressed. However, these can be solved easily, but due to the lack of time they have not been implemented, hence,the errors and their solutions will be discussed in the future developments chapter.

As a conclusion it can be said that the company is satisfied with the results, because there was not a previous simulation and now a new starting point with a solid base has been established. As it has been said above this project is far from ideal, but the most important thing is that both these errors and potential fixes and improvements are known, which from my point of view is one of the most important parts of a project. It lies in knowing what has been made and the range of accuracy under which it works.

Chapter 12

Future developments

12.1 Introduction

This is the final chapter of the project. Firstly, it addresses the errors of the project. Secondly, it deals with potential fixes to those errors and finally, future improvements for the project are discussed.

12.2 Errors of the project

As it has been said in the conclusions, there are several errors that must be addressed and fixed. The main errors of this project are:

- The Solid State Relay of the Digital Outputs has been replaced by an optocoupler, it has a similar behaviour but it is not the correct one. This fact has been proven in the Chapter 10 during the comparison of the simulation and the real case.
- The thermal models have not been calculated, the information is the one provided by the data-sheet. This could make the thermal behaviour wrong.
- The design check rules, as it has been indicated above, are not introduced. Furthermore, the footprint of the components has been downloaded but they have not been linked to the models.

- The grounds are not isolated, so a way of isolating them must be achieved. This is very important for the EMC test, in the transient simulation this will not affect the behaviour of the circuit.

12.3 Solutions to the errors

The errors mentioned are not very difficult to solve, the main problem is the time that they can consume.

The problem of the Solid State Relay can be solved by finding a model that has a behaviour identical to the real component, also it can be developed from zero, this option is the most difficult. Nevertheless, it is the most suitable in this case.

The thermal models are quite difficult because they depend on several factors, such as the position of the components, the separation between them, if they have a heat-sink, the conditions at which they are working, the size of the pad, the amount of copper that is near them, the varnish and so on. As it can be seen, it is quite difficult to achieve a valid thermal model; however, most of this information is known, then, it can be implemented by using a thermal model. The proposed methods are the Cauer or the Foster thermal model. The first one simulates a real case, the second one is a mathematical model, the nodes of the equivalent thermal circuit do not match the reality.

Regarding the design check rules, they can be defined in the routing stage, which has not been done since Ingeteam Power Technologies delegate this part of the project to external companies. The footprint as well must be only added to the components. All the footprints have been downloaded or done; notwithstanding, all of them must be reviewed.

Finally, the EMC problems due to the ground can be solved by generating references between the real ground, which is the earth, and the rest of the references. This is done by using a RC circuit with the resistance in series with the capacitor or LRC having an inductance in series with the parallel of the capacitor and the resistance.

It should be said that the first mentioned configuration, which includes a RC

between the reference of the model and the isolated ground (which is a reference of voltage provided by the DC/DC voltage sources), has been tested. The resistance has been given a high value of $1M\Omega$ and the capacitor has been given a low value of $1pF$. The capacitor simulates the PCB material and the big resistor is used to avoid current flowing. However, this is just a simple test, but since its soundness was not tested, it was discarded.

12.4 Other improvements

Future developments will continue simulating the Electra until all the different parts exposed are achieved. But previously, a verification of all the components is needed.

Other kinds of analysis that are interesting to do are the Montecarlo, the Worst-Case Analysis and also the Sensitive Analysis. These are useful improvements that can be easily done but the most important part is to consolidate the libraries.

By doing this the project will have a strong base which will allow to make changes very fast and with the assurance that the circuit is working as it is expected.

Another option involves including sensors to measure the critical points of the Electra to later compare it with the simulation and ascertain the accuracy of the simulations, as it has been done in the project. These are the most important ideas that can improve the project.

Appendix A

Figures of nDI TB0107

A.1 Voltage Variation for nDI TB0107: 16.8V, 24V, 30V

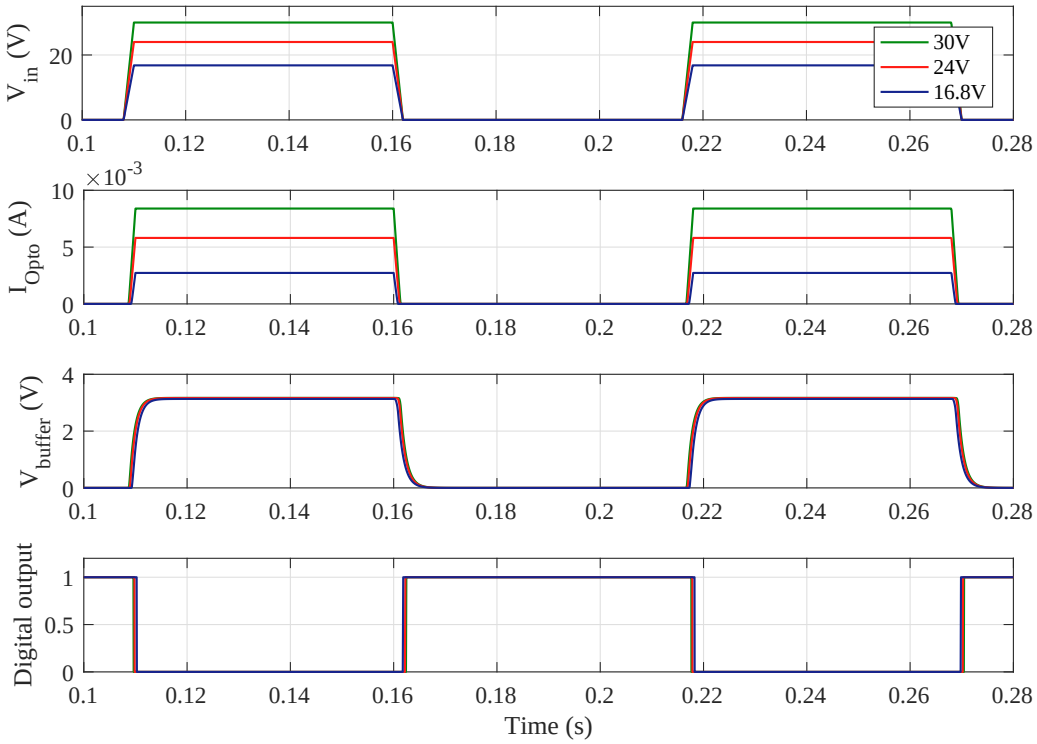


Figure A-1: Transient simulation of the nDI of TB0107 for 16.8V, 24V and 30V: (a) Input voltage. (b) Current flowing through the optocoupler's LED. (c) Voltage at the ouput of the ouptocoupler and the voltage resultant after appliying a RC filter. (d) Digital output nDI.

A.2 Frequency variation for nDI TB0107

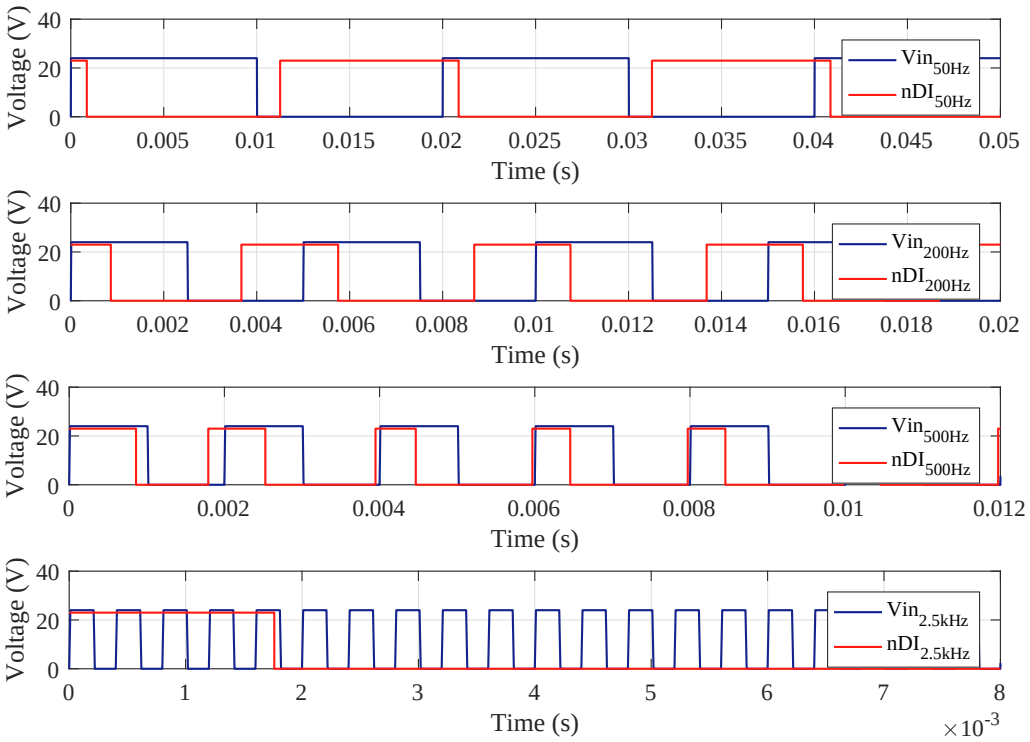


Figure A-2: Frequency variation for nDI TB0107: (a) 50Hz. (b) 200Hz. (c) 500Hz. (d) 2500Hz.

A.3 Surge Test for nDI TB0107 without TVS

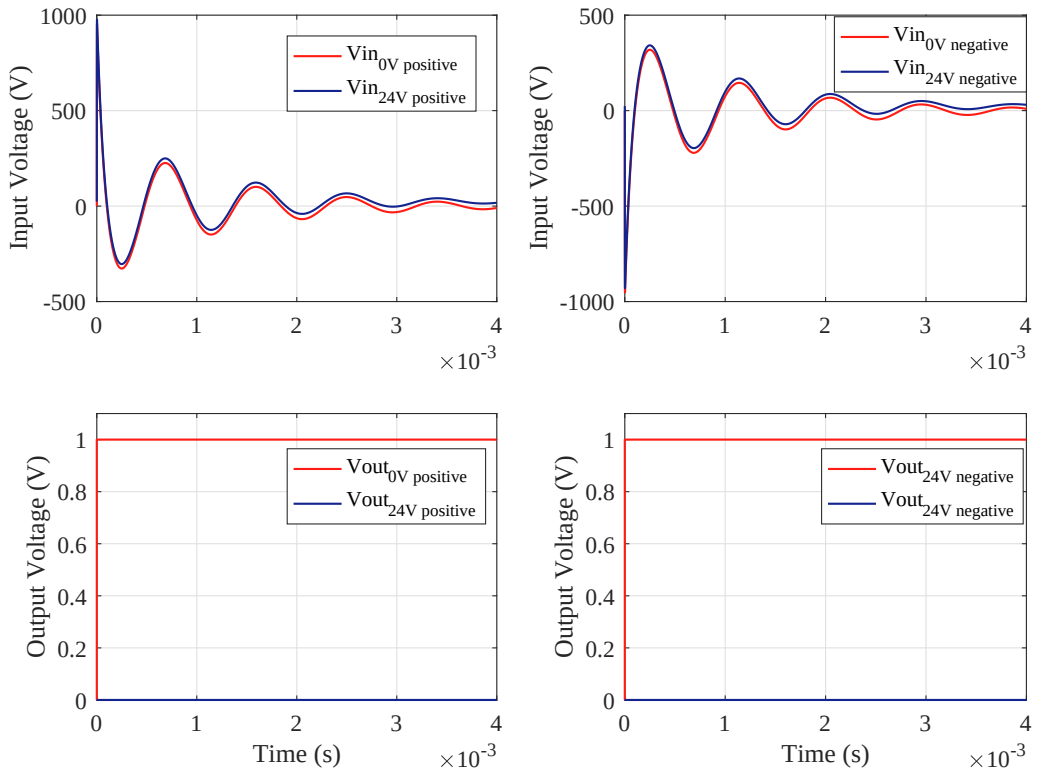


Figure A-3: Surge Test for the nDI TB0107 without TVS: (a) Input voltage at the PCC with a positive surge (b) nDI response to a positive surge. (c) Input voltage at the PCC with a negative surge. (d) nDI response to a negative surge.

A.4 Surge Test for nDI TB0107 with TVS

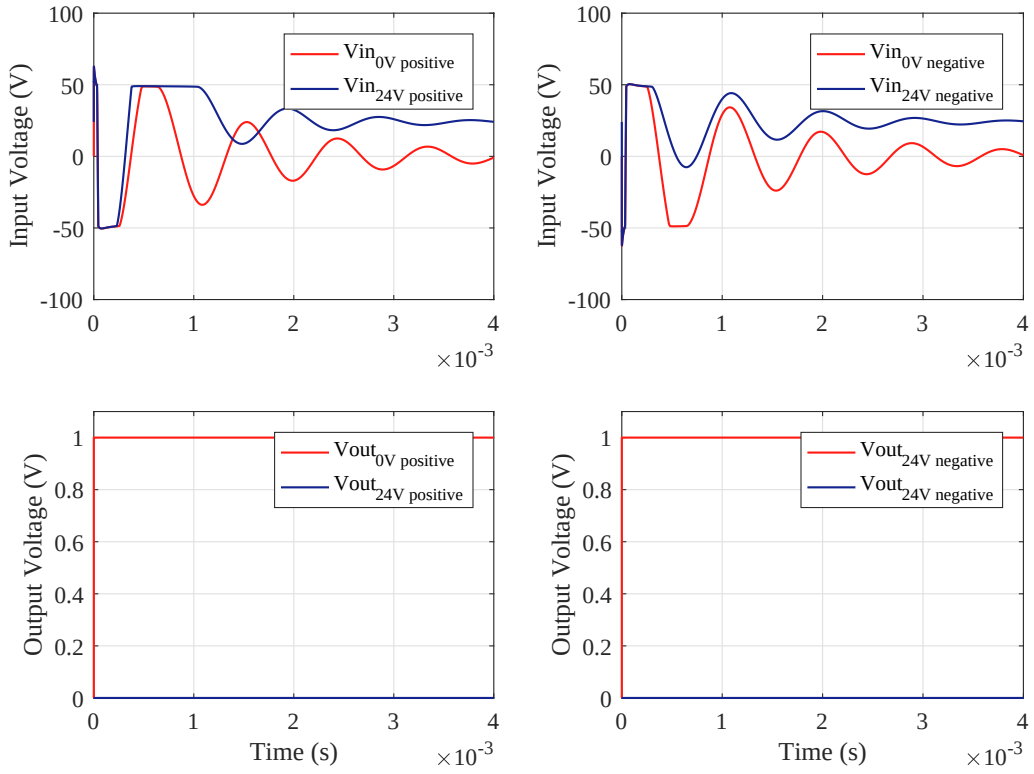


Figure A-4: Surge Test for the nDI TB0107 with TVS: (a) Input voltage at the PCC with a positive surge (b) nDI response to a positive surge. (c) Input voltage at the PCC with a negative surge. (d) nDI response to a negative surge.

A.5 Smoke Analysis for nDI TB0107

A.5.1 Original nDI TB0107

Smoke - opto_1.sim [Derating File: DeRating.drt] Component Filter = [*]

♦	Component	Parameter	Type	Rated Value	% Derating	Max Derating	Measured Value	% Max
	V7	Max Reverse Current	RMS	1u	100	1u	7.6113u	762
	V7	Max Reverse Current	Peak	1u	100	1u	1.5965u	160
	R14	Maximum power dissipation	Peak	250m	50	125m	160.1423m	129
	R15	Maximum power dissipation	Peak	250m	50	125m	160.1423m	129
	R14	Maximum breakdown temperature	Peak	155	80	124	155.1139	126
	R15	Maximum breakdown temperature	Peak	155	80	124	155.1139	126
	R14	Maximum breakdown temperature	RMS	155	80	124	105.2789	85
	R15	Maximum breakdown temperature	RMS	155	80	124	105.2789	85
	R14	Maximum power dissipation	RMS	250m	50	125m	97.8486m	79
	R15	Maximum power dissipation	RMS	250m	50	125m	97.8486m	79
	C1	Maximum voltage	Peak	50	80	40	30	75
	R14	Maximum breakdown temperature	Average	155	80	124	78.2456	64
	R15	Maximum breakdown temperature	Average	155	80	124	78.2456	64
	R14	Maximum power dissipation	Average	250m	50	125m	64.0569m	52
	R15	Maximum power dissipation	Average	250m	50	125m	64.0569m	52
	C1	Maximum voltage	RMS	50	80	40	18.9737	48
	D3	Maximum junction temperature	Peak	175	69	122.5000	45.4135	38
	D2	Maximum junction temperature	Peak	175	69	122.5000	45.4135	38
	K1	NPN max E-C vol	RMS	7	100	7	2.4341	35
	R8	Maximum breakdown temperature	Peak	155	80	124	41.1633	34
	R5	Maximum breakdown temperature	Peak	155	80	124	41.1633	34
	R4	Maximum breakdown temperature	Peak	155	80	124	41.1633	34
	R3	Maximum breakdown temperature	Peak	155	80	124	41.1633	34
	R10	Maximum breakdown temperature	Peak	155	80	124	41.1633	34
	R6	Maximum breakdown temperature	Peak	155	80	124	41.1633	34
	R9	Maximum breakdown temperature	Peak	155	80	124	41.1633	34
	R7	Maximum breakdown temperature	Peak	155	80	124	41.1633	34
	C1	Maximum voltage	Average	50	80	40	13.0000	33
	D3	Maximum junction temperature	RMS	175	69	122.5000	38.2574	32
	D2	Maximum junction temperature	RMS	175	69	122.5000	38.2574	32
	V8	Maximum junction temperature	Average	85	100	85	27	32
	V8	Maximum junction temperature	Peak	85	100	85	27	32
	V8	Maximum junction temperature	RMS	85	100	85	27	32
	V8	Max reverse voltage	RMS	5	100	5	1.5424	31
	R8	Maximum breakdown temperature	RMS	155	80	124	35.4775	29
	R5	Maximum breakdown temperature	RMS	155	80	124	35.4775	29
	R4	Maximum breakdown temperature	RMS	155	80	124	35.4775	29
	R3	Maximum breakdown temperature	RMS	155	80	124	35.4775	29
	R10	Maximum breakdown temperature	RMS	155	80	124	35.4775	29
	R6	Maximum breakdown temperature	RMS	155	80	124	35.4775	29
	R9	Maximum breakdown temperature	RMS	155	80	124	35.4775	29
	R7	Maximum breakdown temperature	RMS	155	80	124	35.4775	29
	R12	Maximum breakdown temperature	Peak	155	80	124	35.4974	29

Smoke - opto_1.sim [Derating File: DeRating.drt] Component Filter = [*]

♦	Component	Parameter	Type	Rated Value	% Derating	Max Derating	Measured Value	% Max
	D3	Maximum junction temperature	Average	175	69	122.5000	34.2793	28
	D2	Maximum junction temperature	Average	175	69	122.5000	34.2793	28
	R8	Maximum breakdown temperature	Average	155	80	124	32.3109	27
	R5	Maximum breakdown temperature	Average	155	80	124	32.3109	27
	R4	Maximum breakdown temperature	Average	155	80	124	32.3109	27
	R3	Maximum breakdown temperature	Average	155	80	124	32.3109	27
	R10	Maximum breakdown temperature	Average	155	80	124	32.3109	27
	R6	Maximum breakdown temperature	Average	155	80	124	32.3109	27
	R9	Maximum breakdown temperature	Average	155	80	124	32.3109	27
	R7	Maximum breakdown temperature	Average	155	80	124	32.3109	27
	R12	Maximum breakdown temperature	RMS	155	80	124	32.5369	27
	R12	Maximum breakdown temperature	Average	155	80	124	30.6612	25
	R13	Maximum breakdown temperature	Peak	155	80	124	29.0079	24
	R13	Maximum breakdown temperature	Average	155	80	124	27.8920	23
	R13	Maximum breakdown temperature	RMS	155	80	124	28.3274	23
	R11	Maximum breakdown temperature	Average	155	80	124	27.0012	22
	R11	Maximum breakdown temperature	Peak	155	80	124	27.0595	22
	R11	Maximum breakdown temperature	RMS	155	80	124	27.0063	22
	D3	Maximum power dissipation	Peak	296m	64	191m	36.8271m	20
	D1	Maximum junction temperature	Average	200	70	140	27	20
	D1	Maximum junction temperature	Peak	200	70	140	27	20
	D1	Maximum junction temperature	RMS	200	70	140	27	20
	D2	Maximum power dissipation	Peak	296m	64	191m	36.8271m	20
	K1	LED max If	Peak	80m	50	40m	7.6551m	20
	V7	Maximum junction temperature	Average	150	100	150	27	19
	V7	Maximum junction temperature	Peak	150	100	150	27	19
	V7	Maximum junction temperature	RMS	150	100	150	27	19
	R14	Maximum voltage	Peak	200	80	160	30	19
	R15	Maximum voltage	Peak	200	80	160	30	19
	K1	LED max rev voltage	RMS	6	75	4.5000	800.3559m	18
	V8	Maximum power dissipation	Peak	62.5000m	100	62.5000m	11.1486m	18
	D1	Max forward current	Peak	100m	50	50m	7.6577m	16
	R8	Maximum power dissipation	Peak	250m	50	125m	17.7041m	15
	R5	Maximum power dissipation	Peak	250m	50	125m	17.7041m	15
	R4	Maximum power dissipation	Peak	250m	50	125m	17.7041m	15
	R3	Maximum power dissipation	Peak	250m	50	125m	17.7041m	15
	R10	Maximum power dissipation	Peak	250m	50	125m	17.7041m	15
	R6	Maximum power dissipation	Peak	250m	50	125m	17.7041m	15
	R9	Maximum power dissipation	Peak	250m	50	125m	17.7041m	15
	R7	Maximum power dissipation	Peak	250m	50	125m	17.7041m	15
	K1	NPN max Ic	Peak	50m	80	40m	5.1797m	13
	D3	Maximum power dissipation	RMS	296m	64	191m	22.5148m	12
	D2	Maximum power dissipation	RMS	296m	64	191m	22.5148m	12
	K1	LED max If	RMS	80m	50	40m	4.6852m	12

Smoke - opto_1.sim [Derating File: DeRating.drt] Component Filter = [*]

♦	Component	Parameter	Type	Rated Value	% Derating	Max Derating	Measured Value	% Max
	V8	Maximum power dissipation	RMS	62.5000m	100	62.5000m	7.3092m	12
	R14	Maximum voltage	RMS	200	80	160	18.9737	12
	R15	Maximum voltage	RMS	200	80	160	18.9737	12
	D1	Max forward current	RMS	100m	50	50m	4.6846m	10
	R8	Maximum power dissipation	RMS	250m	50	125m	10.5969m	9
	R5	Maximum power dissipation	RMS	250m	50	125m	10.5969m	9
	R4	Maximum power dissipation	RMS	250m	50	125m	10.5969m	9
	R3	Maximum power dissipation	RMS	250m	50	125m	10.5969m	9
	R10	Maximum power dissipation	RMS	250m	50	125m	10.5969m	9
	R6	Maximum power dissipation	RMS	250m	50	125m	10.5969m	9
	R9	Maximum power dissipation	RMS	250m	50	125m	10.5969m	9
	R7	Maximum power dissipation	RMS	250m	50	125m	10.5969m	9
	K1	NPN max Ic	RMS	50m	80	40m	3.3995m	9
	R12	Maximum power dissipation	Peak	100m	50	50m	4.2487m	9
	R14	Maximum voltage	Average	200	80	160	13.0000	9
	R15	Maximum voltage	Average	200	80	160	13.0000	9
	D3	Max Reverse Current	Peak	104.1660m	100	104.1660m	7.6548m	8
	D3	Maximum power dissipation	Average	296m	64	191m	14.5585m	8
	D2	Max Reverse Current	Peak	104.1660m	100	104.1660m	7.6548m	8
	D2	Maximum power dissipation	Average	296m	64	191m	14.5585m	8
	K1	LED max If	Average	80m	50	40m	3.0301m	8
	C2	Maximum voltage	Peak	50	80	40	3.1685	8
	V8	Maximum power dissipation	Average	62.5000m	100	62.5000m	4.8646m	8
	D1	Max forward current	Average	100m	50	50m	3.0297m	7
	R8	Maximum power dissipation	Average	250m	50	125m	6.6386m	6
	R5	Maximum power dissipation	Average	250m	50	125m	6.6386m	6
	R4	Maximum power dissipation	Average	250m	50	125m	6.6386m	6
	R3	Maximum power dissipation	Average	250m	50	125m	6.6386m	6
	R10	Maximum power dissipation	Average	250m	50	125m	6.6386m	6
	R6	Maximum power dissipation	Average	250m	50	125m	6.6386m	6
	R9	Maximum power dissipation	Average	250m	50	125m	6.6386m	6
	R7	Maximum power dissipation	Average	250m	50	125m	6.6386m	6
	K1	NPN max Ic	Average	50m	80	40m	2.2669m	6
	K1	NPN max C-E vol	Peak	80	75	60	3.3000	6
	C2	Maximum voltage	RMS	50	80	40	2.0811	6
	R12	Maximum power dissipation	RMS	100m	50	50m	2.7684m	6
	R13	Maximum voltage	Peak	75	80	60	3.1685	6
	D3	Max Reverse Current	RMS	104.1660m	100	104.1660m	4.6808m	5
	D2	Max Reverse Current	RMS	104.1660m	100	104.1660m	4.6808m	5
	K1	Maximum power dissipation	Peak	210m	100	210m	9.6326m	5
	K1	NPN max C-E vol	RMS	80	75	60	2.4341	5
	R11	Maximum voltage	Peak	50	80	40	1.7248	5
	K1	NPN max C-E vol	Average	80	75	60	1.8720	4
	C2	Maximum voltage	Average	50	80	40	1.4070	4

Smoke - opto_1.sim [Derating File: DeRating.drt] Component Filter = [*]

♦	Component	Parameter	Type	Rated Value	% Derating	Max Derating	Measured Value	% Max
	V8	Max forward current	Peak	140m	100	140m	4.8601m	4
	R12	Maximum power dissipation	Average	100m	50	50m	1.8306m	4
	R13	Maximum voltage	RMS	75	80	60	2.1119	4
	D3	Max Reverse Current	Average	104.1660m	100	104.1660m	3.0274m	3
	R8	Maximum voltage	Peak	200	80	160	4.6284	3
	D1	Maximum power dissipation	Peak	500m	50	250m	5.4193m	3
	R5	Maximum voltage	Peak	200	80	160	4.6284	3
	D2	Max Reverse Current	Average	104.1660m	100	104.1660m	3.0274m	3
	R4	Maximum voltage	Peak	200	80	160	4.6284	3
	R3	Maximum voltage	Peak	200	80	160	4.6284	3
	R10	Maximum voltage	Peak	200	80	160	4.6284	3
	R6	Maximum voltage	Peak	200	80	160	4.6284	3
	R9	Maximum voltage	Peak	200	80	160	4.6284	3
	R7	Maximum voltage	Peak	200	80	160	4.6284	3
	K1	Maximum power dissipation	RMS	210m	100	210m	5.8752m	3
	V8	Max forward current	RMS	140m	100	140m	3.1884m	3
	R12	Maximum voltage	Peak	50	80	40	874.5102m	3
	R13	Maximum power dissipation	Peak	100m	50	50m	1.0039m	3
	R13	Maximum voltage	Average	75	80	60	1.4280	3
	D3	Max Forward Current	RMS	250m	100	250m	4.6808m	2
	R8	Maximum voltage	Average	200	80	160	1.8330	2
	R8	Maximum voltage	RMS	200	80	160	2.8342	2
	D1	Maximum power dissipation	RMS	500m	50	250m	3.3062m	2
	R5	Maximum voltage	Average	200	80	160	1.8330	2
	R5	Maximum voltage	RMS	200	80	160	2.8342	2
	D2	Max Forward Current	RMS	250m	100	250m	4.6808m	2
	R4	Maximum voltage	Average	200	80	160	1.8330	2
	R4	Maximum voltage	RMS	200	80	160	2.8342	2
	R3	Maximum voltage	Average	200	80	160	1.8330	2
	R3	Maximum voltage	RMS	200	80	160	2.8342	2
	R10	Maximum voltage	Average	200	80	160	1.8330	2
	R10	Maximum voltage	RMS	200	80	160	2.8342	2
	R6	Maximum voltage	Average	200	80	160	1.8330	2
	R6	Maximum voltage	RMS	200	80	160	2.8342	2
	R9	Maximum voltage	Average	200	80	160	1.8330	2
	R9	Maximum voltage	RMS	200	80	160	2.8342	2
	R7	Maximum voltage	Average	200	80	160	1.8330	2
	R7	Maximum voltage	RMS	200	80	160	2.8342	2
	K1	Maximum power dissipation	Average	210m	100	210m	3.8373m	2
	V8	Max forward current	Average	140m	100	140m	2.1235m	2
	R12	Maximum voltage	RMS	50	80	40	574.0249m	2
	R13	Maximum power dissipation	RMS	100m	50	50m	663.7016u	2
	D3	Max Forward Current	Peak	250m	100	250m	13.8406n	1
	V7	Max Forward Current	Average	100	100	100	5.5475u	1

Smoke - opto_1.sim [Derating File: DeRating.drt] Component Filter = [*]

♦	Component	Parameter	Type	Rated Value	% Derating	Max Derating	Measured Value	% Max
	V7	Max Forward Current	Peak	100	100	100	12.9399u	1
	V7	Max Forward Current	RMS	100	100	100	7.6113u	1
	V7	Maximum power dissipation	Average	515	100	515	134.9861u	1
	V7	Maximum power dissipation	Peak	515	100	515	327.7653u	1
	V7	Maximum power dissipation	RMS	515	100	515	196.9467u	1
	D1	Maximum power dissipation	Average	500m	50	250m	2.1313m	1
	D1	Peak reverse voltage	Peak	100	75	75	543.7516m	1
	D1	Peak reverse voltage	RMS	100	75	75	478.7018m	1
	D2	Max Forward Current	Peak	250m	100	250m	13.8408n	1
	C1	Maximum current	Average	1	100	1	200.0019n	1
	C1	Maximum current	Peak	1	100	1	3.1148u	1
	C1	Maximum current	RMS	1	100	1	1.3416u	1
	K1	LED max rev voltage	Peak	6	75	4.5000	6.4438p	1
	R11	Maximum power dissipation	Average	100m	50	50m	624.7089n	1
	R11	Maximum power dissipation	Peak	100m	50	50m	29.7480u	1
	R11	Maximum power dissipation	RMS	100m	50	50m	3.1718u	1
	R11	Maximum voltage	Average	50	80	40	21.0341m	1
	R11	Maximum voltage	RMS	50	80	40	249.9418m	1
	C2	Maximum current	Average	1	100	1	210.2693n	1
	C2	Maximum current	Peak	1	100	1	17.2416u	1
	C2	Maximum current	RMS	1	100	1	2.4985u	1
	R12	Maximum voltage	Average	50	80	40	382.3047m	1
	R13	Maximum power dissipation	Average	100m	50	50m	445.9992u	1
	D3	Max Forward Current	Average	250m	100	250m	-3.0274m	0
	V7	Max Reverse Current	Average	1u	100	1u	-5.5475u	0
	D1	Peak reverse voltage	Average	100	75	75	-318.3508m	0
	D2	Max Forward Current	Average	250m	100	250m	-3.0274m	0
	K1	NPN max E-C vol	Average	7	100	7	-1.8720	0
	K1	NPN max E-C vol	Peak	7	100	7	-131.4865m	0
	K1	LED max rev voltage	Average	6	75	4.5000	-587.9623m	0
	V8	Max reverse voltage	Average	5	100	5	-1.0457	0
	V8	Max reverse voltage	Peak	5	100	5	-36.4706u	0

A.5.2 Current nDI TB0107

Without De-rated factors

Smoke - transient ndi.sim [No Derating] Component Filter = [*]

♦	Component	Parameter	Type	Rated Value	% Derating	Max Derating	Measured Value	% Max
	V5	Max Reverse Current	RMS	1u	100	1u	7.8069u	781
	V5	Max Reverse Current	Peak	1u	100	1u	1.5869u	159
	C1	Maximum voltage	Peak	50	100	50	30	60
	R2	Maximum breakdown temperature	Peak	155	100	155	92.4545	60
	R1	Maximum breakdown temperature	Peak	155	100	155	92.4545	60
	R2	Maximum breakdown temperature	RMS	155	100	155	69.0389	45
	R1	Maximum breakdown temperature	RMS	155	100	155	69.0389	45
	C1	Maximum voltage	RMS	50	100	50	19.8431	40
	R2	Maximum breakdown temperature	Average	155	100	155	55.6364	36
	R1	Maximum breakdown temperature	Average	155	100	155	55.6364	36
	K1	NPN max E-C vol	RMS	7	100	7	2.3450	34
	R2	Maximum power dissipation	Peak	250m	100	250m	81.8182m	33
	R1	Maximum power dissipation	Peak	250m	100	250m	81.8182m	33
	V6	Max reverse voltage	RMS	5	100	5	1.6086	33
	V6	Maximum junction temperature	Average	85	100	85	27	32
	V6	Maximum junction temperature	Peak	85	100	85	27	32
	V6	Maximum junction temperature	RMS	85	100	85	27	32
	C1	Maximum voltage	Average	50	100	50	14.0625	29
	R8	Maximum breakdown temperature	Peak	155	100	155	43.1937	28
	R7	Maximum breakdown temperature	Peak	155	100	155	43.1937	28
	R6	Maximum breakdown temperature	Peak	155	100	155	43.1937	28
	R5	Maximum breakdown temperature	Peak	155	100	155	43.1937	28
	R4	Maximum breakdown temperature	Peak	155	100	155	43.1937	28
	R3	Maximum breakdown temperature	Peak	155	100	155	43.1937	28
	R10	Maximum breakdown temperature	Peak	155	100	155	43.1937	28
	R9	Maximum breakdown temperature	Peak	155	100	155	43.1937	28
	D2	Maximum junction temperature	Peak	175	100	175	45.5330	27
	D1	Maximum junction temperature	Peak	175	100	175	45.5338	27
	R8	Maximum breakdown temperature	RMS	155	100	155	37.2337	25
	R7	Maximum breakdown temperature	RMS	155	100	155	37.2337	25
	R6	Maximum breakdown temperature	RMS	155	100	155	37.2337	25
	R5	Maximum breakdown temperature	RMS	155	100	155	37.2337	25
	R4	Maximum breakdown temperature	RMS	155	100	155	37.2337	25
	R3	Maximum breakdown temperature	RMS	155	100	155	37.2337	25
	R10	Maximum breakdown temperature	RMS	155	100	155	37.2337	25
	R9	Maximum breakdown temperature	RMS	155	100	155	37.2337	25
	D2	Maximum junction temperature	RMS	175	100	175	38.9358	23
	D1	Maximum junction temperature	RMS	175	100	175	38.9351	23
	R11	Maximum breakdown temperature	Peak	155	100	155	35.5156	23
	R8	Maximum breakdown temperature	Average	155	100	155	33.7314	22
	R7	Maximum breakdown temperature	Average	155	100	155	33.7314	22
	R2	Maximum power dissipation	RMS	250m	100	250m	52.5487m	22
	R6	Maximum breakdown temperature	Average	155	100	155	33.7314	22

Smoke - transient ndi.sim [No Derating] Component Filter = [*]

♦	Component	Parameter	Type	Rated Value	% Derating	Max Derating	Measured Value	% Max
	R5	Maximum breakdown temperature	Average	155	100	155	33.7314	22
	R4	Maximum breakdown temperature	Average	155	100	155	33.7314	22
	R3	Maximum breakdown temperature	Average	155	100	155	33.7314	22
	R10	Maximum breakdown temperature	Average	155	100	155	33.7314	22
	R1	Maximum power dissipation	RMS	250m	100	250m	52.5487m	22
	R11	Maximum breakdown temperature	RMS	155	100	155	32.8176	22
	R9	Maximum breakdown temperature	Average	155	100	155	33.7314	22
	D2	Maximum junction temperature	Average	175	100	175	35.0743	21
	D1	Maximum junction temperature	Average	175	100	175	35.0738	21
	R11	Maximum breakdown temperature	Average	155	100	155	31.0236	21
	V5	Maximum junction temperature	Average	150	100	150	27	19
	V5	Maximum junction temperature	Peak	150	100	150	27	19
	V5	Maximum junction temperature	RMS	150	100	150	27	19
	R12	Maximum breakdown temperature	Average	155	100	155	27.9737	19
	R12	Maximum breakdown temperature	Peak	155	100	155	29.0093	19
	R12	Maximum breakdown temperature	RMS	155	100	155	28.3893	19
	R13	Maximum breakdown temperature	Average	155	100	155	27.0012	18
	R13	Maximum breakdown temperature	Peak	155	100	155	27.0608	18
	R13	Maximum breakdown temperature	RMS	155	100	155	27.0063	18
	V6	Maximum power dissipation	Peak	62.5000m	100	62.5000m	11.1663m	18
	R2	Maximum voltage	Peak	200	100	200	30	16
	R1	Maximum voltage	Peak	200	100	200	30	16
	R2	Maximum power dissipation	Average	250m	100	250m	35.7955m	15
	R1	Maximum power dissipation	Average	250m	100	250m	35.7955m	15
	K1	LED max rev voltage	RMS	6	100	6	836.0862m	14
	D3	Maximum junction temperature	Average	200	100	200	27	14
	D3	Maximum junction temperature	Peak	200	100	200	27	14
	D3	Maximum junction temperature	RMS	200	100	200	27	14
	D2	Maximum power dissipation	Peak	296m	100	296m	37.0660m	13
	D1	Maximum power dissipation	Peak	296m	100	296m	37.0676m	13
	V6	Maximum power dissipation	RMS	62.5000m	100	62.5000m	7.6653m	13
	K1	NPN max Ic	Peak	50m	100	50m	5.1840m	11
	K1	LED max If	Peak	80m	100	80m	8.3986m	11
	R2	Maximum voltage	RMS	200	100	200	19.8431	10
	R1	Maximum voltage	RMS	200	100	200	19.8431	10
	R8	Maximum power dissipation	Peak	250m	100	250m	20.2422m	9
	R7	Maximum power dissipation	Peak	250m	100	250m	20.2422m	9
	R6	Maximum power dissipation	Peak	250m	100	250m	20.2422m	9
	R5	Maximum power dissipation	Peak	250m	100	250m	20.2422m	9
	R4	Maximum power dissipation	Peak	250m	100	250m	20.2422m	9
	D3	Max forward current	Peak	100m	100	100m	8.3989m	9
	R3	Maximum power dissipation	Peak	250m	100	250m	20.2422m	9
	D2	Maximum power dissipation	RMS	296m	100	296m	23.8716m	9
	R10	Maximum power dissipation	Peak	250m	100	250m	20.2422m	9

Smoke - transient ndi.sim [No Derating] Component Filter = [*]

♦	Component	Parameter	Type	Rated Value	% Derating	Max Derating	Measured Value	% Max
	D1	Maximum power dissipation	RMS	296m	100	296m	23.8703m	9
	V6	Maximum power dissipation	Average	62.5000m	100	62.5000m	5.3298m	9
	R9	Maximum power dissipation	Peak	250m	100	250m	20.2422m	9
	R2	Maximum voltage	Average	200	100	200	14.0625	8
	K1	NPN max Ic	RMS	50m	100	50m	3.5632m	8
	D2	Max Reverse Current	Peak	113.6360m	100	113.6360m	8.3985m	8
	D1	Max Reverse Current	Peak	113.6360m	100	113.6360m	8.3989m	8
	R1	Maximum voltage	Average	200	100	200	14.0625	8
	C2	Maximum voltage	Peak	50	100	50	3.1696	7
	K1	LED max If	RMS	80m	100	80m	5.4090m	7
	R8	Maximum power dissipation	RMS	250m	100	250m	12.7921m	6
	R7	Maximum power dissipation	RMS	250m	100	250m	12.7921m	6
	R6	Maximum power dissipation	RMS	250m	100	250m	12.7921m	6
	K1	Maximum power dissipation	Peak	210m	100	210m	10.5412m	6
	R5	Maximum power dissipation	RMS	250m	100	250m	12.7921m	6
	R4	Maximum power dissipation	RMS	250m	100	250m	12.7921m	6
	D3	Max forward current	RMS	100m	100	100m	5.4099m	6
	R3	Maximum power dissipation	RMS	250m	100	250m	12.7921m	6
	D2	Maximum power dissipation	Average	296m	100	296m	16.1485m	6
	R10	Maximum power dissipation	RMS	250m	100	250m	12.7921m	6
	D1	Maximum power dissipation	Average	296m	100	296m	16.1477m	6
	R9	Maximum power dissipation	RMS	250m	100	250m	12.7921m	6
	C2	Maximum voltage	RMS	50	100	50	2.1786	5
	K1	NPN max Ic	Average	50m	100	50m	2.4816m	5
	K1	LED max If	Average	80m	100	80m	3.6599m	5
	K1	NPN max C-E vol	Peak	80	100	80	3.3000	5
	D2	Max Reverse Current	RMS	113.6360m	100	113.6360m	5.4099m	5
	D1	Max Reverse Current	RMS	113.6360m	100	113.6360m	5.4096m	5
	R11	Maximum power dissipation	Peak	100m	100	100m	4.2578m	5
	C2	Maximum voltage	Average	50	100	50	1.5347	4
	R8	Maximum power dissipation	Average	250m	100	250m	8.4143m	4
	R7	Maximum power dissipation	Average	250m	100	250m	8.4143m	4
	R6	Maximum power dissipation	Average	250m	100	250m	8.4143m	4
	K1	Maximum power dissipation	RMS	210m	100	210m	6.7278m	4
	R5	Maximum power dissipation	Average	250m	100	250m	8.4143m	4
	R13	Maximum voltage	Peak	50	100	50	1.7433	4
	R4	Maximum power dissipation	Average	250m	100	250m	8.4143m	4
	D3	Max forward current	Average	100m	100	100m	3.6605m	4
	R3	Maximum power dissipation	Average	250m	100	250m	8.4143m	4
	D2	Max Reverse Current	Average	113.6360m	100	113.6360m	3.6605m	4
	R10	Maximum power dissipation	Average	250m	100	250m	8.4143m	4
	D1	Max Reverse Current	Average	113.6360m	100	113.6360m	3.6603m	4
	V6	Max forward current	Peak	140m	100	140m	4.8673m	4
	R9	Maximum power dissipation	Average	250m	100	250m	8.4143m	4

Smoke - transient ndi.sim [No Derating] Component Filter = [*]

♦	Component	Parameter	Type	Rated Value	% Derating	Max Derating	Measured Value	% Max
	R8	Maximum voltage	Peak	200	100	200	4.8248	3
	R7	Maximum voltage	Peak	200	100	200	4.8248	3
	R6	Maximum voltage	Peak	200	100	200	4.8248	3
	K1	Maximum power dissipation	Average	210m	100	210m	4.5886m	3
	K1	NPN max C-E vol	Average	80	100	80	1.7455	3
	K1	NPN max C-E vol	RMS	80	100	80	2.3450	3
	R5	Maximum voltage	Peak	200	100	200	4.8248	3
	R4	Maximum voltage	Peak	200	100	200	4.8248	3
	R3	Maximum voltage	Peak	200	100	200	4.8248	3
	D2	Max Forward Current	RMS	250m	100	250m	5.4099m	3
	R10	Maximum voltage	Peak	200	100	200	4.8248	3
	D1	Max Forward Current	RMS	250m	100	250m	5.4096m	3
	R11	Maximum power dissipation	Average	100m	100	100m	2.0118m	3
	R11	Maximum power dissipation	RMS	100m	100	100m	2.9088m	3
	V6	Max forward current	RMS	140m	100	140m	3.3431m	3
	R9	Maximum voltage	Peak	200	100	200	4.8248	3
	R8	Maximum voltage	Average	200	100	200	2.1048	2
	R8	Maximum voltage	RMS	200	100	200	3.1107	2
	R7	Maximum voltage	Average	200	100	200	2.1048	2
	R7	Maximum voltage	RMS	200	100	200	3.1107	2
	R6	Maximum voltage	Average	200	100	200	2.1048	2
	R6	Maximum voltage	RMS	200	100	200	3.1107	2
	R5	Maximum voltage	Average	200	100	200	2.1048	2
	R5	Maximum voltage	RMS	200	100	200	3.1107	2
	R4	Maximum voltage	Average	200	100	200	2.1048	2
	R4	Maximum voltage	RMS	200	100	200	3.1107	2
	D3	Maximum power dissipation	Peak	500m	100	500m	5.9872m	2
	R3	Maximum voltage	Average	200	100	200	2.1048	2
	R3	Maximum voltage	RMS	200	100	200	3.1107	2
	R12	Maximum power dissipation	Peak	100m	100	100m	1.0046m	2
	R10	Maximum voltage	Average	200	100	200	2.1048	2
	R10	Maximum voltage	RMS	200	100	200	3.1107	2
	R11	Maximum voltage	Peak	50	100	50	875.4430m	2
	R11	Maximum voltage	RMS	50	100	50	601.7705m	2
	V6	Max forward current	Average	140m	100	140m	2.3259m	2
	R9	Maximum voltage	Average	200	100	200	2.1048	2
	R9	Maximum voltage	RMS	200	100	200	3.1107	2
	C2	Maximum current	Average	1	100	1	198.0943n	1
	C2	Maximum current	Peak	1	100	1	17.4265u	1
	C2	Maximum current	RMS	1	100	1	2.4373u	1
	V5	Max Forward Current	Average	100	100	100	5.8448u	1
	V5	Max Forward Current	Peak	100	100	100	12.8661u	1
	V5	Max Forward Current	RMS	100	100	100	7.8069u	1
	V5	Maximum power dissipation	Average	515	100	515	145.8756u	1

Smoke - transient ndi.sim [No Derating] Component Filter = [*]

♦	Component	Parameter	Type	Rated Value	% Derating	Max Derating	Measured Value	% Max
	V5	Maximum power dissipation	Peak	515	100	515	328.2039u	1
	V5	Maximum power dissipation	RMS	515	100	515	205.7678u	1
	C1	Maximum current	Average	1	100	1	187.5267n	1
	C1	Maximum current	Peak	1	100	1	3.0744u	1
	C1	Maximum current	RMS	1	100	1	1.2990u	1
	K1	LED max rev voltage	Peak	6	100	6	6.4018p	1
	R13	Maximum power dissipation	Average	100m	100	100m	594.4658n	1
	R13	Maximum power dissipation	Peak	100m	100	100m	30.3897u	1
	R13	Maximum power dissipation	RMS	100m	100	100m	3.1375u	1
	R13	Maximum voltage	Average	50	100	50	19.8162m	1
	R13	Maximum voltage	RMS	50	100	50	243.8167m	1
	D3	Maximum power dissipation	Average	500m	100	500m	2.5955m	1
	D3	Maximum power dissipation	RMS	500m	100	500m	3.8471m	1
	D3	Peak reverse voltage	Peak	100	100	100	554.5163m	1
	D3	Peak reverse voltage	RMS	100	100	100	503.4882m	1
	D2	Max Forward Current	Peak	250m	100	250m	13.7202n	1
	R12	Maximum power dissipation	Average	100m	100	100m	486.8495u	1
	R12	Maximum power dissipation	RMS	100m	100	100m	694.6535u	1
	D1	Max Forward Current	Peak	250m	100	250m	13.7202n	1
	R11	Maximum voltage	Average	50	100	50	418.6646m	1
	V5	Max Reverse Current	Average	1u	100	1u	-5.8448u	0
	K1	NPN max E-C vol	Average	7	100	7	-1.7455	0
	K1	NPN max E-C vol	Peak	7	100	7	-130.3905m	0
	K1	LED max rev voltage	Average	6	100	6	-632.4665m	0
	D3	Peak reverse voltage	Average	100	100	100	-351.4145m	0
	D2	Max Forward Current	Average	250m	100	250m	-3.6605m	0
	D1	Max Forward Current	Average	250m	100	250m	-3.6603m	0
	V6	Max reverse voltage	Average	5	100	5	-1.1358	0
	V6	Max reverse voltage	Peak	5	100	5	-36.4972u	0

With De-rated factors

Smoke - transient ndi.sim [Derating File: DeRating.drt] Component Filter = [*]

♦	Component	Parameter	Type	Rated Value	% Derating	Max Derating	Measured Value	% Max
	V5	Max Reverse Current	RMS	1u	100	1u	7.8069u	781
	V5	Max Reverse Current	Peak	1u	100	1u	1.5869u	159
	C1	Maximum voltage	Peak	50	80	40	30	75
	R2	Maximum breakdown temperature	Peak	155	80	124	92.4545	75
	R1	Maximum breakdown temperature	Peak	155	80	124	92.4545	75
	R2	Maximum power dissipation	Peak	250m	50	125m	81.8182m	66
	R1	Maximum power dissipation	Peak	250m	50	125m	81.8182m	66
	R2	Maximum breakdown temperature	RMS	155	80	124	69.0389	56
	R1	Maximum breakdown temperature	RMS	155	80	124	69.0389	56
	C1	Maximum voltage	RMS	50	80	40	19.8431	50
	V6	Maximum junction temperature	Average	85	69	59.5000	27	46
	V6	Maximum junction temperature	Peak	85	69	59.5000	27	46
	V6	Maximum junction temperature	RMS	85	69	59.5000	27	46
	R2	Maximum breakdown temperature	Average	155	80	124	55.6364	45
	R1	Maximum breakdown temperature	Average	155	80	124	55.6364	45
	R2	Maximum power dissipation	RMS	250m	50	125m	52.5487m	43
	R1	Maximum power dissipation	RMS	250m	50	125m	52.5487m	43
	V6	Max reverse voltage	RMS	5	75	3.7500	1.6086	43
	D2	Maximum junction temperature	Peak	175	69	122.5000	45.5330	38
	D1	Maximum junction temperature	Peak	175	69	122.5000	45.5338	38
	C1	Maximum voltage	Average	50	80	40	14.0625	36
	R8	Maximum breakdown temperature	Peak	155	80	124	43.1937	35
	R7	Maximum breakdown temperature	Peak	155	80	124	43.1937	35
	R6	Maximum breakdown temperature	Peak	155	80	124	43.1937	35
	R5	Maximum breakdown temperature	Peak	155	80	124	43.1937	35
	R4	Maximum breakdown temperature	Peak	155	80	124	43.1937	35
	R3	Maximum breakdown temperature	Peak	155	80	124	43.1937	35
	R10	Maximum breakdown temperature	Peak	155	80	124	43.1937	35
	R9	Maximum breakdown temperature	Peak	155	80	124	43.1937	35
	K1	NPN max E-C vol	RMS	7	100	7	2.3450	34
	D2	Maximum junction temperature	RMS	175	69	122.5000	38.9358	32
	D1	Maximum junction temperature	RMS	175	69	122.5000	38.9351	32
	R8	Maximum breakdown temperature	RMS	155	80	124	37.2337	31
	R7	Maximum breakdown temperature	RMS	155	80	124	37.2337	31
	R6	Maximum breakdown temperature	RMS	155	80	124	37.2337	31
	R5	Maximum breakdown temperature	RMS	155	80	124	37.2337	31
	R4	Maximum breakdown temperature	RMS	155	80	124	37.2337	31
	R3	Maximum breakdown temperature	RMS	155	80	124	37.2337	31
	R10	Maximum breakdown temperature	RMS	155	80	124	37.2337	31
	R9	Maximum breakdown temperature	RMS	155	80	124	37.2337	31
	R2	Maximum power dissipation	Average	250m	50	125m	35.7955m	29

Smoke - transient ndi.sim [Derating File: DeRating.drt] Component Filter = [*]

♦	Component	Parameter	Type	Rated Value	% Derating	Max Derating	Measured Value	% Max
	D2	Maximum junction temperature	Average	175	69	122.5000	35.0743	29
	D1	Maximum junction temperature	Average	175	69	122.5000	35.0738	29
	R1	Maximum power dissipation	Average	250m	50	125m	35.7955m	29
	R11	Maximum breakdown temperature	Peak	155	80	124	35.5156	29
	R8	Maximum breakdown temperature	Average	155	80	124	33.7314	28
	R7	Maximum breakdown temperature	Average	155	80	124	33.7314	28
	R6	Maximum breakdown temperature	Average	155	80	124	33.7314	28
	R5	Maximum breakdown temperature	Average	155	80	124	33.7314	28
	R4	Maximum breakdown temperature	Average	155	80	124	33.7314	28
	R3	Maximum breakdown temperature	Average	155	80	124	33.7314	28
	R10	Maximum breakdown temperature	Average	155	80	124	33.7314	28
	V6	Maximum power dissipation	Peak	62.5000m	65	40.6250m	11.1663m	28
	R9	Maximum breakdown temperature	Average	155	80	124	33.7314	28
	R11	Maximum breakdown temperature	RMS	155	80	124	32.8176	27
	V5	Maximum junction temperature	Average	150	70	105	27	26
	V5	Maximum junction temperature	Peak	150	70	105	27	26
	V5	Maximum junction temperature	RMS	150	70	105	27	26
	R11	Maximum breakdown temperature	Average	155	80	124	31.0236	26
	R12	Maximum breakdown temperature	Peak	155	80	124	29.0093	24
	R12	Maximum breakdown temperature	Average	155	80	124	27.9737	23
	R12	Maximum breakdown temperature	RMS	155	80	124	28.3893	23
	R13	Maximum breakdown temperature	Average	155	80	124	27.0012	22
	R13	Maximum breakdown temperature	Peak	155	80	124	27.0608	22
	R13	Maximum breakdown temperature	RMS	155	80	124	27.0063	22
	K1	LED max If	Peak	80m	50	40m	8.3986m	21
	D3	Maximum junction temperature	Average	200	70	140	27	20
	D3	Maximum junction temperature	Peak	200	70	140	27	20
	D3	Maximum junction temperature	RMS	200	70	140	27	20
	D2	Maximum power dissipation	Peak	296m	64	191m	37.0660m	20
	D1	Maximum power dissipation	Peak	296m	64	191m	37.0676m	20
	R2	Maximum voltage	Peak	200	80	160	30	19
	K1	LED max rev voltage	RMS	6	75	4.5000	836.0862m	19
	R1	Maximum voltage	Peak	200	80	160	30	19
	V6	Maximum power dissipation	RMS	62.5000m	65	40.6250m	7.6653m	19
	R8	Maximum power dissipation	Peak	250m	50	125m	20.2422m	17
	R7	Maximum power dissipation	Peak	250m	50	125m	20.2422m	17
	R6	Maximum power dissipation	Peak	250m	50	125m	20.2422m	17
	R5	Maximum power dissipation	Peak	250m	50	125m	20.2422m	17
	R4	Maximum power dissipation	Peak	250m	50	125m	20.2422m	17
	D3	Max forward current	Peak	100m	50	50m	8.3989m	17
	R3	Maximum power dissipation	Peak	250m	50	125m	20.2422m	17
	R10	Maximum power dissipation	Peak	250m	50	125m	20.2422m	17

Smoke - transient ndi.sim [Derating File: DeRating.drt] Component Filter = [*]

♦	Component	Parameter	Type	Rated Value	% Derating	Max Derating	Measured Value	% Max
	R9	Maximum power dissipation	Peak	250m	50	125m	20.2422m	17
	K1	LED max If	RMS	80m	50	40m	5.4090m	14
	V6	Maximum power dissipation	Average	62.5000m	65	40.6250m	5.3298m	14
	R2	Maximum voltage	RMS	200	80	160	19.8431	13
	K1	NPN max Ic	Peak	50m	80	40m	5.1840m	13
	D2	Maximum power dissipation	RMS	296m	64	191m	23.8716m	13
	D1	Maximum power dissipation	RMS	296m	64	191m	23.8703m	13
	R1	Maximum voltage	RMS	200	80	160	19.8431	13
	R8	Maximum power dissipation	RMS	250m	50	125m	12.7921m	11
	R7	Maximum power dissipation	RMS	250m	50	125m	12.7921m	11
	R6	Maximum power dissipation	RMS	250m	50	125m	12.7921m	11
	R5	Maximum power dissipation	RMS	250m	50	125m	12.7921m	11
	R4	Maximum power dissipation	RMS	250m	50	125m	12.7921m	11
	D3	Max forward current	RMS	100m	50	50m	5.4099m	11
	R3	Maximum power dissipation	RMS	250m	50	125m	12.7921m	11
	R10	Maximum power dissipation	RMS	250m	50	125m	12.7921m	11
	R9	Maximum power dissipation	RMS	250m	50	125m	12.7921m	11
	K1	LED max If	Average	80m	50	40m	3.6599m	10
	R2	Maximum voltage	Average	200	80	160	14.0625	9
	K1	NPN max Ic	RMS	50m	80	40m	3.5632m	9
	D2	Maximum power dissipation	Average	296m	64	191m	16.1485m	9
	D1	Maximum power dissipation	Average	296m	64	191m	16.1477m	9
	R1	Maximum voltage	Average	200	80	160	14.0625	9
	R11	Maximum power dissipation	Peak	100m	50	50m	4.2578m	9
	C2	Maximum voltage	Peak	50	80	40	3.1696	8
	D3	Max forward current	Average	100m	50	50m	3.6605m	8
	D2	Max Reverse Current	Peak	113.6360m	100	113.6360m	8.3985m	8
	D1	Max Reverse Current	Peak	113.6360m	100	113.6360m	8.3989m	8
	R8	Maximum power dissipation	Average	250m	50	125m	8.4143m	7
	R7	Maximum power dissipation	Average	250m	50	125m	8.4143m	7
	R6	Maximum power dissipation	Average	250m	50	125m	8.4143m	7
	K1	NPN max Ic	Average	50m	80	40m	2.4816m	7
	R5	Maximum power dissipation	Average	250m	50	125m	8.4143m	7
	R4	Maximum power dissipation	Average	250m	50	125m	8.4143m	7
	R3	Maximum power dissipation	Average	250m	50	125m	8.4143m	7
	R10	Maximum power dissipation	Average	250m	50	125m	8.4143m	7
	V6	Max forward current	Peak	140m	50	70m	4.8673m	7
	R9	Maximum power dissipation	Average	250m	50	125m	8.4143m	7
	C2	Maximum voltage	RMS	50	80	40	2.1786	6
	K1	Maximum power dissipation	Peak	210m	100	210m	10.5412m	6
	K1	NPN max C-E vol	Peak	80	75	60	3.3000	6
	R11	Maximum power dissipation	RMS	100m	50	50m	2.9088m	6

Smoke - transient ndi.sim [Derating File: DeRating.drt] Component Filter = [*]

♦	Component	Parameter	Type	Rated Value	% Derating	Max Derating	Measured Value	% Max
	R13	Maximum voltage	Peak	50	80	40	1.7433	5
	D2	Max Reverse Current	RMS	113.6360m	100	113.6360m	5.4099m	5
	D1	Max Reverse Current	RMS	113.6360m	100	113.6360m	5.4096m	5
	R11	Maximum power dissipation	Average	100m	50	50m	2.0118m	5
	V6	Max forward current	RMS	140m	50	70m	3.3431m	5
	C2	Maximum voltage	Average	50	80	40	1.5347	4
	R8	Maximum voltage	Peak	200	80	160	4.8248	4
	R7	Maximum voltage	Peak	200	80	160	4.8248	4
	R6	Maximum voltage	Peak	200	80	160	4.8248	4
	K1	Maximum power dissipation	RMS	210m	100	210m	6.7278m	4
	K1	NPN max C-E vol	RMS	80	75	60	2.3450	4
	R5	Maximum voltage	Peak	200	80	160	4.8248	4
	R4	Maximum voltage	Peak	200	80	160	4.8248	4
	R3	Maximum voltage	Peak	200	80	160	4.8248	4
	D2	Max Reverse Current	Average	113.6360m	100	113.6360m	3.6605m	4
	R10	Maximum voltage	Peak	200	80	160	4.8248	4
	D1	Max Reverse Current	Average	113.6360m	100	113.6360m	3.6603m	4
	V6	Max forward current	Average	140m	50	70m	2.3259m	4
	R9	Maximum voltage	Peak	200	80	160	4.8248	4
	K1	Maximum power dissipation	Average	210m	100	210m	4.5886m	3
	K1	NPN max C-E vol	Average	80	75	60	1.7455	3
	D3	Maximum power dissipation	Peak	500m	50	250m	5.9872m	3
	D2	Max Forward Current	RMS	250m	100	250m	5.4099m	3
	R12	Maximum power dissipation	Peak	100m	50	50m	1.0046m	3
	D1	Max Forward Current	RMS	250m	100	250m	5.4096m	3
	R11	Maximum voltage	Peak	50	80	40	875.4430m	3
	R8	Maximum voltage	Average	200	80	160	2.1048	2
	R8	Maximum voltage	RMS	200	80	160	3.1107	2
	R7	Maximum voltage	Average	200	80	160	2.1048	2
	R7	Maximum voltage	RMS	200	80	160	3.1107	2
	R6	Maximum voltage	Average	200	80	160	2.1048	2
	R6	Maximum voltage	RMS	200	80	160	3.1107	2
	R5	Maximum voltage	Average	200	80	160	2.1048	2
	R5	Maximum voltage	RMS	200	80	160	3.1107	2
	R4	Maximum voltage	Average	200	80	160	2.1048	2
	R4	Maximum voltage	RMS	200	80	160	3.1107	2
	D3	Maximum power dissipation	Average	500m	50	250m	2.5955m	2
	D3	Maximum power dissipation	RMS	500m	50	250m	3.8471m	2
	R3	Maximum voltage	Average	200	80	160	2.1048	2
	R3	Maximum voltage	RMS	200	80	160	3.1107	2
	R12	Maximum power dissipation	RMS	100m	50	50m	694.6535u	2
	R10	Maximum voltage	Average	200	80	160	2.1048	2

Smoke - transient ndi.sim [Derating File: DeRating.drt] Component Filter = [*]

♦	Component	Parameter	Type	Rated Value	% Derating	Max Derating	Measured Value	% Max
	R10	Maximum voltage	RMS	200	80	160	3.1107	2
	R11	Maximum voltage	Average	50	80	40	418.6646m	2
	R11	Maximum voltage	RMS	50	80	40	601.7705m	2
	R9	Maximum voltage	Average	200	80	160	2.1048	2
	R9	Maximum voltage	RMS	200	80	160	3.1107	2
	C2	Maximum current	Average	1	100	1	198.0943n	1
	C2	Maximum current	Peak	1	100	1	17.4265u	1
	C2	Maximum current	RMS	1	100	1	2.4373u	1
	V5	Max Forward Current	Average	100	100	100	5.8448u	1
	V5	Max Forward Current	Peak	100	100	100	12.8661u	1
	V5	Max Forward Current	RMS	100	100	100	7.8069u	1
	V5	Maximum power dissipation	Average	515	65	334.7500	145.8756u	1
	V5	Maximum power dissipation	Peak	515	65	334.7500	328.2039u	1
	V5	Maximum power dissipation	RMS	515	65	334.7500	205.7678u	1
	C1	Maximum current	Average	1	100	1	187.5267n	1
	C1	Maximum current	Peak	1	100	1	3.0744u	1
	C1	Maximum current	RMS	1	100	1	1.2990u	1
	K1	LED max rev voltage	Peak	6	75	4.5000	6.4018p	1
	R13	Maximum power dissipation	Average	100m	50	50m	594.4658n	1
	R13	Maximum power dissipation	Peak	100m	50	50m	30.3897u	1
	R13	Maximum power dissipation	RMS	100m	50	50m	3.1375u	1
	R13	Maximum voltage	Average	50	80	40	19.8162m	1
	R13	Maximum voltage	RMS	50	80	40	243.8167m	1
	D3	Peak reverse voltage	Peak	100	75	75	554.5163m	1
	D3	Peak reverse voltage	RMS	100	75	75	503.4882m	1
	D2	Max Forward Current	Peak	250m	100	250m	13.7202n	1
	R12	Maximum power dissipation	Average	100m	50	50m	486.8495u	1
	D1	Max Forward Current	Peak	250m	100	250m	13.7202n	1
	V5	Max Reverse Current	Average	1u	100	1u	-5.8448u	0
	K1	NPN max E-C vol	Average	7	100	7	-1.7455	0
	K1	NPN max E-C vol	Peak	7	100	7	-130.3905m	0
	K1	LED max rev voltage	Average	6	75	4.5000	-632.4665m	0
	D3	Peak reverse voltage	Average	100	75	75	-351.4145m	0
	D2	Max Forward Current	Average	250m	100	250m	-3.6605m	0
	D1	Max Forward Current	Average	250m	100	250m	-3.6603m	0
	V6	Max reverse voltage	Average	5	75	3.7500	-1.1358	0
	V6	Max reverse voltage	Peak	5	75	3.7500	-36.4972u	0

Appendix B

Figures of DI TB0107

B.1 Voltage Variation for DI TB0107: 16.8V, 24V, 30V

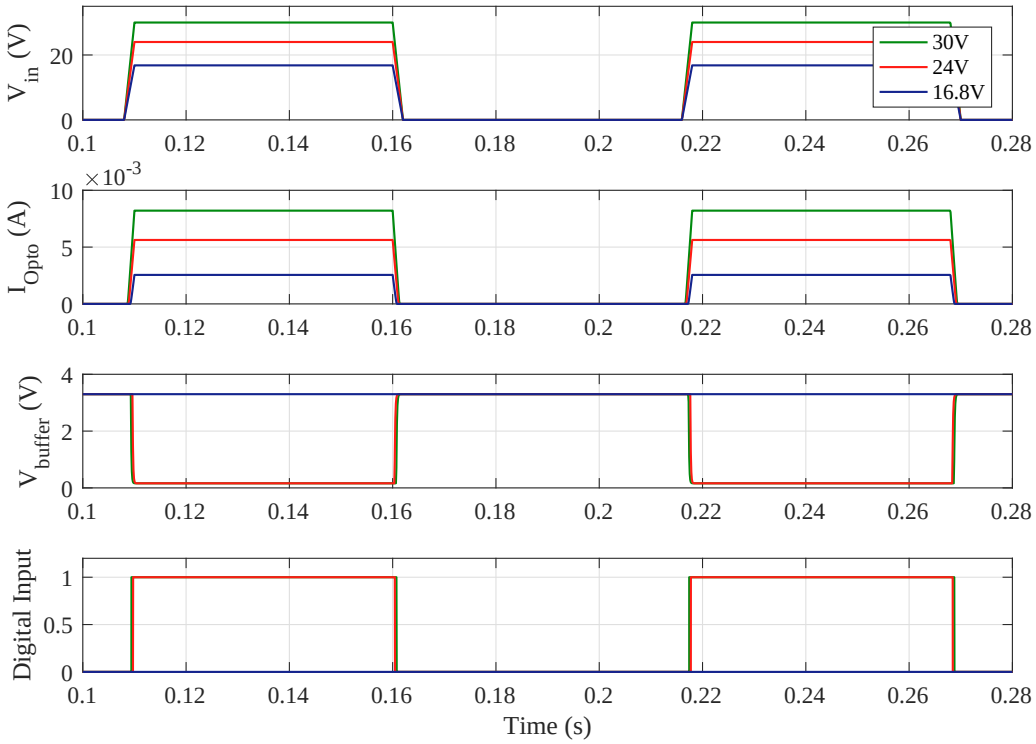


Figure B-1: Transient simulation of the DI of TB0107 for 16.8V, 24V and 30V: (a) Input voltage. (b) Current flowing through the optocoupler's LED. (c) Voltage at the ouput of the ouptocoupler and the voltage resultant after applying a RC filter. (d) Digital output DI.

B.2 Frequency variation for DI TB0107

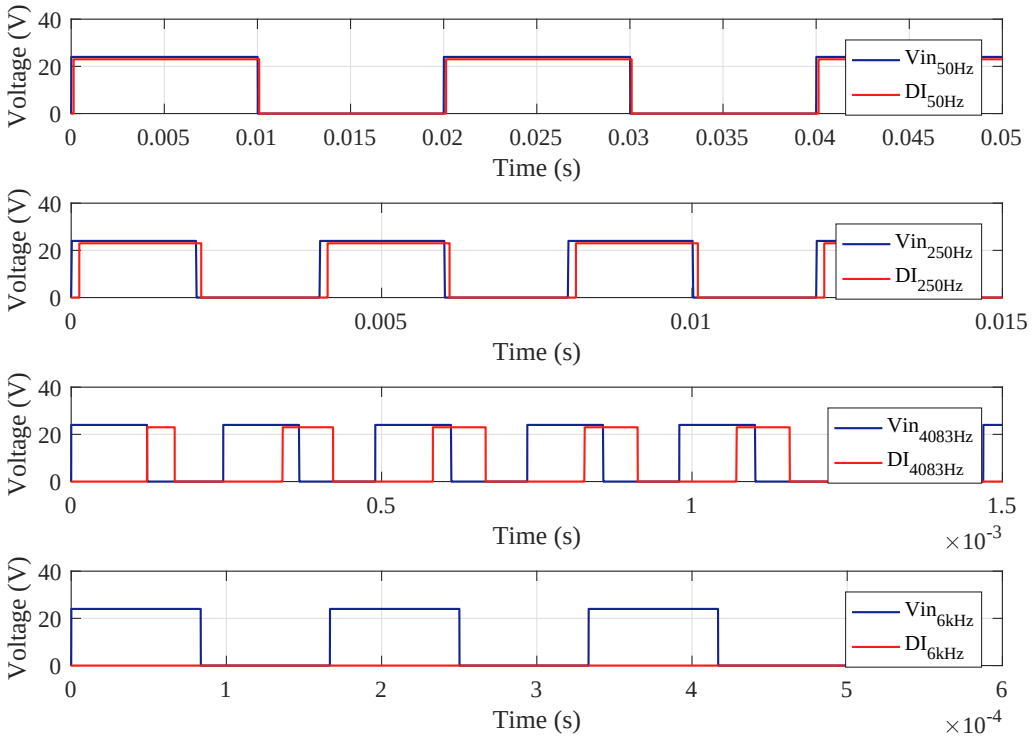


Figure B-2: Frequency variation for DI TB0107: (a) 50Hz. (b) 250Hz. (c) 4083Hz. (d) 6000Hz.

B.3 Surge Test for DI TB0107

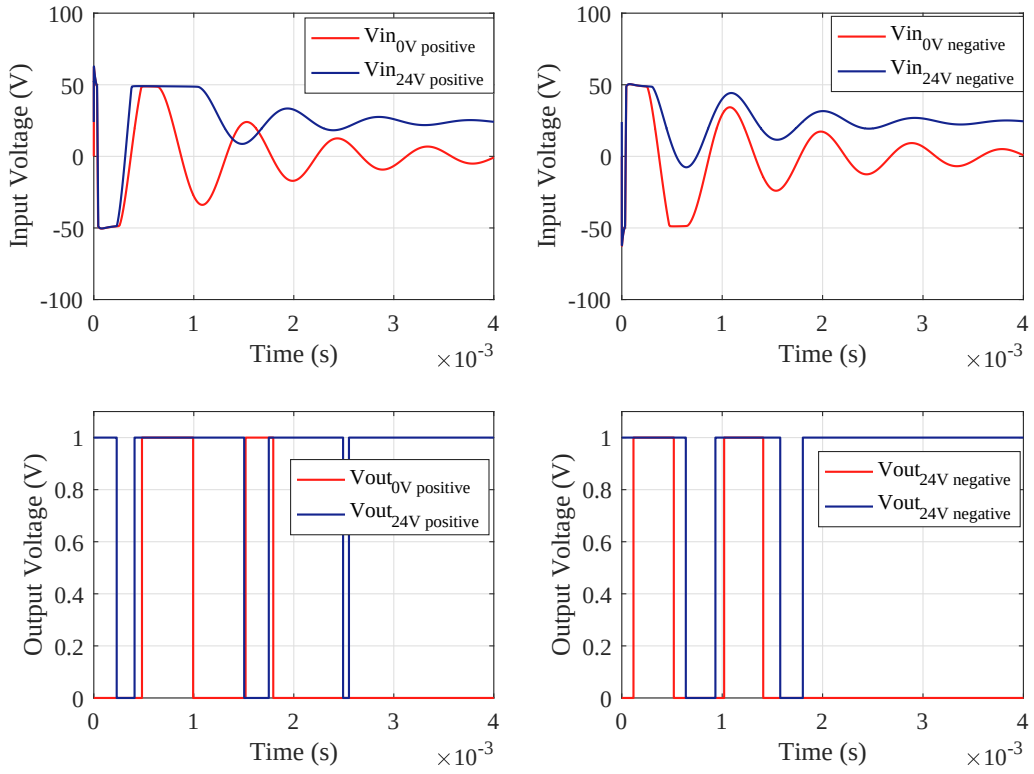


Figure B-3: Surge Test for the DI TB0107: (a) Input voltage at the PCC with a positive surge (b) DI response to a positive surge. (c) Input voltage at the PCC with a negative surge. (d) DI response to a negative surge.

B.4 Smoke Analysis for DI TB0107

Smoke - transient di.sim [Derating File: DeRating.drt] Component Filter = [*]

♦	Component	Parameter	Type	Rated Value	% Derating	Max Derating	Measured Value	% Max
	V6	Max Reverse Current	RMS	1u	100	1u	7.8073u	781
	V6	Max Reverse Current	Peak	1u	100	1u	1.5970u	160
	R2	Maximum breakdown temperature	Peak	155	80	124	92.4545	75
	R1	Maximum breakdown temperature	Peak	155	80	124	92.4545	75
	C1	Maximum voltage	Peak	50	80	40	30	75
	V7	Max reverse voltage	RMS	2.5000	75	1.8750	1.2682	68
	R2	Maximum power dissipation	Peak	250m	50	125m	81.8182m	66
	R1	Maximum power dissipation	Peak	250m	50	125m	81.8182m	66
	R2	Maximum breakdown temperature	RMS	155	80	124	69.0389	56
	R1	Maximum breakdown temperature	RMS	155	80	124	69.0389	56
	C1	Maximum voltage	RMS	50	80	40	19.8431	50
	V7	Maximum junction temperature	Average	85	69	59.5000	27	46
	V7	Maximum junction temperature	Peak	85	69	59.5000	27	46
	V7	Maximum junction temperature	RMS	85	69	59.5000	27	46
	R2	Maximum breakdown temperature	Average	155	80	124	55.6364	45
	R1	Maximum breakdown temperature	Average	155	80	124	55.6364	45
	R2	Maximum power dissipation	RMS	250m	50	125m	52.5487m	43
	R1	Maximum power dissipation	RMS	250m	50	125m	52.5487m	43
	D1	Maximum junction temperature	Peak	175	69	122.5000	45.1271	37
	D2	Maximum junction temperature	Peak	175	69	122.5000	45.1251	37
	R12	Maximum breakdown temperature	Peak	155	80	124	44.7355	37
	C1	Maximum voltage	Average	50	80	40	14.0625	36
	R7	Maximum breakdown temperature	Peak	155	80	124	42.4988	35
	R6	Maximum breakdown temperature	Peak	155	80	124	42.4988	35
	R4	Maximum breakdown temperature	Peak	155	80	124	42.4988	35
	R3	Maximum breakdown temperature	Peak	155	80	124	42.4988	35
	R8	Maximum breakdown temperature	Peak	155	80	124	42.4988	35
	R10	Maximum breakdown temperature	Peak	155	80	124	42.4988	35
	R9	Maximum breakdown temperature	Peak	155	80	124	42.4988	35
	R5	Maximum breakdown temperature	Peak	155	80	124	42.4988	35
	D1	Maximum junction temperature	RMS	175	69	122.5000	38.6636	32
	D2	Maximum junction temperature	RMS	175	69	122.5000	38.6634	32
	R12	Maximum breakdown temperature	RMS	155	80	124	38.1192	31
	R7	Maximum breakdown temperature	RMS	155	80	124	36.7883	30
	R6	Maximum breakdown temperature	RMS	155	80	124	36.7883	30
	R4	Maximum breakdown temperature	RMS	155	80	124	36.7883	30
	R3	Maximum breakdown temperature	RMS	155	80	124	36.7883	30
	R8	Maximum breakdown temperature	RMS	155	80	124	36.7883	30
	R10	Maximum breakdown temperature	RMS	155	80	124	36.7883	30
	R9	Maximum breakdown temperature	RMS	155	80	124	36.7883	30
	R5	Maximum breakdown temperature	RMS	155	80	124	36.7883	30
	R2	Maximum power dissipation	Average	250m	50	125m	35.7955m	29
	R1	Maximum power dissipation	Average	250m	50	125m	35.7955m	29

Smoke - transient di.sim [Derating File: DeRating.drt] Component Filter = [*]

♦	Component	Parameter	Type	Rated Value	% Derating	Max Derating	Measured Value	% Max
	D1	Maximum junction temperature	Average	175	69	122.5000	34.8756	29
	D2	Maximum junction temperature	Average	175	69	122.5000	34.8755	29
	R12	Maximum breakdown temperature	Average	155	80	124	34.3809	28
	R7	Maximum breakdown temperature	Average	155	80	124	33.4295	27
	R6	Maximum breakdown temperature	Average	155	80	124	33.4295	27
	R4	Maximum breakdown temperature	Average	155	80	124	33.4295	27
	R3	Maximum breakdown temperature	Average	155	80	124	33.4295	27
	R8	Maximum breakdown temperature	Average	155	80	124	33.4295	27
	R10	Maximum breakdown temperature	Average	155	80	124	33.4295	27
	R9	Maximum breakdown temperature	Average	155	80	124	33.4295	27
	R5	Maximum breakdown temperature	Average	155	80	124	33.4295	27
	V6	Maximum junction temperature	Average	150	70	105	27	26
	V6	Maximum junction temperature	Peak	150	70	105	27	26
	V6	Maximum junction temperature	RMS	150	70	105	27	26
	R13	Maximum breakdown temperature	Peak	155	80	124	29.0175	24
	R13	Maximum breakdown temperature	Average	155	80	124	27.8680	23
	R13	Maximum breakdown temperature	RMS	155	80	124	28.3076	23
	R11	Maximum breakdown temperature	Average	155	80	124	27.0002	22
	R11	Maximum breakdown temperature	Peak	155	80	124	27.2017	22
	R11	Maximum breakdown temperature	RMS	155	80	124	27.0041	22
	D3	Maximum junction temperature	Average	200	70	140	27	20
	D3	Maximum junction temperature	Peak	200	70	140	27	20
	D3	Maximum junction temperature	RMS	200	70	140	27	20
	V7	Maximum power dissipation	Peak	105m	65	68.2500m	13.4306m	20
	R2	Maximum voltage	Peak	200	80	160	30	19
	R1	Maximum voltage	Peak	200	80	160	30	19
	D1	Maximum power dissipation	Peak	296m	64	191m	36.2542m	19
	D2	Maximum power dissipation	Peak	296m	64	191m	36.2502m	19
	R12	Maximum power dissipation	Peak	100m	50	50m	8.8677m	18
	D3	Max forward current	Peak	100m	50	50m	8.2147m	17
	R7	Maximum power dissipation	Peak	250m	50	125m	19.3735m	16
	R6	Maximum power dissipation	Peak	250m	50	125m	19.3735m	16
	R4	Maximum power dissipation	Peak	250m	50	125m	19.3735m	16
	R3	Maximum power dissipation	Peak	250m	50	125m	19.3735m	16
	R8	Maximum power dissipation	Peak	250m	50	125m	19.3735m	16
	R10	Maximum power dissipation	Peak	250m	50	125m	19.3735m	16
	R9	Maximum power dissipation	Peak	250m	50	125m	19.3735m	16
	R5	Maximum power dissipation	Peak	250m	50	125m	19.3735m	16
	R2	Maximum voltage	RMS	200	80	160	19.8431	13
	R1	Maximum voltage	RMS	200	80	160	19.8431	13
	D1	Maximum power dissipation	RMS	296m	64	191m	23.3272m	13
	D2	Maximum power dissipation	RMS	296m	64	191m	23.3269m	13
	V7	Maximum power dissipation	RMS	105m	65	68.2500m	8.6451m	13
	R12	Maximum power dissipation	RMS	100m	50	50m	5.5596m	12

Smoke - transient di.sim [Derating File: DeRating.drt] Component Filter = [*]

♦	Component	Parameter	Type	Rated Value	% Derating	Max Derating	Measured Value	% Max
	D3	Max forward current	RMS	100m	50	50m	5.2872m	11
	R7	Maximum power dissipation	RMS	250m	50	125m	12.2354m	10
	R6	Maximum power dissipation	RMS	250m	50	125m	12.2354m	10
	R4	Maximum power dissipation	RMS	250m	50	125m	12.2354m	10
	R3	Maximum power dissipation	RMS	250m	50	125m	12.2354m	10
	R8	Maximum power dissipation	RMS	250m	50	125m	12.2354m	10
	R10	Maximum power dissipation	RMS	250m	50	125m	12.2354m	10
	R9	Maximum power dissipation	RMS	250m	50	125m	12.2354m	10
	R5	Maximum power dissipation	RMS	250m	50	125m	12.2354m	10
	R2	Maximum voltage	Average	200	80	160	14.0625	9
	R1	Maximum voltage	Average	200	80	160	14.0625	9
	D1	Maximum power dissipation	Average	296m	64	191m	15.7512m	9
	D2	Maximum power dissipation	Average	296m	64	191m	15.7510m	9
	C2	Maximum voltage	Peak	50	80	40	3.3000	9
	V7	Max forward current	Peak	160m	50	80m	7.0220m	9
	V7	Maximum power dissipation	Average	105m	65	68.2500m	5.7386m	9
	D1	Max Reverse Current	Peak	113.6360m	100	113.6360m	8.2156m	8
	D2	Max Reverse Current	Peak	113.6360m	100	113.6360m	8.2147m	8
	D3	Max forward current	Average	100m	50	50m	3.5709m	8
	R11	Maximum voltage	Peak	50	80	40	3.1759	8
	R12	Maximum power dissipation	Average	100m	50	50m	3.6905m	8
	R7	Maximum power dissipation	Average	250m	50	125m	8.0369m	7
	R6	Maximum power dissipation	Average	250m	50	125m	8.0369m	7
	R4	Maximum power dissipation	Average	250m	50	125m	8.0369m	7
	R3	Maximum power dissipation	Average	250m	50	125m	8.0369m	7
	R8	Maximum power dissipation	Average	250m	50	125m	8.0369m	7
	R10	Maximum power dissipation	Average	250m	50	125m	8.0369m	7
	R9	Maximum power dissipation	Average	250m	50	125m	8.0369m	7
	R5	Maximum power dissipation	Average	250m	50	125m	8.0369m	7
	C2	Maximum voltage	RMS	50	80	40	2.4697	7
	V7	Max forward current	RMS	160m	50	80m	4.5249m	6
	D1	Max Reverse Current	RMS	113.6360m	100	113.6360m	5.2872m	5
	D2	Max Reverse Current	RMS	113.6360m	100	113.6360m	5.2872m	5
	C2	Maximum voltage	Average	50	80	40	1.9189	5
	D1	Max Reverse Current	Average	113.6360m	100	113.6360m	3.5709m	4
	D2	Max Reverse Current	Average	113.6360m	100	113.6360m	3.5709m	4
	R12	Maximum voltage	Peak	50	80	40	1.2634	4
	V7	Max forward current	Average	160m	50	80m	3.0036m	4
	R7	Maximum voltage	Peak	200	80	160	4.7201	3
	R6	Maximum voltage	Peak	200	80	160	4.7201	3
	R4	Maximum voltage	Peak	200	80	160	4.7201	3
	R3	Maximum voltage	Peak	200	80	160	4.7201	3
	R8	Maximum voltage	Peak	200	80	160	4.7201	3
	D1	Max Forward Current	RMS	250m	100	250m	5.2872m	3

Smoke - transient di.sim [Derating File: DeRating.drt] Component Filter = [*]

♦	Component	Parameter	Type	Rated Value	% Derating	Max Derating	Measured Value	% Max
	D2	Max Forward Current	RMS	250m	100	250m	5.2872m	3
	R10	Maximum voltage	Peak	200	80	160	4.7201	3
	D3	Maximum power dissipation	Peak	500m	50	250m	5.8458m	3
	R9	Maximum voltage	Peak	200	80	160	4.7201	3
	R5	Maximum voltage	Peak	200	80	160	4.7201	3
	R12	Maximum voltage	RMS	50	80	40	815.0354m	3
	R13	Maximum power dissipation	Peak	100m	50	50m	1.0087m	3
	R7	Maximum voltage	Average	200	80	160	2.0533	2
	R7	Maximum voltage	RMS	200	80	160	3.0401	2
	R6	Maximum voltage	Average	200	80	160	2.0533	2
	R6	Maximum voltage	RMS	200	80	160	3.0401	2
	R4	Maximum voltage	Average	200	80	160	2.0533	2
	R4	Maximum voltage	RMS	200	80	160	3.0401	2
	R3	Maximum voltage	Average	200	80	160	2.0533	2
	R3	Maximum voltage	RMS	200	80	160	3.0401	2
	R8	Maximum voltage	Average	200	80	160	2.0533	2
	R8	Maximum voltage	RMS	200	80	160	3.0401	2
	R10	Maximum voltage	Average	200	80	160	2.0533	2
	R10	Maximum voltage	RMS	200	80	160	3.0401	2
	D3	Maximum power dissipation	Average	500m	50	250m	2.5278m	2
	D3	Maximum power dissipation	RMS	500m	50	250m	3.7535m	2
	R9	Maximum voltage	Average	200	80	160	2.0533	2
	R9	Maximum voltage	RMS	200	80	160	3.0401	2
	R5	Maximum voltage	Average	200	80	160	2.0533	2
	R5	Maximum voltage	RMS	200	80	160	3.0401	2
	R12	Maximum voltage	Average	50	80	40	541.0179m	2
	R13	Maximum power dissipation	RMS	100m	50	50m	653.8039u	2
	V6	Max Forward Current	Average	100	100	100	5.8451u	1
	V6	Max Forward Current	Peak	100	100	100	12.8616u	1
	V6	Max Forward Current	RMS	100	100	100	7.8073u	1
	V6	Maximum power dissipation	Average	515	65	334.7500	145.8835u	1
	V6	Maximum power dissipation	Peak	515	65	334.7500	327.9965u	1
	V6	Maximum power dissipation	RMS	515	65	334.7500	205.7790u	1
	C1	Maximum current	Average	1	100	1	187.5260n	1
	C1	Maximum current	Peak	1	100	1	3.0509u	1
	C1	Maximum current	RMS	1	100	1	1.2990u	1
	D1	Max Forward Current	Peak	250m	100	250m	10.9289n	1
	D2	Max Forward Current	Peak	250m	100	250m	10.9288n	1
	D3	Peak reverse voltage	Peak	100	75	75	512.9762m	1
	D3	Peak reverse voltage	RMS	100	75	75	497.8059m	1
	R11	Maximum power dissipation	Average	100m	50	50m	89.8958n	1
	R11	Maximum power dissipation	Peak	100m	50	50m	100.8657u	1
	R11	Maximum power dissipation	RMS	100m	50	50m	2.0509u	1
	R11	Maximum voltage	Average	50	80	40	1.9668m	1

Smoke - transient di.sim [Derating File: DeRating.drt] Component Filter = [*]

♦	Component	Parameter	Type	Rated Value	% Derating	Max Derating	Measured Value	% Max
	R11	Maximum voltage	RMS	50	80	40	94.8134m	1
	C2	Maximum current	Average	1	100	1	19.5985n	1
	C2	Maximum current	Peak	1	100	1	31.6483u	1
	C2	Maximum current	RMS	1	100	1	944.8179n	1
	R13	Maximum power dissipation	Average	100m	50	50m	433.9960u	1
	V6	Max Reverse Current	Average	1u	100	1u	-5.8451u	0
	D1	Max Forward Current	Average	250m	100	250m	-3.5709m	0
	D2	Max Forward Current	Average	250m	100	250m	-3.5709m	0
	D3	Peak reverse voltage	Average	100	75	75	-359.8856m	0
	V7	Max reverse voltage	Average	2.5000	75	1.8750	-842.0356m	0
	V7	Max reverse voltage	Peak	2.5000	75	1.8750	-175.9181n	0

Appendix C

Figures of DO TB0107

C.1 Voltage Variation for DO TB0107: 16.8V, 24V, 30V

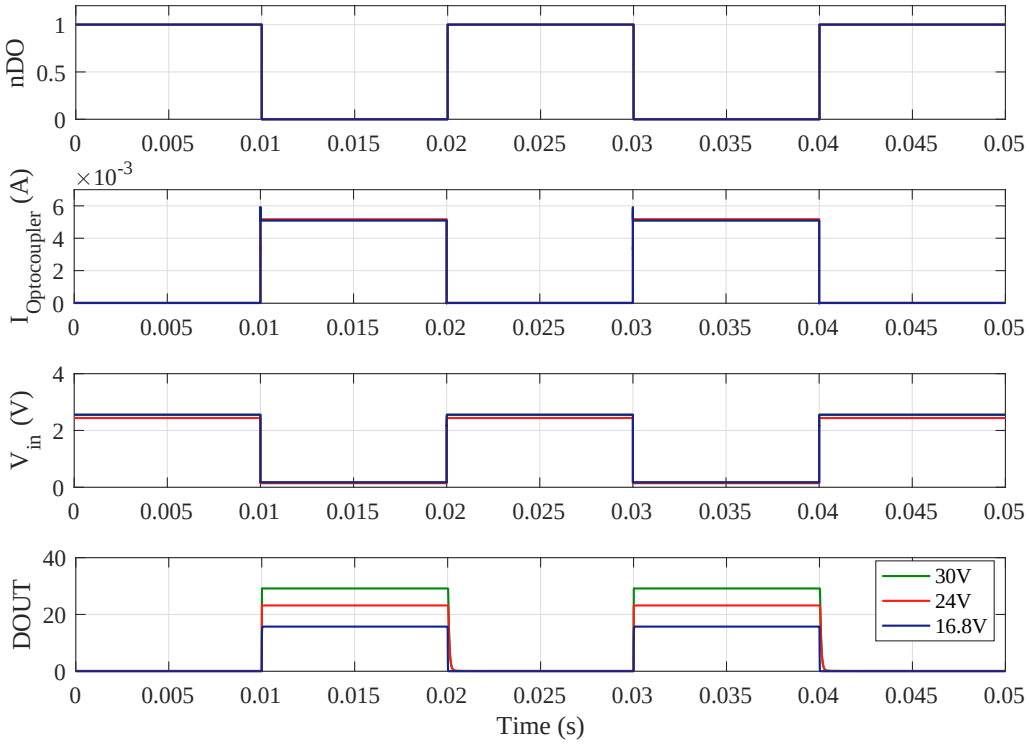


Figure C-1: Transient simulation of the DO of TB0107 for 16.8V, 24V and 30V: (a) Input digital signal nDO. (b) Current flowing through the optocoupler's LED. (c) Input Voltage of the DO. (d) Digital output DOUT.

C.2 Frequency variation for DO TB0107

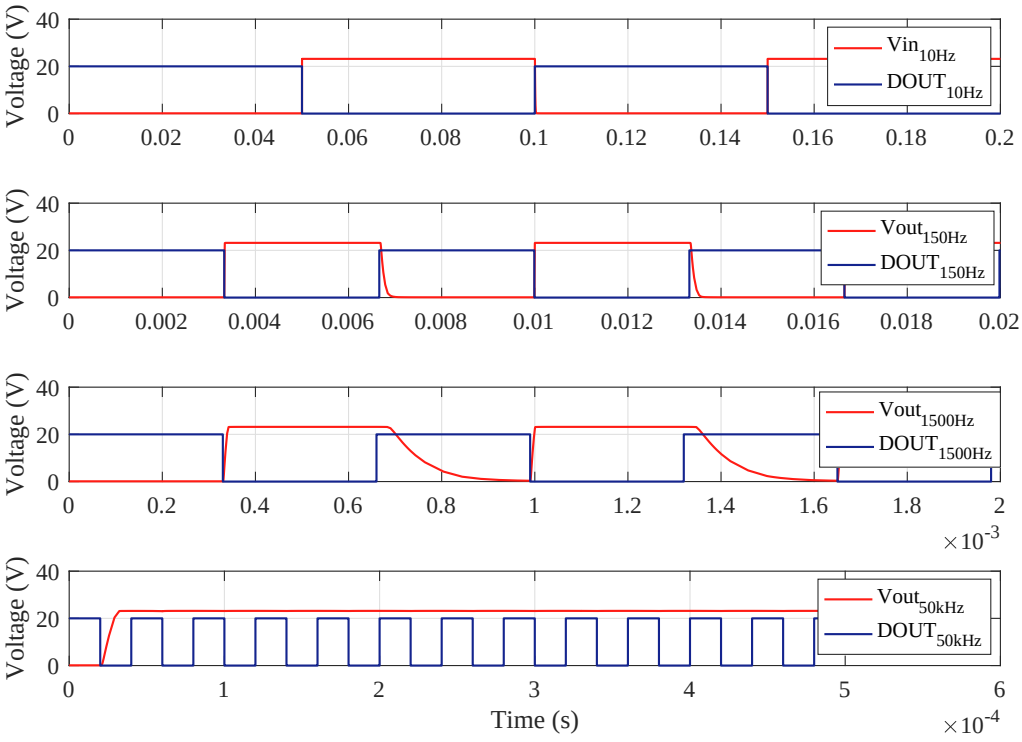


Figure C-2: Frequency variation for DI TB0107: (a) 10Hz. (b) 150Hz. (c) 1500Hz. (d) 50kHz.

C.3 Smoke Analysis for DO TB0107

Smoke - digital_outputs.sim [Derating File: DeRating.drt] Component Filter = [*]

♦	Component	Parameter	Type	Rated Value	% Derating	Max Derating	Measured Value	% Max
	V5	Max Reverse Current	Peak	1u	100	1u	914.0108u	91402
	V6	Max Reverse Current	Peak	1u	100	1u	911.0877u	91109
	V5	Max Reverse Current	RMS	1u	100	1u	17.1175u	1712
	V6	Max Reverse Current	RMS	1u	100	1u	13.0589u	1306
	K1	NPN max E-C vol	RMS	7	100	7	21.1806	303
	K2	NPN max E-C vol	RMS	7	100	7	20.8101	298
	K2	Maximum power dissipation	Peak	210m	100	210m	210.1364m	101
	K1	Maximum power dissipation	Peak	210m	100	210m	210.1916m	101
	V4	Max reverse voltage	RMS	2.5000	75	1.8750	1.4499	78
	V1	Max reverse voltage	RMS	2.5000	75	1.8750	1.4284	77
	C3	Maximum voltage	Peak	50	80	40	29.8989	75
	C1	Maximum voltage	Peak	50	80	40	29.8989	75
	C4	Maximum voltage	Peak	50	80	40	29.1582	73
	C2	Maximum voltage	Peak	50	80	40	29.1582	73
	R5	Maximum power dissipation	Peak	250m	52	131.2302m	85.0198m	65
	R6	Maximum power dissipation	Peak	250m	52	131.2302m	85.0198m	65
	C1	Maximum voltage	RMS	50	80	40	21.5062	54
	C3	Maximum voltage	RMS	50	80	40	21.1292	53
	C4	Maximum voltage	RMS	50	80	40	20.6269	52
	C2	Maximum voltage	RMS	50	80	40	20.2296	51
	K2	NPN max C-E vol	Peak	80	75	60	29.4601	50
	K1	NPN max C-E vol	Peak	80	75	60	29.4601	50
	R5	Maximum breakdown temperature	Peak	200	100	200	95.0158	48
	R6	Maximum breakdown temperature	Peak	200	100	200	95.0158	48
	V1	Maximum junction temperature	Average	85	69	59.5000	27	46
	V1	Maximum junction temperature	Peak	85	69	59.5000	27	46
	V1	Maximum junction temperature	RMS	85	69	59.5000	27	46
	V4	Maximum junction temperature	Average	85	69	59.5000	27	46
	V4	Maximum junction temperature	Peak	85	69	59.5000	27	46
	V4	Maximum junction temperature	RMS	85	69	59.5000	27	46
	R3	Maximum breakdown temperature	Peak	155	80	124	54.0906	44
	R1	Maximum breakdown temperature	Peak	155	80	124	54.2316	44
	C1	Maximum voltage	Average	50	80	40	15.8880	40
	C3	Maximum voltage	Average	50	80	40	15.3496	39
	R5	Maximum power dissipation	RMS	250m	62	156.1155m	60.1345m	39
	R5	Maximum breakdown temperature	RMS	200	100	200	75.1076	38
	R6	Maximum power dissipation	RMS	250m	62	157.2925m	58.9575m	38
	R6	Maximum breakdown temperature	RMS	200	100	200	74.1660	38
	C4	Maximum voltage	Average	50	80	40	14.6504	37
	R4	Maximum breakdown temperature	Peak	155	80	124	43.4580	36
	C2	Maximum voltage	Average	50	80	40	14.1120	36

Smoke - digital_outputs.sim [Derating File: DeRating.drt] Component Filter = [*]

♦	Component	Parameter	Type	Rated Value	% Derating	Max Derating	Measured Value	% Max
	K1	NPN max C-E vol	RMS	80	75	60	21.1806	36
	R2	Maximum breakdown temperature	Peak	155	80	124	43.4580	36
	K2	NPN max C-E vol	RMS	80	75	60	20.8101	35
	R3	Maximum breakdown temperature	RMS	155	80	124	41.3496	34
	R1	Maximum breakdown temperature	RMS	155	80	124	41.0596	34
	R4	Maximum breakdown temperature	RMS	155	80	124	38.6374	32
	R5	Maximum breakdown temperature	Average	200	100	200	61.0375	31
	R2	Maximum breakdown temperature	RMS	155	80	124	38.4023	31
	R3	Maximum breakdown temperature	Average	155	80	124	37.1467	30
	R1	Maximum breakdown temperature	Average	155	80	124	36.7408	30
	R6	Maximum breakdown temperature	Average	200	100	200	59.7390	30
	R4	Maximum breakdown temperature	Average	155	80	124	35.2289	29
	R2	Maximum breakdown temperature	Average	155	80	124	34.8998	29
	R3	Maximum power dissipation	Peak	100m	50	50m	13.5453m	28
	R1	Maximum power dissipation	Peak	100m	50	50m	13.6158m	28
	D3	Maximum junction temperature	Average	150	70	105	27	26
	D3	Maximum junction temperature	Peak	150	70	105	27	26
	D3	Maximum junction temperature	RMS	150	70	105	27	26
	D2	Maximum junction temperature	Average	150	70	105	27	26
	D2	Maximum junction temperature	Peak	150	70	105	27	26
	D2	Maximum junction temperature	RMS	150	70	105	27	26
	D1	Maximum junction temperature	Average	150	70	105	27	26
	D1	Maximum junction temperature	Peak	150	70	105	27	26
	D1	Maximum junction temperature	RMS	150	70	105	27	26
	K1	NPN max C-E vol	Average	80	75	60	15.3134	26
	D4	Maximum junction temperature	Average	150	70	105	27	26
	D4	Maximum junction temperature	Peak	150	70	105	27	26
	D4	Maximum junction temperature	RMS	150	70	105	27	26
	R5	Maximum power dissipation	Average	250m	69	173.7031m	42.5469m	25
	K2	NPN max C-E vol	Average	80	75	60	14.7706	25
	R6	Maximum power dissipation	Average	250m	70	175.3262m	40.9238m	24
	K2	LED max rev voltage	RMS	6	75	4.5000	961.9500m	22
	K1	LED max rev voltage	RMS	6	75	4.5000	954.2657m	22
	K2	NPN max Ic	Peak	50m	80	40m	8.2342m	21
	K1	NPN max Ic	Peak	50m	80	40m	8.2486m	21
	V6	Maximum junction temperature	Average	150	100	150	27	19
	V6	Maximum junction temperature	Peak	150	100	150	27	19
	V6	Maximum junction temperature	RMS	150	100	150	27	19
	V1	Maximum power dissipation	Peak	105m	65	68.2500m	12.9257m	19
	V4	Maximum power dissipation	Peak	105m	65	68.2500m	12.9261m	19
	V5	Maximum junction temperature	Average	150	100	150	27	19
	V5	Maximum junction temperature	Peak	150	100	150	27	19

Smoke - digital_outputs.sim [Derating File: DeRating.drt] Component Filter = [*]

♦	Component	Parameter	Type	Rated Value	% Derating	Max Derating	Measured Value	% Max
	V5	Maximum junction temperature	RMS	150	100	150	27	19
	R4	Maximum power dissipation	Peak	100m	50	50m	8.2290m	17
	R2	Maximum power dissipation	Peak	100m	50	50m	8.2290m	17
	C5	Maximum voltage	Peak	250	80	200	30	16
	C5	Maximum voltage	RMS	250	80	200	30.0000	16
	R3	Maximum power dissipation	RMS	100m	50	50m	7.1748m	15
	C5	Maximum voltage	Average	250	80	200	30.0000	15
	R1	Maximum power dissipation	RMS	100m	50	50m	7.0298m	15
	K2	LED max If	Peak	80m	50	40m	5.8980m	15
	K1	LED max If	Peak	80m	50	40m	5.9132m	15
	V1	Maximum power dissipation	RMS	105m	65	68.2500m	8.9483m	14
	V4	Maximum power dissipation	RMS	105m	65	68.2500m	9.1324m	14
	R4	Maximum power dissipation	RMS	100m	50	50m	5.8187m	12
	R2	Maximum power dissipation	RMS	100m	50	50m	5.7012m	12
	R3	Maximum power dissipation	Average	100m	50	50m	5.0733m	11
	V1	Maximum power dissipation	Average	105m	65	68.2500m	6.1996m	10
	R1	Maximum power dissipation	Average	100m	50	50m	4.8704m	10
	K2	LED max If	RMS	80m	50	40m	3.6063m	10
	V4	Maximum power dissipation	Average	105m	65	68.2500m	6.4575m	10
	R4	Maximum power dissipation	Average	100m	50	50m	4.1145m	9
	V1	Max forward current	Peak	160m	50	80m	6.7677m	9
	V4	Max forward current	Peak	160m	50	80m	6.7679m	9
	K1	LED max If	RMS	80m	50	40m	3.5344m	9
	R2	Maximum power dissipation	Average	100m	50	50m	3.9499m	8
	K2	LED max If	Average	80m	50	40m	2.5503m	7
	K1	LED max If	Average	80m	50	40m	2.4490m	7
	R3	Maximum voltage	Peak	50	80	40	2.2984	6
	V1	Max forward current	RMS	160m	50	80m	4.6852m	6
	R1	Maximum voltage	Peak	50	80	40	2.3044	6
	K2	NPN max Ic	RMS	50m	80	40m	2.0573m	6
	V4	Max forward current	RMS	160m	50	80m	4.7816m	6
	K1	NPN max Ic	RMS	50m	80	40m	2.0204m	6
	V1	Max forward current	Average	160m	50	80m	3.2460m	5
	V4	Max forward current	Average	160m	50	80m	3.3811m	5
	R4	Maximum voltage	Peak	50	80	40	1.2171	4
	R3	Maximum voltage	RMS	50	80	40	1.4066	4
	R1	Maximum voltage	RMS	50	80	40	1.3782	4
	K2	NPN max Ic	Average	50m	80	40m	1.4555m	4
	K1	NPN max Ic	Average	50m	80	40m	1.4024m	4
	R2	Maximum voltage	Peak	50	80	40	1.2171	4
	D3	Maximum power dissipation	Peak	350m	65	227.5000m	4.9496m	3
	R4	Maximum voltage	RMS	50	80	40	860.5827m	3

Smoke - digital_outputs.sim [Derating File: DeRating.drt] Component Filter = [*]

♦	Component	Parameter	Type	Rated Value	% Derating	Max Derating	Measured Value	% Max
	D1	Maximum power dissipation	Peak	350m	65	227.5000m	5.0009m	3
	R3	Maximum voltage	Average	50	80	40	994.7421m	3
	R1	Maximum voltage	Average	50	80	40	954.9584m	3
	K2	Maximum power dissipation	RMS	210m	100	210m	4.5568m	3
	K1	Maximum power dissipation	RMS	210m	100	210m	4.7567m	3
	R2	Maximum voltage	RMS	50	80	40	843.1952m	3
	R4	Maximum voltage	Average	50	80	40	608.5237m	2
	K2	Maximum power dissipation	Average	210m	100	210m	3.1079m	2
	K1	Maximum power dissipation	Average	210m	100	210m	3.0322m	2
	R2	Maximum voltage	Average	50	80	40	584.1826m	2
	D3	Max forward current	Average	1.5000	100	1.5000	1.4649m	1
	D3	Max forward current	Peak	1.5000	100	1.5000	7.3199m	1
	D3	Max forward current	RMS	1.5000	100	1.5000	2.0632m	1
	D3	Maximum power dissipation	Average	350m	65	227.5000m	1.0501m	1
	D3	Maximum power dissipation	RMS	350m	65	227.5000m	1.4811m	1
	V6	Max Forward Current	Average	100	100	100	9.6261u	1
	V6	Max Forward Current	Peak	100	100	100	351.5727u	1
	V6	Max Forward Current	RMS	100	100	100	13.0589u	1
	V6	Maximum power dissipation	Average	600	100	600	149.2522u	1
	V6	Maximum power dissipation	Peak	600	100	600	1.6647m	1
	V6	Maximum power dissipation	RMS	600	100	600	253.2015u	1
	D2	Max forward current	Peak	1.5000	100	1.5000	1.7251u	1
	D2	Max forward current	RMS	1.5000	100	1.5000	372.1456n	1
	D2	Maximum power dissipation	Average	350m	65	227.5000m	19.3733n	1
	D2	Maximum power dissipation	Peak	350m	65	227.5000m	286.5450u	1
	D2	Maximum power dissipation	RMS	350m	65	227.5000m	4.1705u	1
	C3	Maximum current	Average	1	100	1	59.8025n	1
	C3	Maximum current	Peak	1	100	1	3.3367m	1
	C3	Maximum current	RMS	1	100	1	27.9426u	1
	D1	Max forward current	Average	1.5000	100	1.5000	1.4112m	1
	D1	Max forward current	Peak	1.5000	100	1.5000	7.3306m	1
	D1	Max forward current	RMS	1.5000	100	1.5000	2.0248m	1
	D1	Maximum power dissipation	Average	350m	65	227.5000m	1.0114m	1
	D1	Maximum power dissipation	RMS	350m	65	227.5000m	1.4534m	1
	C5	Maximum current	Peak	1	100	1	56.8434f	1
	C4	Maximum current	Average	1	100	1	59.8025n	1
	C4	Maximum current	Peak	1	100	1	3.3367m	1
	C4	Maximum current	RMS	1	100	1	27.9426u	1
	C2	Maximum current	Average	1	100	1	5.3165n	1
	C2	Maximum current	Peak	1	100	1	3.3459m	1
	C2	Maximum current	RMS	1	100	1	43.7079u	1
	C1	Maximum current	Average	1	100	1	5.3165n	1

Smoke - digital_outputs.sim [Derating File: DeRating.drt] Component Filter = [*]

♦	Component	Parameter	Type	Rated Value	% Derating	Max Derating	Measured Value	% Max
	C1	Maximum current	Peak	1	100	1	3.3459m	1
	C1	Maximum current	RMS	1	100	1	43.7079u	1
	V5	Max Forward Current	Average	100	100	100	9.6815u	1
	V5	Max Forward Current	Peak	100	100	100	351.8224u	1
	V5	Max Forward Current	RMS	100	100	100	17.1175u	1
	V5	Maximum power dissipation	Average	600	100	600	155.9007u	1
	V5	Maximum power dissipation	Peak	600	100	600	1.6646m	1
	V5	Maximum power dissipation	RMS	600	100	600	308.7614u	1
	D4	Max forward current	Peak	1.5000	100	1.5000	1.7225u	1
	D4	Max forward current	RMS	1.5000	100	1.5000	238.6302n	1
	D4	Maximum power dissipation	Average	350m	65	227.5000m	25.6428n	1
	D4	Maximum power dissipation	Peak	350m	65	227.5000m	287.8614u	1
	D4	Maximum power dissipation	RMS	350m	65	227.5000m	2.6666u	1
	D3	Peak reverse voltage	Average	1k	100	1k	0	0
	D3	Peak reverse voltage	Peak	1k	100	1k	0	0
	D3	Peak reverse voltage	RMS	1k	100	1k	0	0
	V6	Max Reverse Current	Average	1u	100	1u	-9.6261u	0
	C6	Maximum voltage	Average	250	80	200	0	0
	C6	Maximum voltage	Peak	250	80	200	0	0
	C6	Maximum voltage	RMS	250	80	200	0	0
	C6	Maximum current	Average	1	100	1	0	0
	C6	Maximum current	Peak	1	100	1	0	0
	C6	Maximum current	RMS	1	100	1	0	0
	D2	Max forward current	Average	1.5000	100	1.5000	-1.3183n	0
	D2	Peak reverse voltage	Average	1k	100	1k	0	0
	D2	Peak reverse voltage	Peak	1k	100	1k	0	0
	D2	Peak reverse voltage	RMS	1k	100	1k	0	0
	D1	Peak reverse voltage	Average	1k	100	1k	0	0
	D1	Peak reverse voltage	Peak	1k	100	1k	0	0
	D1	Peak reverse voltage	RMS	1k	100	1k	0	0
	C5	Maximum current	Average	1	100	1	0.0011f	0
	C5	Maximum current	RMS	1	100	1	0.0249f	0
	V1	Max reverse voltage	Average	2.5000	75	1.8750	-1.3048	0
	V1	Max reverse voltage	Peak	2.5000	75	1.8750	-746.1036m	0
	K2	NPN max E-C vol	Average	7	100	7	-14.7706	0
	K2	NPN max E-C vol	Peak	7	100	7	-123.9890m	0
	K2	LED max rev voltage	Average	6	75	4.5000	-941.7943m	0
	K2	LED max rev voltage	Peak	6	75	4.5000	-745.8934m	0
	V4	Max reverse voltage	Average	2.5000	75	1.8750	-1.3280	0
	V4	Max reverse voltage	Peak	2.5000	75	1.8750	-746.1036m	0
	V5	Max Reverse Current	Average	1u	100	1u	-9.6815u	0
	K1	NPN max E-C vol	Average	7	100	7	-15.3134	0

Smoke - digital_outputs.sim [Derating File: DeRating.drt] Component Filter = [*]

♦	Component	Parameter	Type	Rated Value	% Derating	Max Derating	Measured Value	% Max
	K1	NPN max E-C vol	Peak	7	100	7	-123.9966m	0
	K1	LED max rev voltage	Average	6	75	4.5000	-933.9783m	0
	K1	LED max rev voltage	Peak	6	75	4.5000	-745.8934m	0
	D4	Max forward current	Average	1.5000	100	1.5000	-1.7545n	0
	D4	Peak reverse voltage	Average	1k	100	1k	0	0
	D4	Peak reverse voltage	Peak	1k	100	1k	0	0
	D4	Peak reverse voltage	RMS	1k	100	1k	0	0

Appendix D

Figures of nDI TB1350

D.1 Voltage Variation for nDI TB1350: 16.8V, 24V, 30V

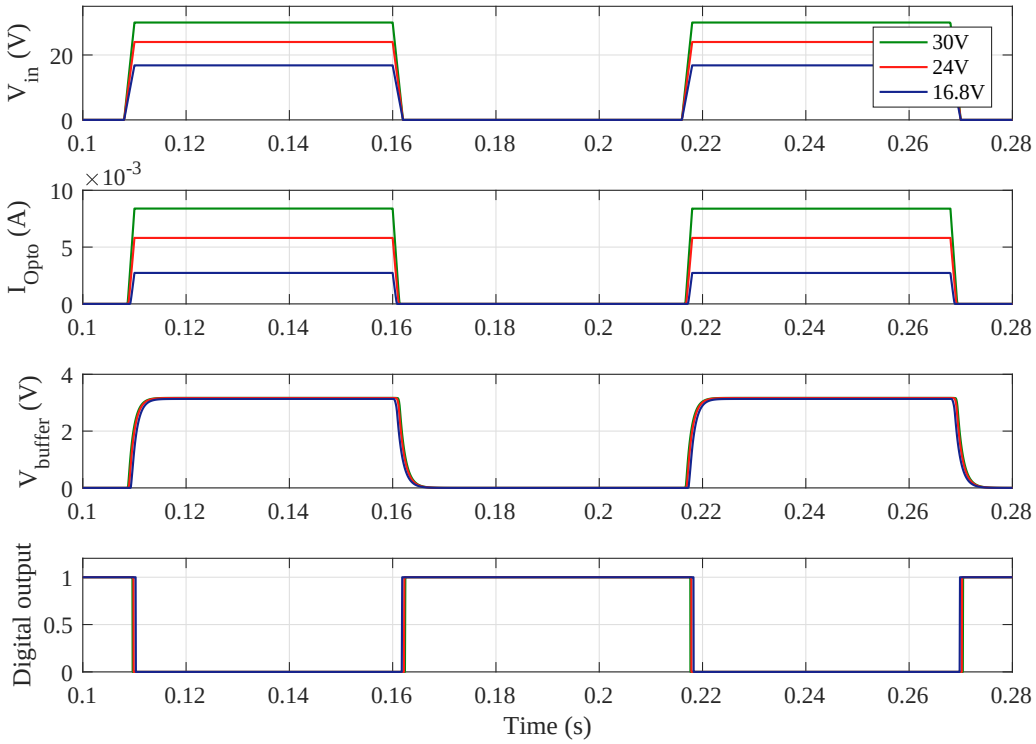


Figure D-1: Transient simulation of the nDI of TB1350 for 16.8V, 24V and 30V: (a) Input voltage. (b) Current flowing through the optocoupler's LED. (c) Voltage at the ouput of the ouptocoupler and the voltage resultant after applying a RC filter. (d) Digital output DI.

D.2 Frequency variation for nDI TB1350

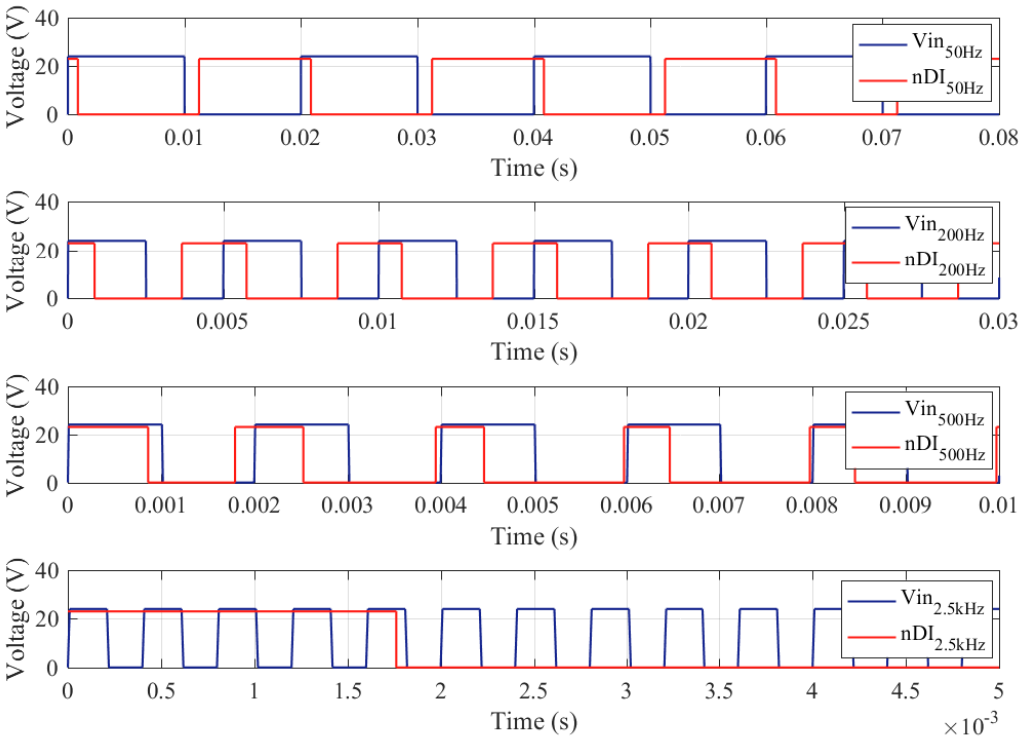


Figure D-2: Frequency variation for nDI TB1350: (a) 50Hz. (b) 250Hz. (c) 4083Hz. (d) 6000Hz.

D.3 Surge Test for nDI TB1350

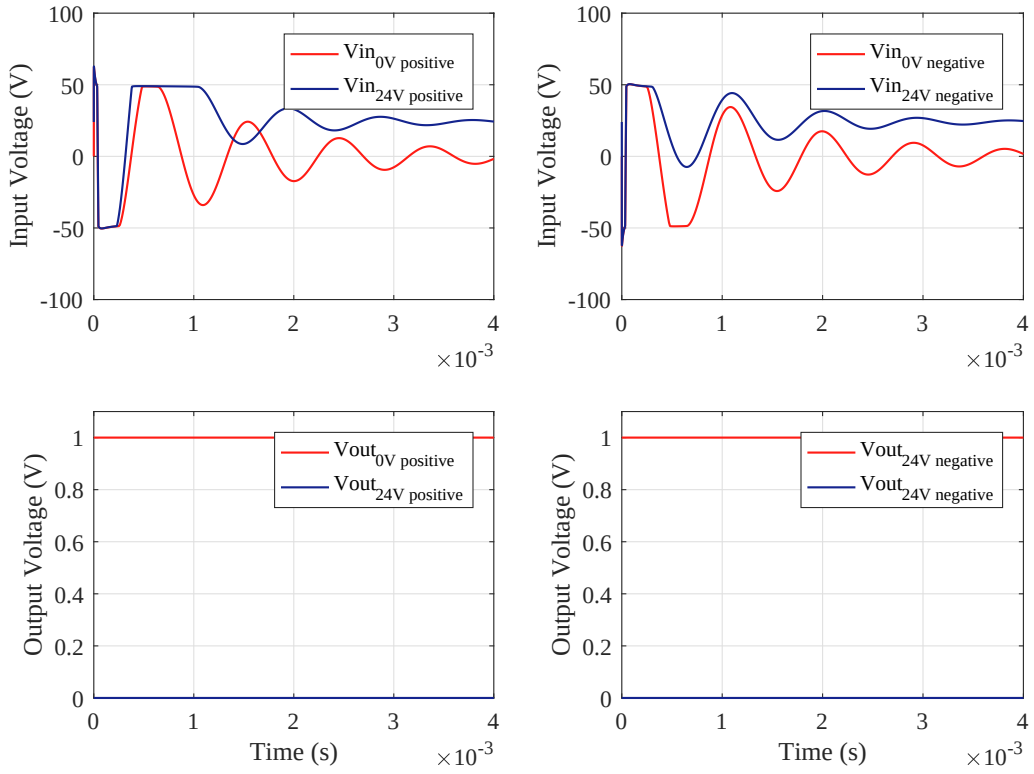


Figure D-3: Surge Test for the nDI TB1350: (a) Input voltage at the PCC with a positive surge (b) DI response to a positive surge. (c) Input voltage at the PCC with a negative surge. (d) DI response to a negative surge.

Appendix E

Figures of DI TB1350

E.1 Voltage Variation for DI TB1350: 16.8V, 24V, 30V

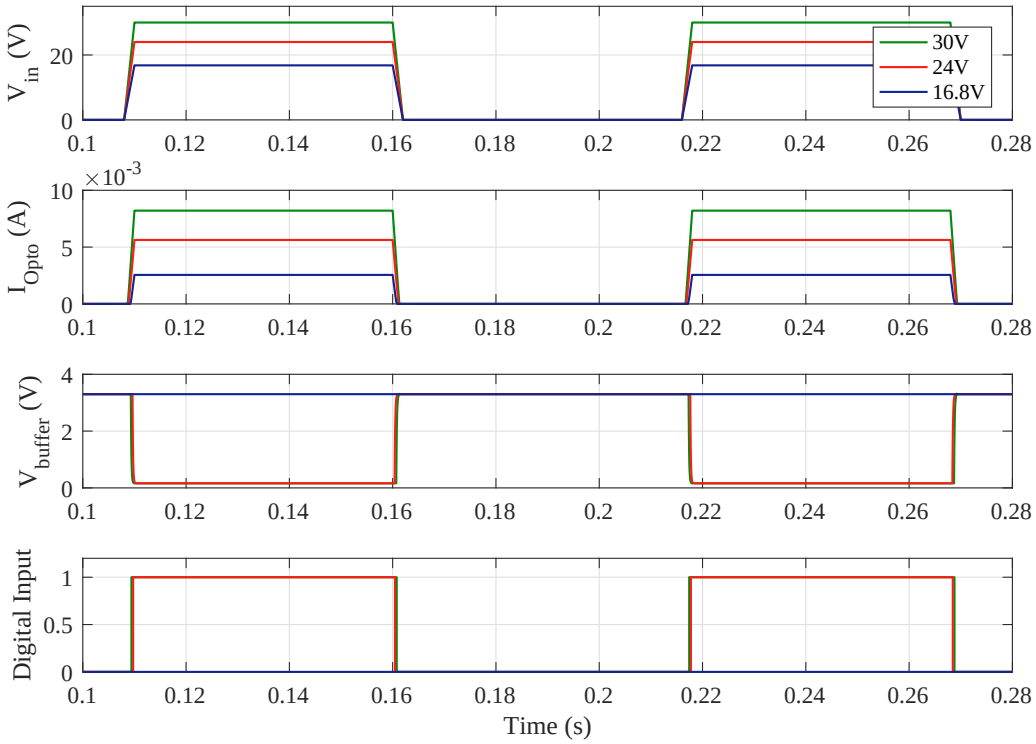


Figure E-1: Transient simulation of the DI of TB1350 for 16.8V, 24V and 30V: (a) Input voltage. (b) Current flowing through the optocoupler's LED. (c) Voltage at the ouput of the ouptocoupler and the voltage resultant after applying a RC filter. (d) Digital output DI.

E.2 Frequency variation for DI TB1350

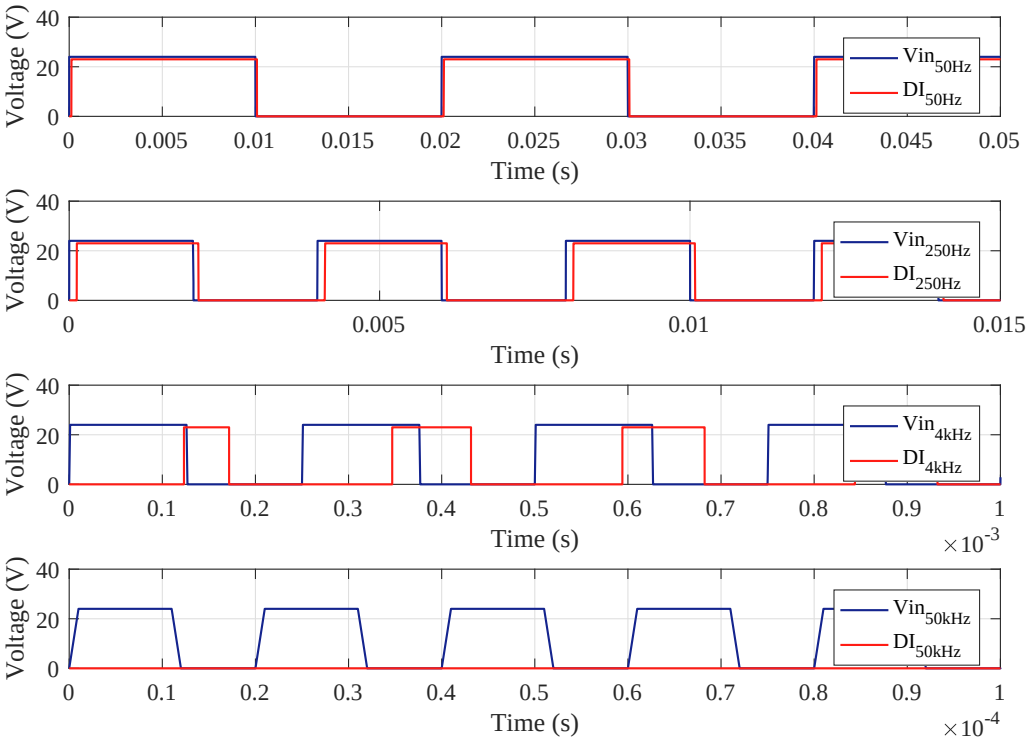


Figure E-2: Frequency variation for DI TB1350: (a) 50Hz. (b) 250Hz. (c) 4083Hz. (d) 6000Hz.

E.3 Surge Test for DI TB1350

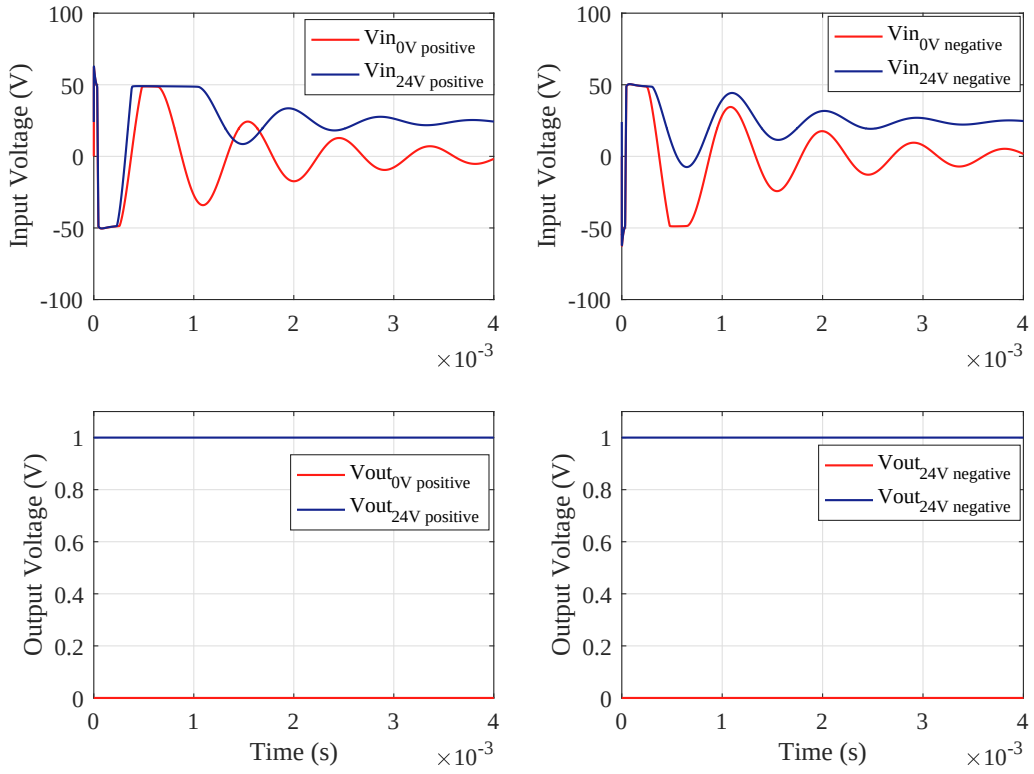


Figure E-3: Surge Test for the DI TB1350: (a) Input voltage at the PCC with a positive surge (b) DI response to a positive surge. (c) Input voltage at the PCC with a negative surge. (d) DI response to a negative surge.

Appendix F

Figures of DO TB1350

F.1 Frequency variation for DO TB1350

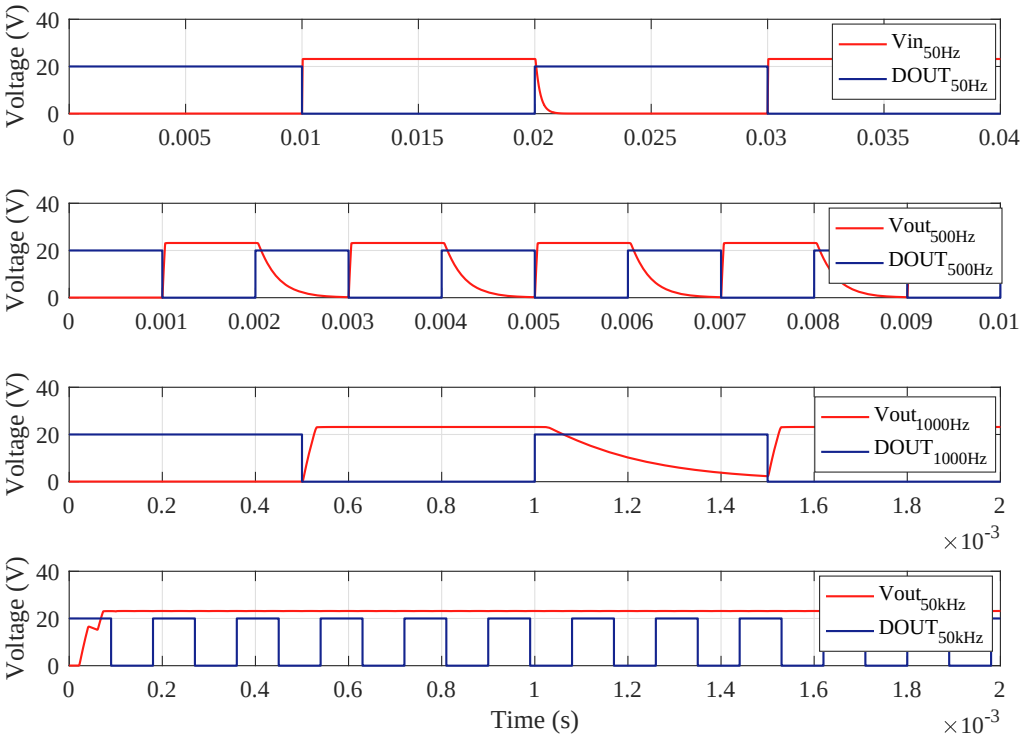


Figure F-1: Frequency variation for DO TB0107: (a) 10Hz. (b) 150Hz. (c) 1500Hz. (d) 50kHz.

Appendix G

Figures of the Encoder

G.1 Voltage Variation for Encoder: 16.8V

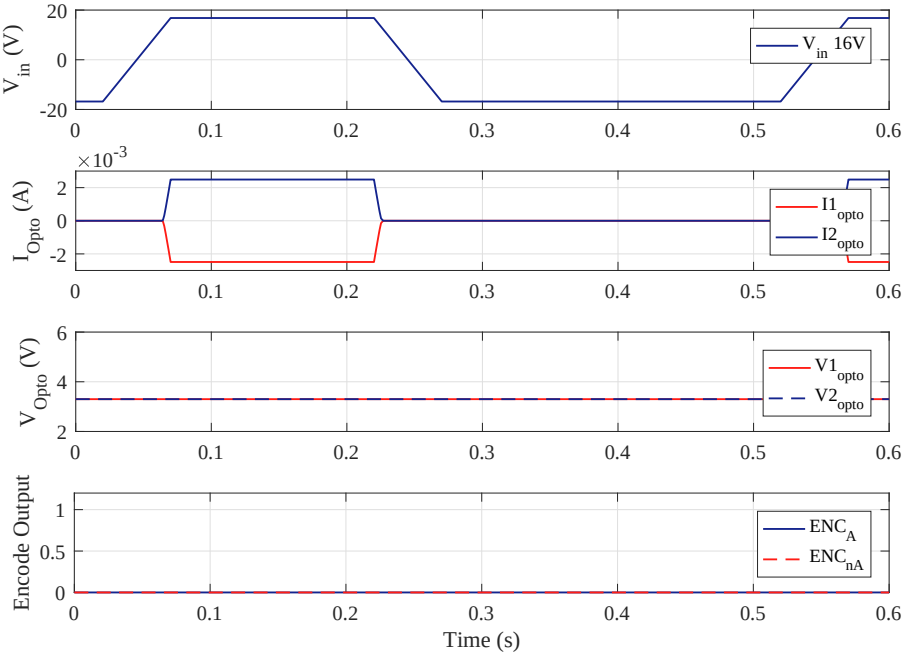


Figure G-1: Transient simulation of the encoder for an input voltage of 16.8V: (a) Input voltage. (b) Current through the upper and lower LED of the optocoupler. (c) Output voltages of the optocoupler. (d) Two channel digital output of the encoder circuit.

G.2 Voltage Variation for Encoder: 30V

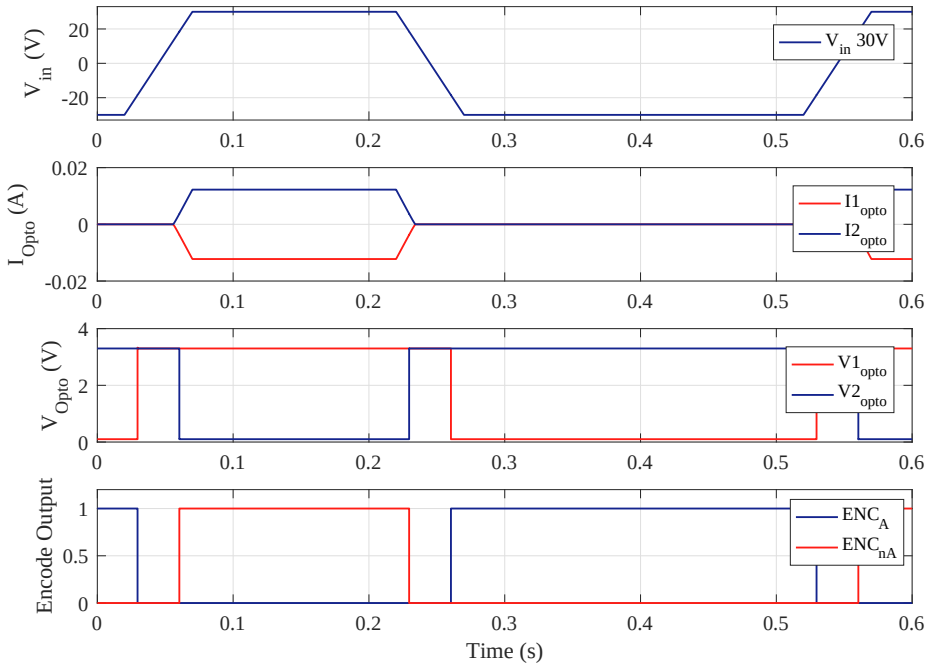


Figure G-2: Transient simulation of the encoder for an input voltage of 30V: (a) Input voltage. (b) Current through the upper and lower LED of the optocoupler. (c) Output voltages of the optocoupler. (d) Two channel digital output of the encoder circuit.

G.3 Frequency variation for Encoder

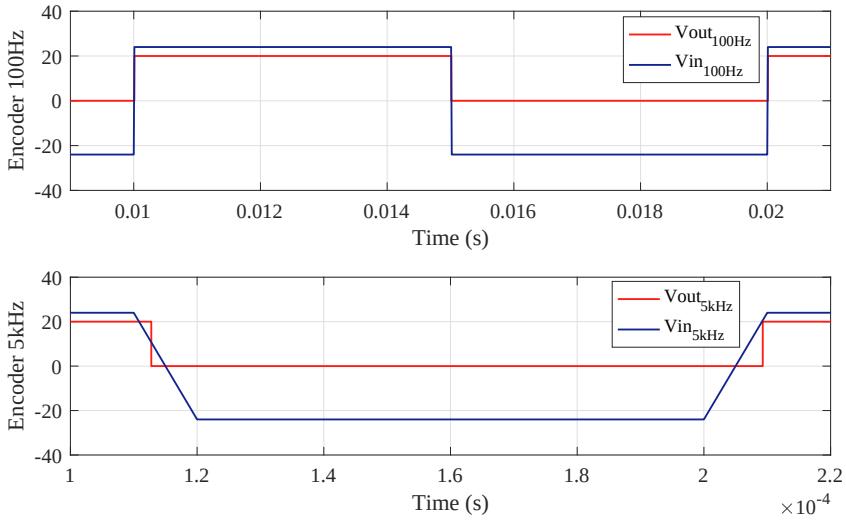


Figure G-3: Frequency variation of the input voltage: (a) 100Hz. (b) 5kHz.

Bibliography

[1] European Court of Auditors. (2016). Nº8: Transporte de mercancías por ferrocarril en la UE: todavía no avanza por la buena vía .

[2] European Commission. (2011). Commission staff working paper: Impact assessment. Communication from the Commission 'Horizon 2020 - The Framework Programme for Research and Innovation'.

[3] Vladimirescu, A. (1994). The SPICE book. John Wiley & Sons, Inc..

[4] Lin, R. L., & Chen, Y. F. (2009, October). Equivalent circuit model of light-emitting-diode for system analyses of lighting drivers. In Industry Applications Society Annual Meeting, 2009. IAS 2009. IEEE (pp. 1-5). IEEE.

[5] Adamopoulou, L., & Alexiou, M. K. G. The concept of hierarchical design: the views of computer science and engineering students.

[6] Cadence. (2004, November). PSpice Advanced Analysis User's Guide.

[7] Denning, R. (2012). Applied R&M Manual for Defence Systems. Part C - R&M Related Techniques MoD, Abbey Wood.