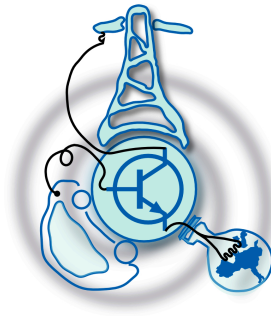# Modular Converters for Electrical Energy Storage

by

Miguel Crespo Iglesias

Submitted to the Department of Electrical Engineering, Electronics,
Computers and Systems
in partial fulfillment of the requirements for the degree of

Master Course in Electrical Energy Conversion and Power Systems

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Abstract

In this Master Thesis, different modular converters are studied, designed and compared for an electrical energy storage system based on lithium cells. The main objective of the modular converter is to boost the voltage of a battery pack from 48V to 400V, allowing bidirectional power transfer, charge and discharge from the bus to the battery. Rated for a 18 kW, the presented document includes also a prototype design for a Dual Active Bridge using a three phase transformer.

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Acknowledgments

Contents

List of Figures

List of Tables

Chapter 1

Introduction

Battery energy storage systems (BESS) are increasingly used to stabilize and balance our energy supply system. Current technology development focuses on new system designs with improved modularity, scalability and efficiency [1]. Typical energy storages systems (ESS) are based on super-capacitors, flywheel, electrochemical cells or fuel cells. All of these systems presents different operation ranges, Figure 1-1 shows the ranges in terms of power, energy and discharge/charge time [2]. Electrochemical batteries cover the mid range of power and energy, where most popular choices are Lithium - Ion (Li-Ion) and Lead Acid batteries.
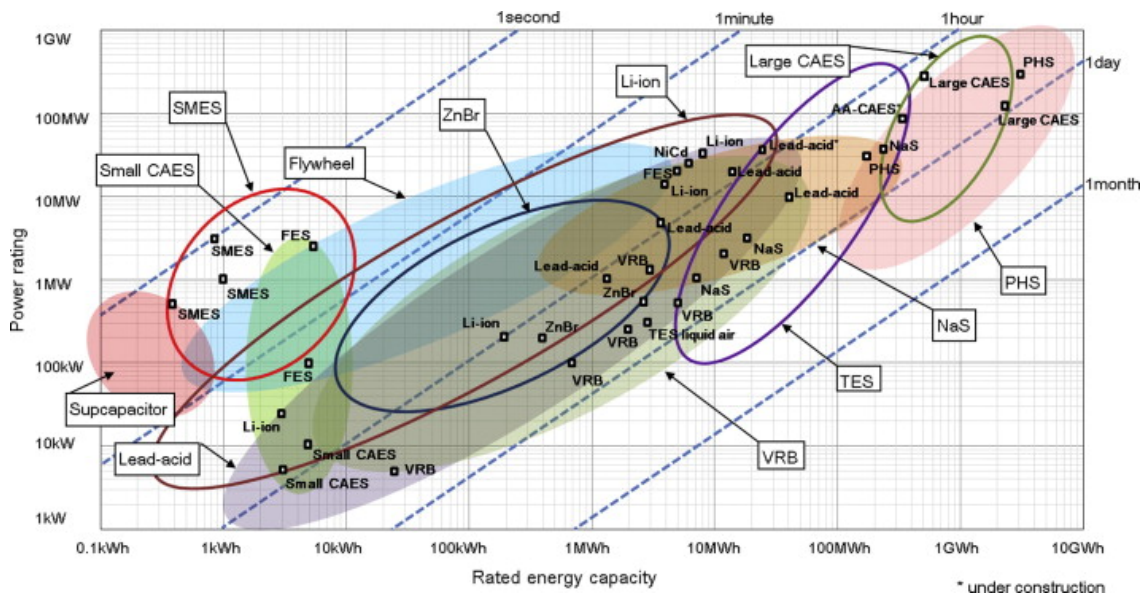
Figure 1-1: Comparation between the different ESSs. [2]

The main drawback of electrochemical cells is the low voltage level, around 3-4 volts, that is not useful for power applications. A typical solution to boost the voltage includes arrays of cells in series to obtain a medium voltage (400 V). However, this solution, usually is not sustainable for high voltage because it implies arrangements of too many cells in series. In Figure 1-2 a typical passive structure is shown where many cells are connected in parallel to achieve a high energy level, these parallel arrays are connected in series to boost the low voltage of the cell.
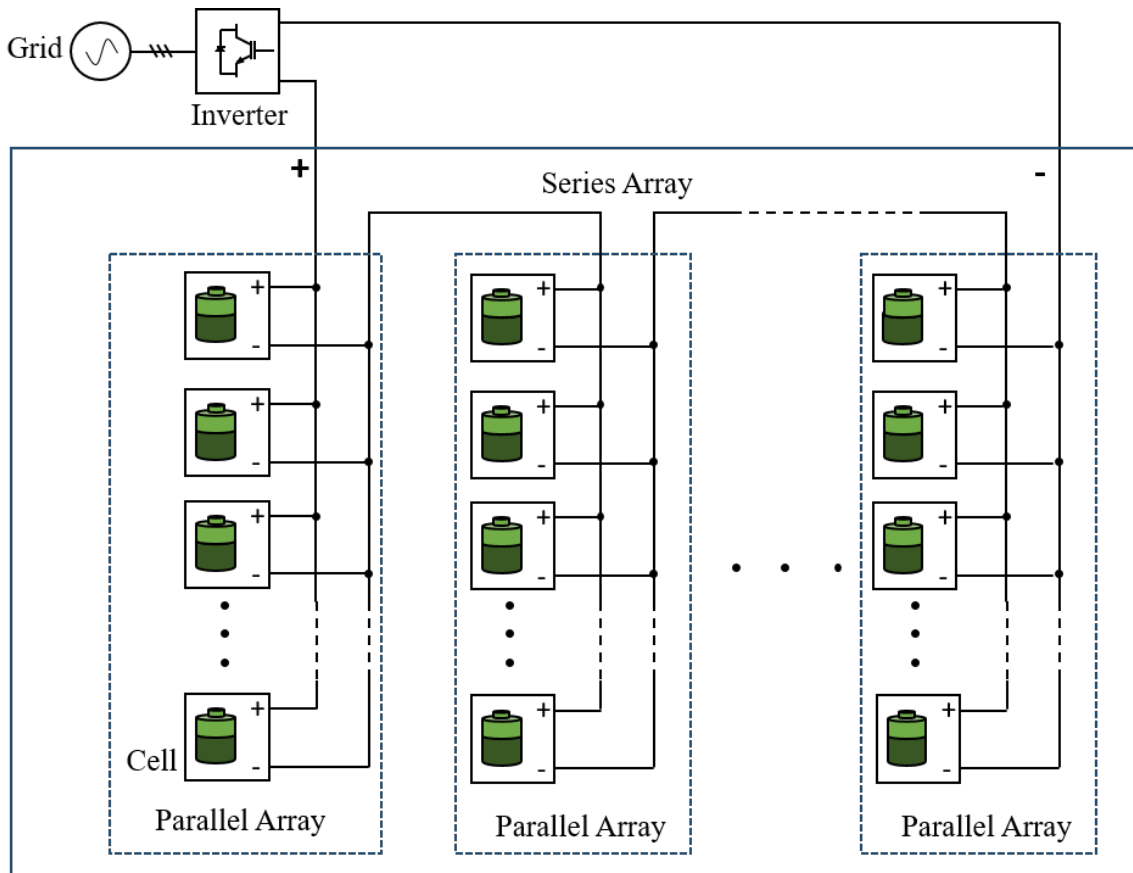
Figure 1-2: Passive array structure.

This kind of arrange is the simplest option, however it requires a similar behaviour of each module. For batteries the voltage of each cell depends on the State of Charge (SOC), and depending the type of cell the behaviour of the voltage varies. It implies voltage unbalances between cells that generates SOC variations between modules. In order to solve this problem, equalization systems are included in each series module, balancing the voltage of each cell. Despite equalization systems allow a better man-

agement of cells. Nevertheless, a voltage boost is needed to avoid huge numbers of arrays and equalization systems. To solve this problem modular power converters are used. These power converters are designed to boost and control the voltage of each cell, so it is possible to reduce the number of cells in series per module. A modular converter allows power exchange between cells. For this application, modular converters usually include one DC/DC converter per cell array or battery pack and they are connected to a common mid voltage DC bus, as Figure 1-3 shown.
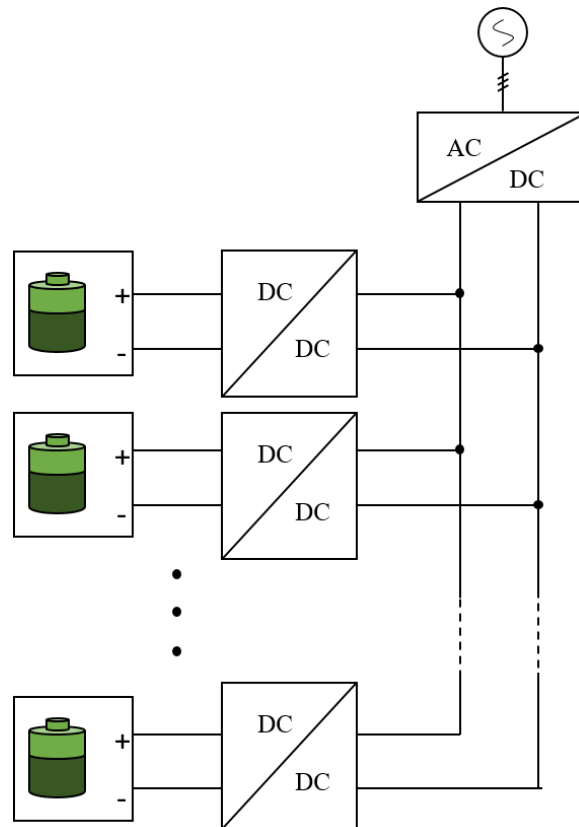
Figure 1-3: Typical modular converter structure.

Some advantaged of modular converter involves good reliability, efficiency, expansion capacity, easy maintenance and strong monitoring function [3]. In this Master Thesis, a modular converter is presented for a battery pack of a rated voltage of 48V, rated energy storage 180 Ah and maximum power of 18 kW. This converter is part of a structure which control several battery packs interconnected through a 400V bus.

17

1.1 Master Thesis Objectives & Motivation

This master thesis is focused in the design of a modular power converter for a BESS based on lithium-ion (Li-ion) used in stationary applications. These kind of systems require many modules being attached in series or parallel, to arrange high power or energy requirements. Usually they are connected passively using only one DC/DC converter to control the overall system.

In this case, due to the control and management system requirements, every Li-ion module must behave in a similar manner. Li-ion voltage are non linear elements where the voltage strongly depends on SOC of the battery. Figure 1-4 shows the voltage for different SOC in percent for a tested Li-ion of Iron Phosphate type during a charge process. This graph shows that different level of voltage also implies different SOCs and therefore when two or more cells has different levels of voltage the cells with lower voltage has less capacity, so voltage unbalances implies energy capacity losses. For this reason, Li-ion must be monitoring and controlled by an electronic device.
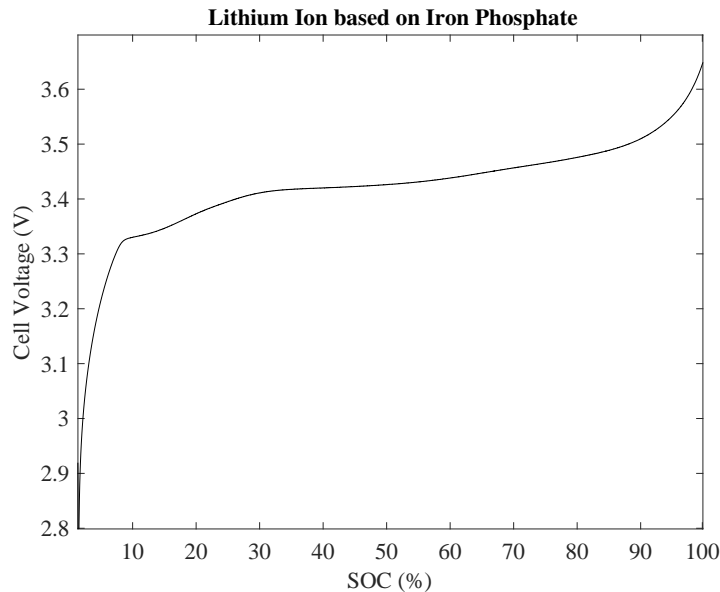
Figure 1-4: Voltage dependence of SOC for a Li-ion Iron Phosphate cell.

This project will contemplate different options for modular power converters, being the motivation of the master thesis the study, design and implementation of one of this

module. In order to achieve this goal, a prototype will be designed and an analysis of the converter will be done using a electronic circuit software tool, PLECS & Matlab, to show the availability of the design.

1.2   Master Thesis Structure

This master thesis is structure as follows.

- Chapter 2 is an overview of the state of the art of BESSs and DC/DC modular topologyes.

- Chapter 3 includes the project description with the scope of the project.

- Chapter 4 presents the design of the proposed DC/DC converter, the selection of different elements, as semiconductor devices, inductors, capacitor, etcetera.

- Chapter 5 shows the design of the prototype design.

- In Chapter 6 the control design for the proposed DC/DC converter is designed, studied and analysed using the simulation software tools: Matlab & PLECS.

- Chapter 7 includes conclusions and future implementations.

Chapter 2

State of the Art

Electrochemical BESSs exchange energy through oxidation/reduction reactions. They can divided in two big group: Secondary Batteries and Flow batteries. Battery used in this project will be a Li-Ion battery. This kind of cell is included into the secondary batteries group, where also are included very well known batteries as the Lead Acid, Niquel based (NiCd/NiMH), metal air or Sodium based (Sulphur and Nickel Chloride).

In secondary batteries, cells are formed by a positive electrode (cathode), a negative electrode (anode) and electrolyte solution , , dividing each electrode with a separator. Structure of a cell is represented in Figure 2-1.

The operation principle of this type of battery consists to put the cathode paired with the anode inducing the motion of ions in response to an electric field to maintain local and global electroneutrality [4]. For secondary batteries the energy is charged and discharged in the active masses of the electrodes. In contrast with the flow batteries where the energy is storage in one or more electroactive species which are dissolved in liquid electrolytes [5].

In electrochemical batteries, the voltage is indicated by the electrochemical window (EW), and it is calculated by the subtracting between the potential of the cathode from the anode. The maximum potential obtained is between 5 V and 6 V, and is produced in Li-Ion batteries.
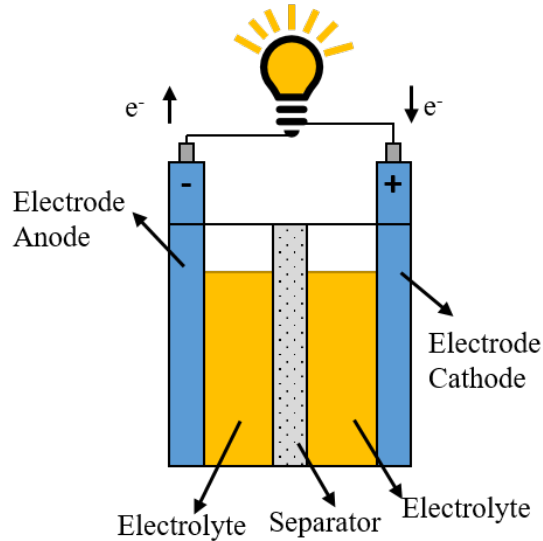
Figure 2-1: Typical structure of a secondary cell.

2.1   Lithium Ion Batteries

Nowadays Li-ion batteries are the most important storage technology in the areas of portable and mobile applications, becoming to be a good alternative for lead batteries in stationary applications. This technology has a high voltage cell level, in contrast with other cells as Niquel based cells. Also Li-ion presents huge gravimetric energy density and a high efficiency around the 97%. The main obstacle is the high cost of more than USD 600/kWh [5], which is related with the special packaging and internal overcharge protection circuits, because most of the metal oxide electrodes are thermally unstable, which can decompose at elevated temperatures releasing oxygen which can lead to a thermal runaway. For that reason, Li-Ion management systems must be continuous monitoring the temperature and voltage of each cell.

2.1.1   Lithium Ion configurations

Li-ion follows the typical structure of secondary cells. Usually the cathode is a lithium oxide metal and the anode is a carbon with an organic electrolyte. Changing the metal of the cathode is possible to obtain different properties for the battery. Then, the Li-ion batteries are classify based on the metal chemistry, being the most popular

types of Li-ion:

- **Lithium Cobalt Oxide (LCO)**: this type of battery presents a high specific energy, but a low life span, thermal instability and low power options. They are used in mobile phones, laptops and digital cameras [6].

- **Lithium Manganese Oxide (LMO)**: low internal resistance that allows a fast charge / discharge time with high-current discharging. This type of battery presents a low life span and lower capacity. They are not common in the market, only used for some specific applications in power tools, medical or power trains.

- **Lithium Nickel Manganese Cobalt Oxide (LNMCO)**: with a combination of nickel, manganes and cobalt (NMC) this type of Li-ion battery is one of the most common batteries. With less power than LMO, LNMCO presentes a high specific energy, good specific power and better performance and life spam than LMO. For that reasons they are used instead of LMO in medical, power trains, power tools or e-bikes. [6].

- **Lithium Iron Phosphate Oxide(LFPO)**: With a low internal resistance and a good performance, LFPO batteries allows a high current rated and long cycle life. Also they have a good thermal stability being one of the most safe cells.

2.2 Power Converter Topologies for Battery-Pack Systems

BESS are a very versatile systems covering a wide range of power and energy storage defined by the application. In this document the battery pack is connected to a 400V bus through a DC/DC converter. The DC/DC converter is selected based on: power

requirements, parallel connection with other DC/DC converter, voltage boost ratio and isolation or non-isolation. Among the different availability options, some of these will be a better choice for modular systems.

Along this section different options will be discussed, with an special emphasis in those converter that can implement at module level. Organizing them in two big groups: Isolated converters and Non-Isolated Converters.

2.2.1 Isolated Converters

This type of DC/DC interface include transformers to provide galvanic isolation. In order to reduce size, cost and improve efficiency these converters use a high frequency transformer.

Dual Active Bridge

As alternative for the bidirectional boost converter, Dual Active Bridges (DAB) converters are the most common topology for isolated options. It includes a transformer between two bridges, Figure 2-2. The most simple control manages the phase shift between sides of the transformer. More complex designs use three degrees of freedom to implement soft-switching modulations controlling duty ratio in each bridge [8].
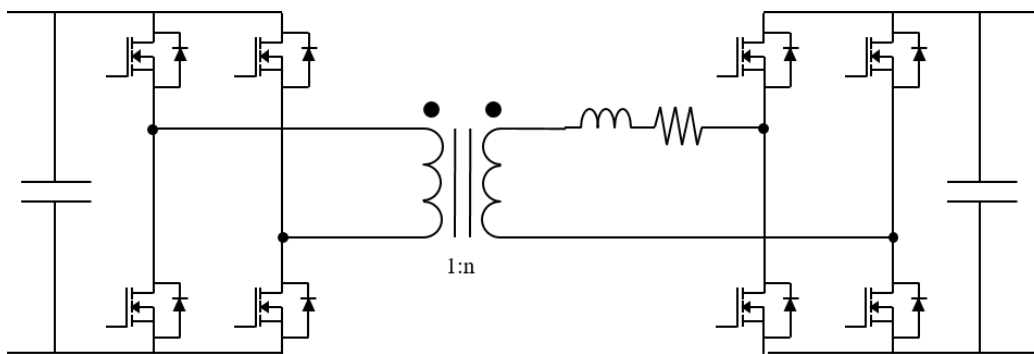
Figure 2-2: DAB converter topology.

Three Phase Dual Active Bridge

Based on a DAB converter, the Three Phase Dual Active Bridge (TPDAB) behaves similar to the DAB but the transformer array is a three phase transformer. Presented for first time in [9] this system implies more semiconductors and adding another winding in the transformer with respect the DAB converter, but also allows a lower peak current through devices and better current ripple at input and output. Schematic is presented in Figure 2-3.
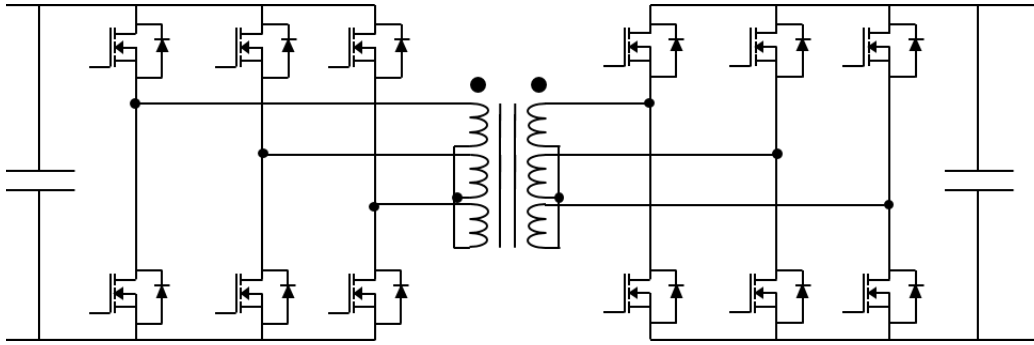
Figure 2-3: TPDAB schematic.

Bidirectional Push-Pull Converter

Push-pull converters can be also used as interface for batteries replacing the diode rectifier by an active bridge, as is shown in Figure 2-5. In comparison with the DAB converter, it replaces a half bridge but adds a new winding in the transformer.
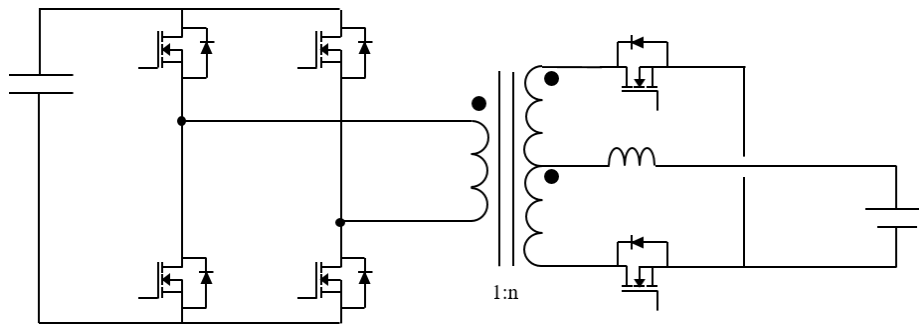
Figure 2-4: Push-pull Converter. [10]

Half-Bridge Converter

Another isolated topology is the half-bridge converter. Presented in Figure 2-5 is formed by a push-pull converter with a half-bridge at the high voltage side and two winding in the low voltage side. This converter allows low ripple in the low voltage side and less components than the TPDAB, but the system is more complex.
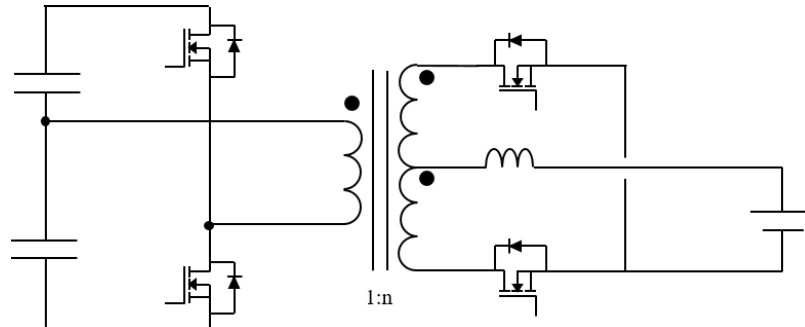
Figure 2-5: Half-Bridge Converter. [11]

Double Half-Bridge

Isolated symmetry half-bridge converter allows a high boost-ratio, simple circuit topology and bidirectional features. The main drawback of this converter is the high leakage inductance and problems to obtain zero voltage switching [12]. Figure 2-6 shows the topology.
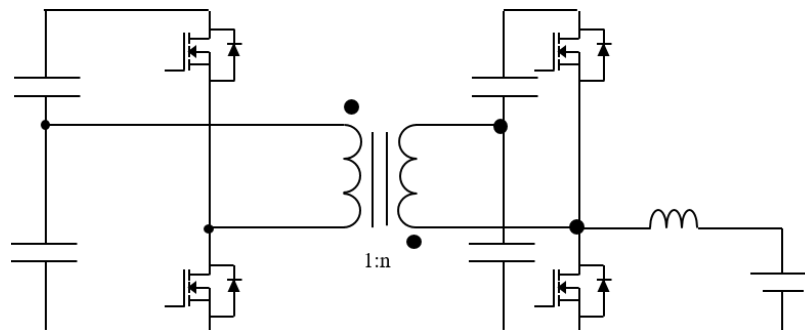
Figure 2-6: Double Half-bridge topology.

2.2.2 Non-Isolated Converter

Bidirectional Boost Converter (BDC Boost)

This is the most common non-isolated topology, due to it's simple design, well-known controllability and cheap implementation. This topology is commonly used in configuration with a double power stage. Figure 2-7 shows the circuit of a bidirectional boost converter (BDC).
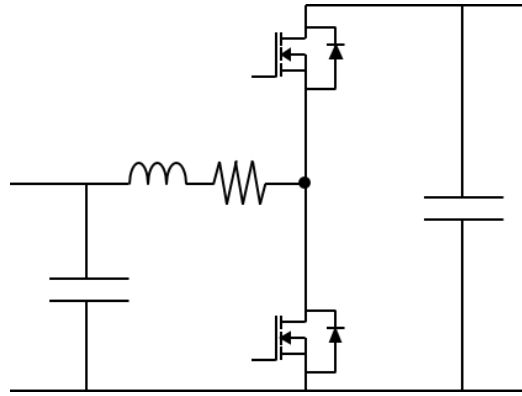
Figure 2-7: Bidirectional Boost Converter topology.

The main drawback of this topology is the operation range, for those applications with a boost ratio higher than 5 the system do not work as expected.

High Gain Bidirectional Bridge Boost Converters

Those applications where the classic bidirectional boost do not allows the needed step up ratio, new topologies with high gain ratios are introduced. A high gain boost converter is show in Figure 2-8. It consists in a bridge, where the battery is connected between the bridge switches allowing two times the ratio of a classic bidirectional boost [13].

Quadratic Boost Converter

Another options include complex systems that use coupled inductors or resonant cells to obtain better performances. One of this option is the Quadratic Boost Converter. Is former by two boost converter in series with a coupled inductor allowing high
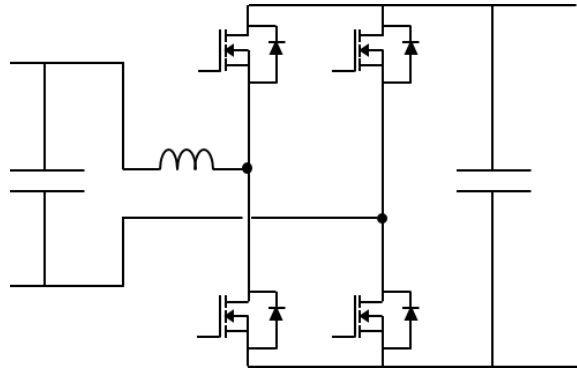
Figure 2-8: Bidirectional Bridge Boost Converter [13]

voltage rates and better power distribution between stages. Figure 2-9 shows the schematic.
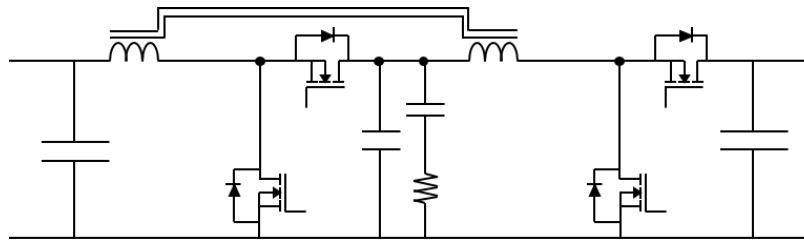
Figure 2-9: Quadratic Boost Converter [14].

2.2.3 Comparative

A qualitative comparison between previous topologies is attached in Table 2.1. Main aspects analysed for this application are the boost ratio, modularity, how easy and how much costs implement more of this topologies, isolation, efficiency and costs.

Table 2.1: DC/DC comparison

Converter	Boost Ratio	Modularity		Isolation	Efficiency	Cost
		Implementation	Cost			
DAB	High	Easy	Cheap	Yes	Good	Cheaper than TPDAB
TPDAB	High	Easy	Expensive	Yes	Very Good	Expensive
Push-Pull	High	Complex	Expensive	Yes	Good	Expensive
Half-Bridge Converter	High	Complex	Expensive	Yes	Very Good	Cheaper than Push
Double Half-Bridge	High	Complex	Expensive	Yes	Very Good	Cheaper than Push
BDC Boost	Low	Easy	Cheap	No	Good	Cheap
High Gain BDC Bridge Boost	Medium	Easy	Cheap	No	Bad	Cheap
Quadratic Boost	Medium	Complex	Cheap	No	Good	Expensive

28

Main challenges for DC/DC converters for battery packs are the huge current and variable low voltage in the input of the converter. To manage this current some applications keep the same topology adding parallel switching devices. This implementation increase the number of semiconductors, and is not trivial the parallelism of switching devices due to non linearities in the system due to current is not distributed evenly.

In this project, to manage the current for the cases of half-bridge, double half-bridge and push-pull the needed number of converters in the output increases from two switches to eight switches. Also, Half-bridge implies two series capacitors operating at the same voltage level, then unbalances in voltage capacitors will be translate into problems in the output voltage. Also those converters which add resonant circuits to increase efficiency are even more complex since the switching frequency is used to control the device. Moreover the variable input voltage can be a problem in terms of unbalance of capacitors, being critical for the double half-bridge converter.

Another topologies, as DAB or Boost converters allows a technique known as interleaved. It consist instead put parallel switching devices use parallel bridges or legs. In the DAB converter the interleaved is formed by a transformer with one secondary at high voltage / low current and two or more primaries that distribute the current, with a phase shift in the carry signal of the duty is possible compensate the current ripple of each leg reducing the current ripple input. For this application the needed interleaved legs will be 3, that implies moving to twelve semiconductors and three primaries.

In the case of the Boost converter the main drawbacks are the non-isolation and the low voltage ratio, being needed at least two of this BDC boosts in parallel to obtain the desire voltage. Also parallel semiconductor or interleaved will be needed to manage the current at the battery side.

Quadratic boost could be a good option to obtain a good boost ratio, but will also need parallel semiconductors and couple inductors are introduced without providing galvanic isolation.

Table 2.1 shows that one of the best topologies is the TPDAB, but also is expensive

to increase modularity. Aslo, TPDAB needs complex controls implemntations for variable input voltages. Study of [9] shows how the converter tends to work in hard switching zones when the ratio between voltages is not kept at 1. To manage currents in the primary of this converter adding interleaving is a expensive option because the primary is moving from 3 windings to 9 windings (three interleaved bridges), so parallel switching devices should be implemented increasing the number from 6 to 18 switching devices in the primary.

Another option is used this converter with an additional circuit that compensate those problems. BDC Boost seems to be the correct option to increase the modularity without loosing efficiency. This converter could control the voltage at the input of the TPDAB allowing a better performance, boost the voltage to reduce the current in the primary avoiding parallel semiconductors and reducing the needed Transformer ratio. Furthermore BDC Boost is easy to implement an interleaving method.

In conclusion, making a double stage of BDC Boost and TPDAB will solve problems of high current, variable input voltage and parallel switch-devices options.

Chapter 3

Project Description

To combine different battery modules together the proposed project presents a modular converter structure. The project consists in several battery pack connected to a 400 V bus through a DC/DC converter. Figure 3-1 shows the structure of the project.
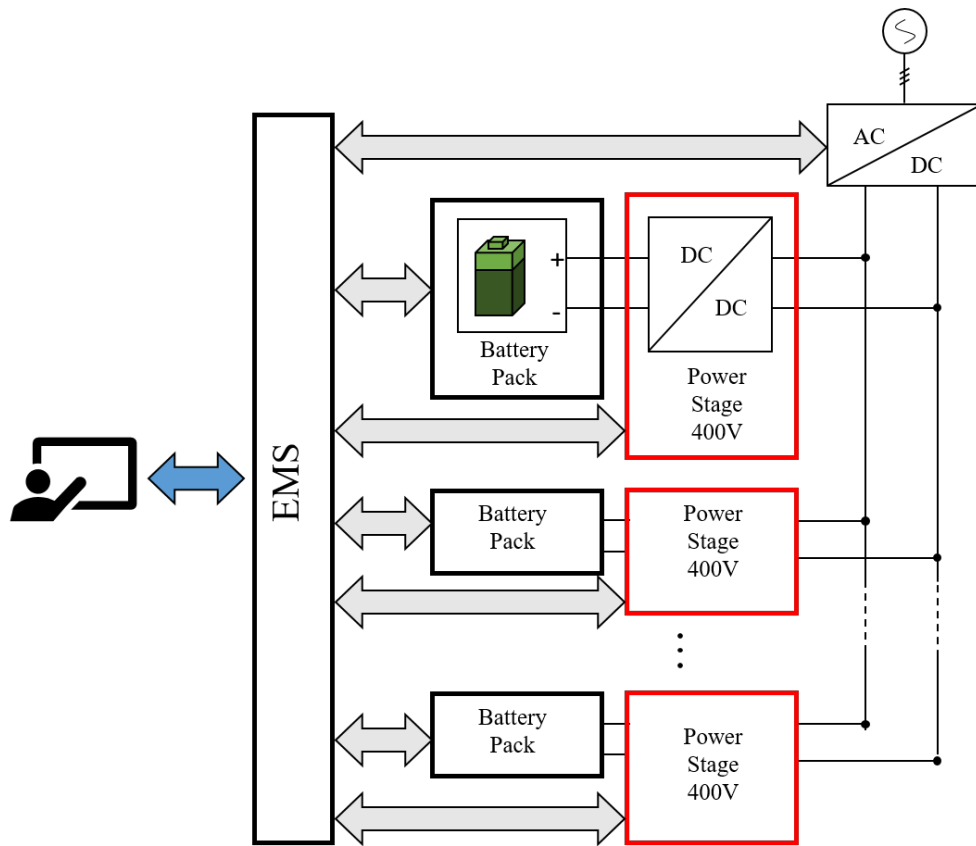
Figure 3-1: Overall Project Structure.

Modules follows a master-slave configuration where the master is a control board (EMS) that monitory each module, sets the power flow from the batteries and send information to a display. This configuration allows power exchange between modules being possible an active equalization between modules.

This master thesis is focused in the developed of the power stage 400V, show in red at figure 3-1. In order to determine the operation range and power limitations, battery pack specifications and configuration are previously studied, both the hold module as the cells in this module.

3.1   Battery Pack 48V

The battery module consists in 15 cells in series with a Battery Manage System (BMS) that measure the voltage of the cells and send the information to the EMS. Also it controls a passive equalizer system that maintain the voltage of cells in same levels. For these cells, in prismatic packaging, specifications are collected in table 3.1.
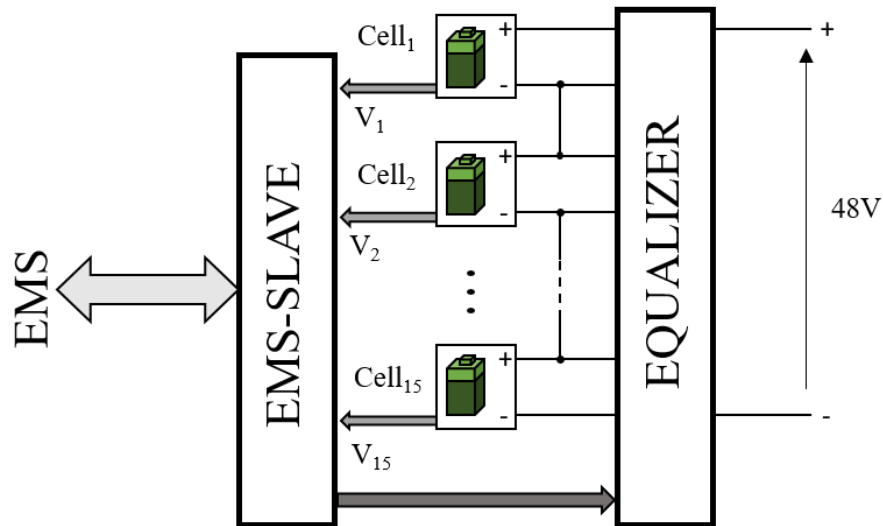
Figure 3-2: Battery Pack 48V structure.

Table 3.1: Battery Pack Module Characteristics

Parameter	Value	Unity
Minimum Voltage	41	V
Maximum Voltage	53	V
Nominal Voltage	48	V
Nominal Capacity	180	V
Nominal Current (Discharge)	180 (1C)	A
Maximum discharge (3 min)	360 (2C)	A
Peak current discharge (10 sec)	540 (3C)	A
Rated Power	18	kW
Recommended Charge Current	90	A

3.2   Power Stage 400V

The structure of this module, consists in a DC/DC with galvanic isolation, that boost the variable voltage of the battery to a stable 400 V bus. This power stage in controlled by a Control Board, that also includes a communication with the EMS. The module will be designed for the maximum power capability of the battery module: 18 kW.

In comparison with non-isolation systems, galvanic isolation includes the following advantages:

- Increase safety and reliability without a significant loss in operational efficiency [15].

- Under different voltage disturbances, the disturbance is not transferred from one side of the transformer to another, [16].

- Based on the DC/DC isolated topology, high power transfer can be transferred, as the three phase DAB [16].

- High gain voltage allowed through the transformer ratio design.

Another advantages of transformer in DC/DC are size, cost and losses can be reduced when the frequency of the transformer is increased. Therefore use of MOSFETs in this power stage will be translate in a high frequency transformer with a better efficiency

and less size. Also increasing the switching frequency will decrease the size of passive elements but will increase the switching losses.

In magnetic transformers its necessary ensure that the transformer does not saturate [17]. So they require DC blocking capacitors or control the current through the transformer. Also including a transformer is expensive and bigger than the passive components in a non-isolation system. However, if a high frequency transformer is chosen the impact in costs is reduce and all advantages of galvanic isolation are achieved.

As is commented in Chapter 2.2.3 the better implementation that allows previous requirements will be the double stage, being the overall topology presented in Figure 3-3. It consist in a three interleaved boost converter and a TPDAB. Following chapter will study the design of this topology.
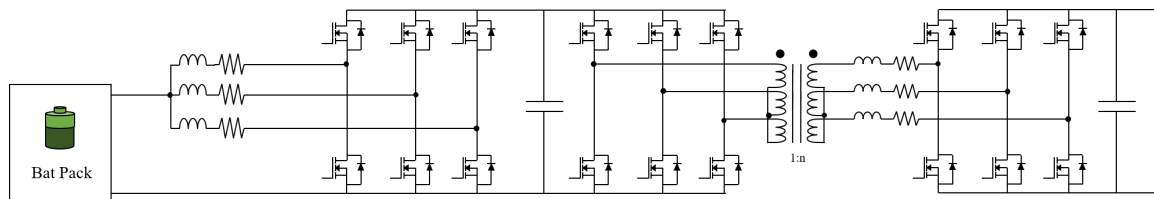
Figure 3-3: Proposed Double Stage Topology

Chapter 4

Design of the Power Stage

Requirements of high efficiency, high boost ratio, high reliability, and specifications of the Li-ion battery, the topology of the modular converter must has the capability of be connected in parallel with another modules and manage huge current in the battery with the lowest current ripple possible.

The proposed DC/DC converter of the 48/400 power stage consists in a double stage topology, presented in the previous chapter. The double stage is formed by two different double DC/DC converter: bidirectional boost converter and a three phase DAB, that provides galvanic isolation. Figure 4-1 shows the structure of the power stage divided in two main blocks: Stage 1 and Stage 2. The first stage boost the voltage of the battery to 115 V in order to reduce the transformer ratio and current through the primary of the TPDAB.
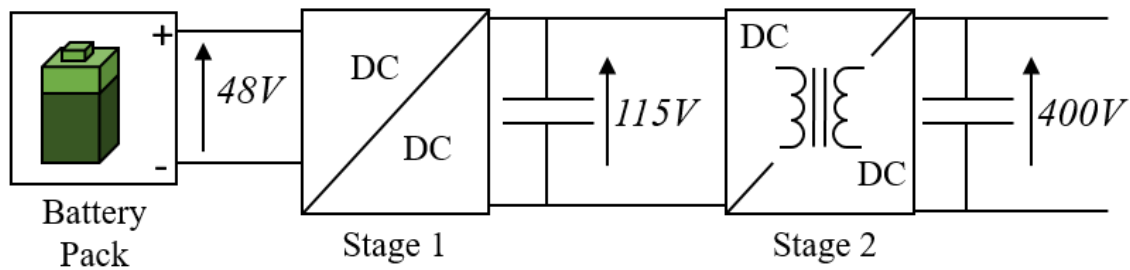
Figure 4-1: Proposed power converter: Double Stage.

4.1 Stage 1: Interleaved Bidirectional Converter

To avoid parallel semiconductors, ripple problems, reduce the voltage in the primary and control the input variable voltage of the battery pack, first stage used an interleaved BDC Boost. An interleaved converter consists of several identical converters connected in parallel [18]. Every interleaved leg is controlled by signals with the same duty ratio and different phase shift. In this case, the interleaving consists on three parallel BDC converters with a carry signal phase shifted 120 degrees, reducing the size of the inductors and current ripple at the input of the battery. Figure 4-2 shows the proposed topology for the stage 1, where each leg has the same inductor value (L_{INT}) and parasitic resistor (R_{INT}), with 6 semiconductors (M_x) and a output capacitor (C_{int}).

To design the passive components and select switches, specifications have been attached in Table 4.1. Frequency is selected as the trade of switching losses and conduction losses keeping both at the same levels.

Table 4.1: Interleaved Stage Specifications

Parameter	Symbol	Value	Unit
Battery Voltage	V_{bat}	53-41	V
Primary Capacitor Voltage	V_{pDC}	115	V
Maximum Battery Current (Discharge)	i_{bat}	440	A
Switching Frequency	Fhz_{sw}	20	kH
Battery Current Ripple	ΔI_{bat}	1	%

4.1.1 Inductor Design

In boost converters the current ripple is defined as equation 4.1.

$$\Delta I_{bat} = \frac{V_{bat}D}{L \cdot Fhz_{sw}} \tag{4.1}$$

Where D is the duty ratio and ΔI_{bat} the current ripple. In BDC converters the duty ratio is defined as equation 4.2, [19].
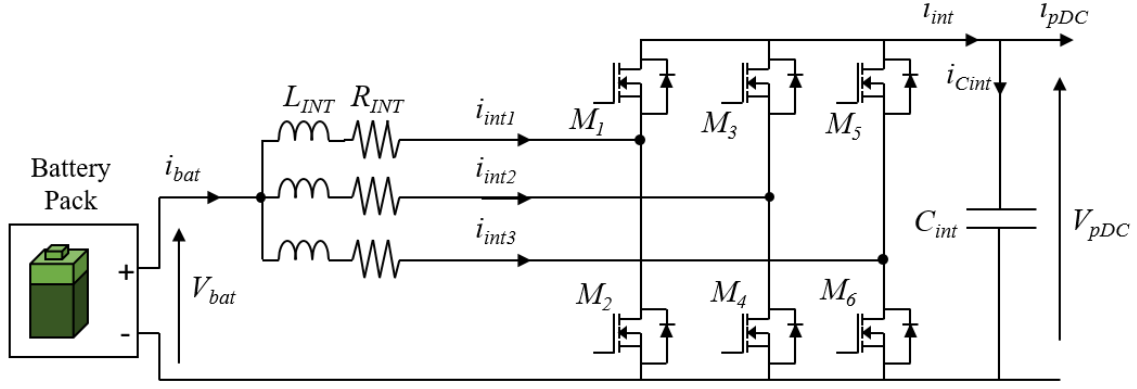
Figure 4-2: Interleaved Bidirectional Boost Converter.

$$\frac{V_{pDC}}{V_{bat}} = \frac{1}{1-D} \rightarrow D = \frac{V_{pDC} - V_{bat}}{V_{pDC}} = \frac{115 - 48}{115} = 0.5826 \qquad (4.2)$$

Rewriting equation 4.1 and knowing that the current of one leg is three times less the current in the battery, L_{int} can be calculated with equation 4.3.

$$L_i nt = \frac{1}{3} \frac{V_{bat}D}{Fhz_{sw}\Delta I_{bat}} = \frac{1}{3} \frac{48 \cdot 0.5826}{20 \cdot 10^3 \cdot 0.01 \cdot 440} = 91.83 \ \mu H \qquad (4.3)$$

Figure 4-3 shows the current ripple in steady state for the proposed inductor in each leg of the interleaved. The sum at each instant of this signals is the current through battery side. Then Figure 4-4 shows the evolution of the current in the battery. As is shown the ripple of 14 amps in the interleaved legs is reduced to 1 amp with the proposed interleaved structure. In addition, the current supported for each MOSFET is also reduced to 153 Amps,

4.1.2 Interleaved Capacitor Design

To select the capacitor used in the DC link, two types of capacitors have been analysed: electrolytic and film capacitor. Electrolytic capacitors are the typical option for DC link applications due its high capacitance. However, electrolytic capacitors are delimited by the maximum current ripple that they can manage, being typical values between 30 A_{rms}. Following the procedure presented in [20], with the assumption
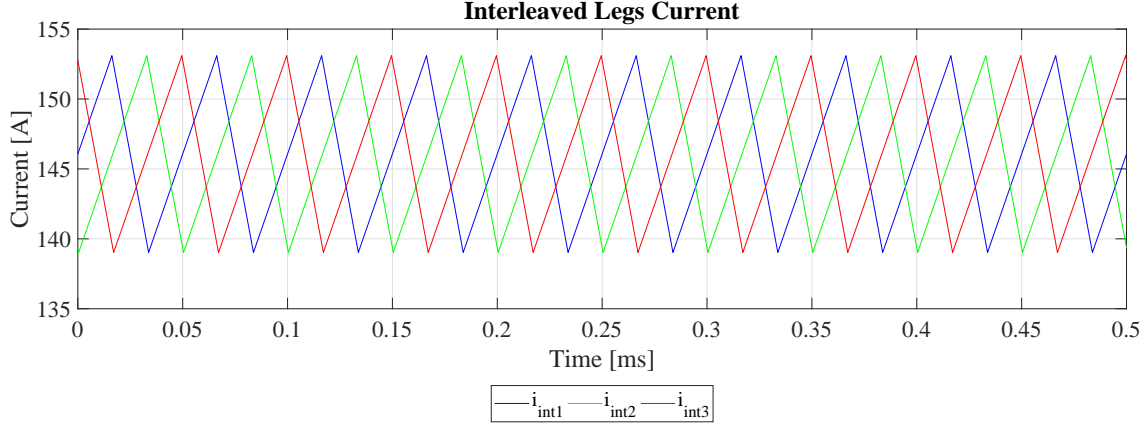
Figure 4-3: Interleaved current.
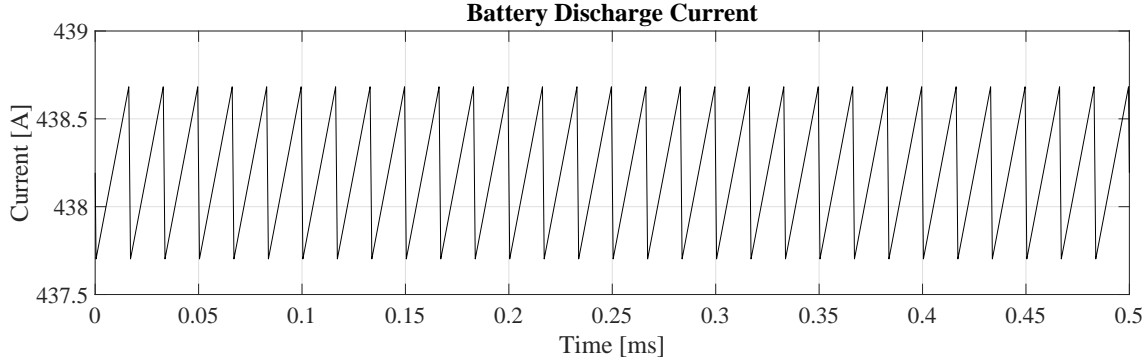
Figure 4-4: Battery current ripple.

of not delimited current ripples for electrolytic capacitor, the estimated values for a voltage ripple of 5% for a maximum voltage at V_{pDC} of 120V the needed capacitance are 17.015 μF.

To select the minimum number of electrolytic capacitors needed to withstand the maximum current Figure 4-5 shows the current and voltage behaviour in C_{int} during the same discharge process that in the previous case.

From Figure 4-5 the maximum current that capacitor must withstand is 149.475 A. For switching frequencies higher than 10 kHz the ripple factor of electrolytic capacitors is 1.35, so the number of parallel electrolytic capacitors is calculated with equation 4.4.

$$n_{Cparallel} = \frac{I_{max}}{I_{Cadmissible}} = \frac{149.475 \cdot 1.01}{(149.475 \cdot 0.01) \cdot 1.35} = 8 \; Capacitors \qquad (4.4)$$

With a film capacitor, maximum A_{rms} of 149.475A can be supported adding only two capacitors. As is presented, using film capacitors the number of capacitors is reduced from 8 to 2, total capacitance of 1200 μF. Implies a compact interleaved DC link and a very stable V_{pDC} voltage as Figure 4-5 shows.
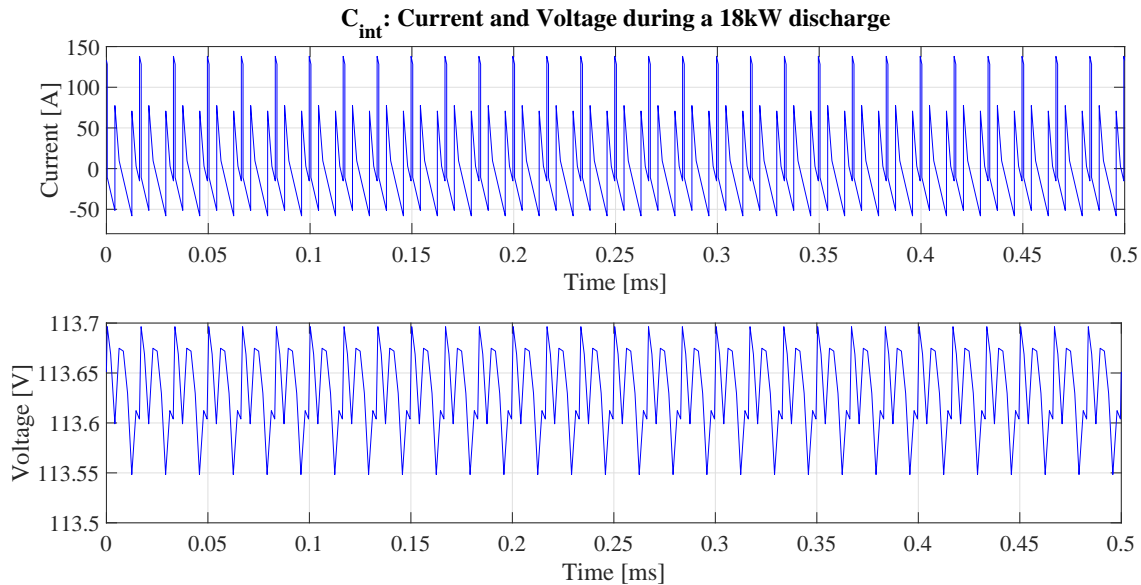
Figure 4-5: C_{int} current and voltage steady state analysis.

4.1.3   Semiconductor Selection

Semiconductor devices must operate with low voltage and high current in the worst case. In steady state current for interleaved semiconductors are presented in Figure 4-6. The study options for semiconductors are: IGBTs, MOSFETs and Silicon Carbide devices. Despite IGBTs presents high voltage and high current capabilities are dismissed due to the losses at high switching frequency in this devices. A high frequency switching with less losses can be obtained with Silicon Carbide devices but the costs of one this module is too expensive for this application. Then the proposed option is MOSFETs semiconductor due to the low cost in comparison with Silicon Carbide and high switching frequency with less losses than IGBTs. The main drawback is the maximum current and voltage that can withstand. The voltage in this application is not a problem, but the high current can suppose a problem, but thanks

to the interleaved strategy the current is three time lower than the nominal and this type of device can be implemented.

Voltage that MOSFETs will support is the voltage at the V_{pDC}, presented in Figure 4-5. Current through each device is shown in Figure 4-6 the maximum current peak is 154 amps. The selected MOSFET has a maximum current chip of 360A and maximum voltage of 150V.
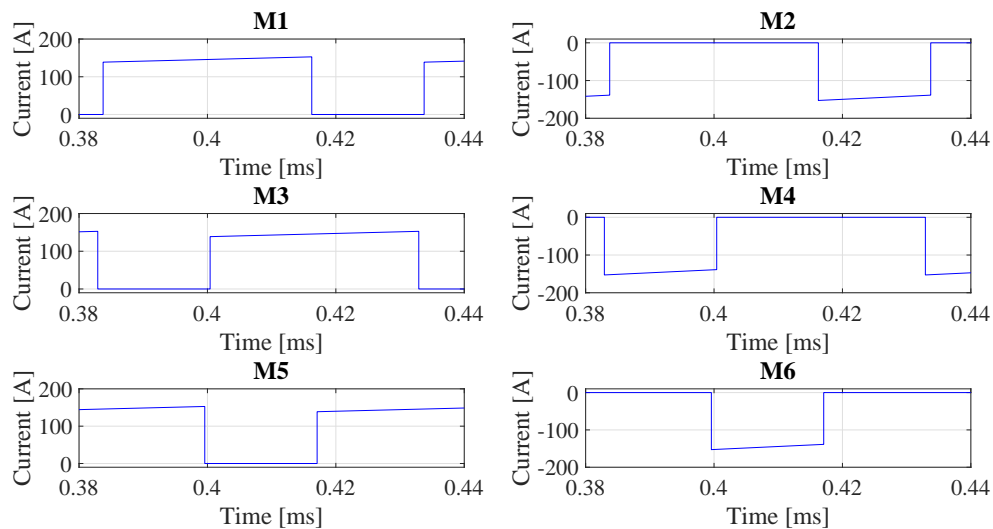
Figure 4-6: Current across interleaved semiconductor during one cycle for maximum power discharge.

4.2   Stage 2: Three Phase Dual Active Bridge

The main function of the TPDAB is adapt the voltage to 400 volts, and demand or supply power to the bus. As commented in Chapter 2, the TPDAB reduces the peak current through the switches, the ripple in the DC current and therefore losses, but also increase the number of elements and cost.

In Figure 4-7 a detailed model of the proposed stage two is presented. This topology consists in two three phase inverters connected to a high frequency transformer, where the equivalent series inductor determines the maximum power transfer that can be achieved by the system. Requirements for this stage are attached in Table 4.2.
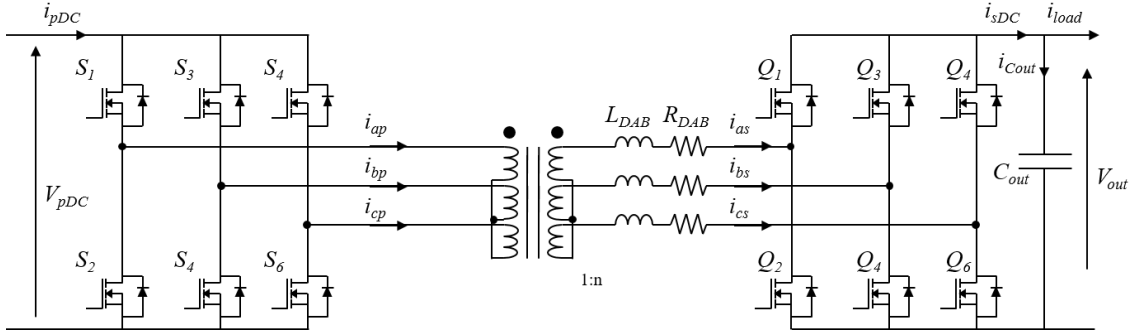
Figure 4-7: Proposed TPDAB schematic.

Table 4.2: TPDAB Stage Specifications

Parameter	Symbol	Value	Unit
Output Voltage	V_{out}	400	V
Input Voltage	V_{in}	115	V
Maximum Power Transfer	P_{max}	18	kW
Output Voltage ripple	ΔV	10	%
Switching Frequency	F_{sw}	20	kHz
Transformer Ratio	n	115/400	

4.2.1 Transformer & Inductor Design

In this type of topology the maximum power transfer is determined by the inductor and the power amount is determined by the phase shift between the low voltage active bridge and the high voltage bridge. From the study of [9], the equations that define the system, is the relation between current and voltage drop across an inductor. Figure 4-8 shows the circuit to study.
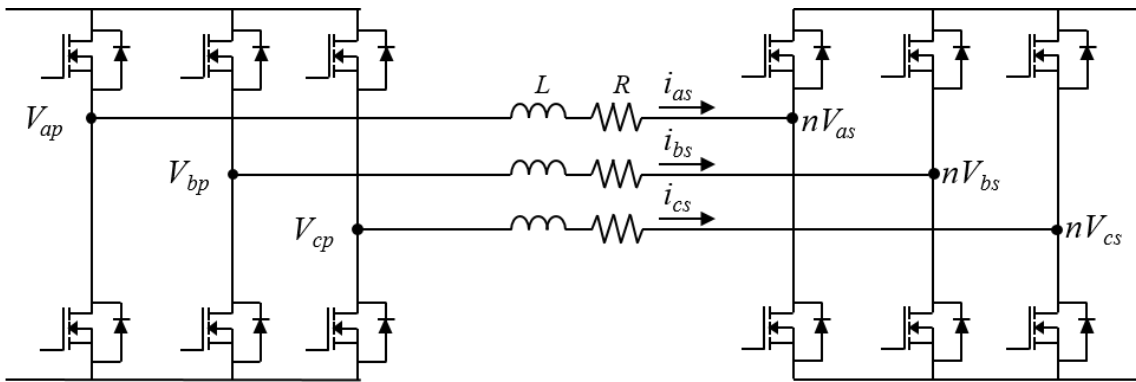
Figure 4-8: TPDAB circuit.

Without considered the parasitic resistor (R), the current through each phase can

41

be written as equation 4.5, refer to the primary side.

$$L\frac{di_{as}}{dt} = nV_{as}(t) - V_{ap}(t) \tag{4.5}$$

Following [9] of the power flow in a TPDAB, power flow through the inductor in a TPDAB can be expressed as equation 4.6. Where ϕ is the phase shift between the primary side and the secondary side.

$$P_{flow} = \frac{V_{pDC}^2}{2\pi F_{sw}L}d\phi(\frac{2}{3} - \frac{\phi}{2\pi}); \ 0 \le \phi \le \pi/3$$
$$P_{flow} = \frac{V_{pDC}^2}{2piF_{sw}L}d(\phi - \frac{\phi^2}{\pi} - \frac{\pi}{18}); \ \pi/3 \le \phi \le 2\pi/3 \tag{4.6}$$

Where d is nV_{sDC}/V_{pDC}. From this equations the minimum inductor to achieve a maximum power flow of 18 kW is calculated for all the possible phase shifted. Then the evolution for the inductor for ϕ from 0 to $2\pi/3$ is represented in Figure 4-9. As it shown, the maximum inductor that can achieve this power transfer is 3.572 μH at 90°. This value will be the optimal one because, higher values of inductors cannot reach this maximum power transfer and lower inductors could reach higher power values that implies oversize with not useful operation zones and increasing the risk to operate with higher current in the semiconductors.

Then with this value of equivalent inductor the power evolution over all phase shift range [-120, 120] is represented in Figure 4-10.

Table 4.3: Transformer Specifications

Parameter	Value	Unit
Secondary Voltage	400	V
Primary Voltage	115	V
Maximum Power	18	kVA
Frequency	20	kHz
Transformer Ratio	115/400	
Primary Inductor	1.7860	μH
Primary Resistor	3	mΩ
Secondary Inductor	21.6076	μH
Secondary Resistor	3	mΩ
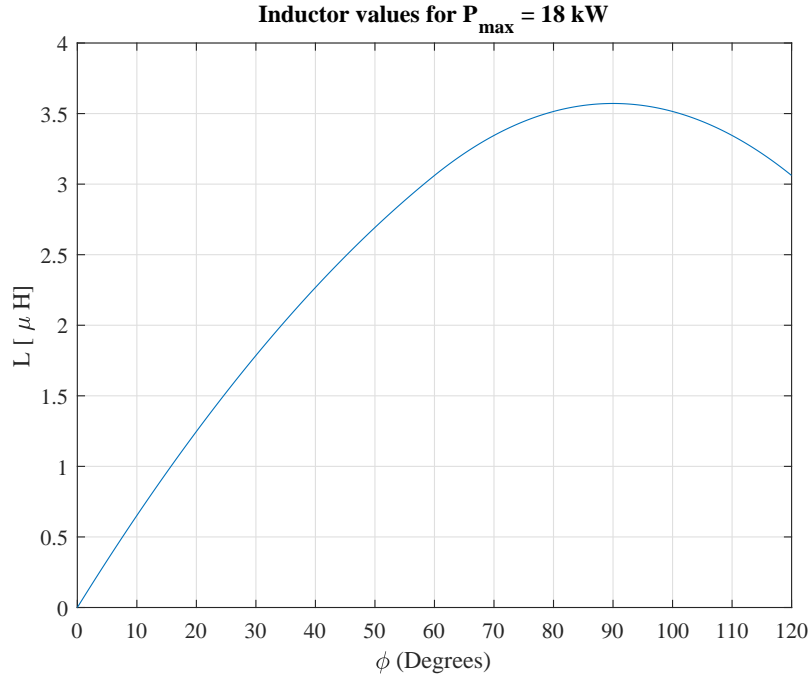
Figure 4-9: Inductor values per phase shift.
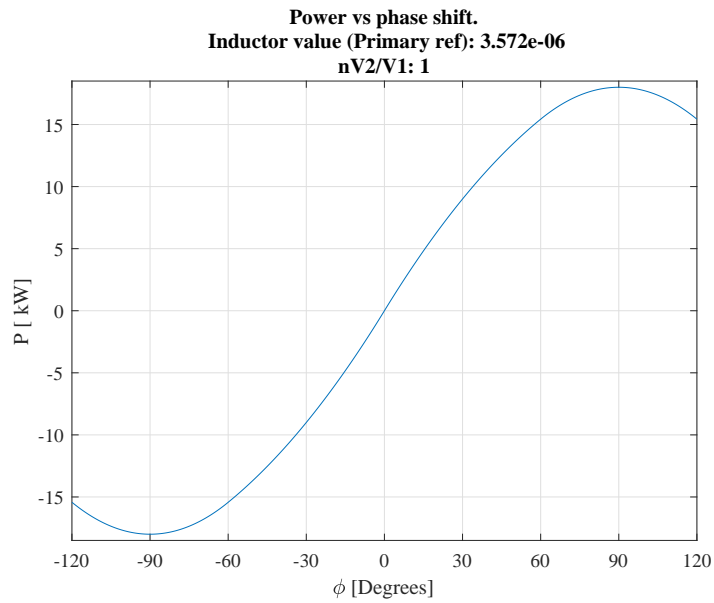
Figure 4-10: Power flow per phase shift.

Is impossible to obtain a transformer with one inductor at the primary side and a 0 inductance at the secondary. For the analysis of the converter, the inductance value of 3.572 μH is divided in both transformer sides: primary series inductor will

be the half of this value: 1.7860 μH, and the secondary will be the other half refereed to the secondary: 21.6076 μ H.

As in the case of the stage 1, the steady state analysis is done with the presented parameters for the transformer. Figure 4-11 shows current and voltage at the primary side for the three phases. Figure 4-12 shows current and voltage at the secondary. This results shows the availability of the current transformer.
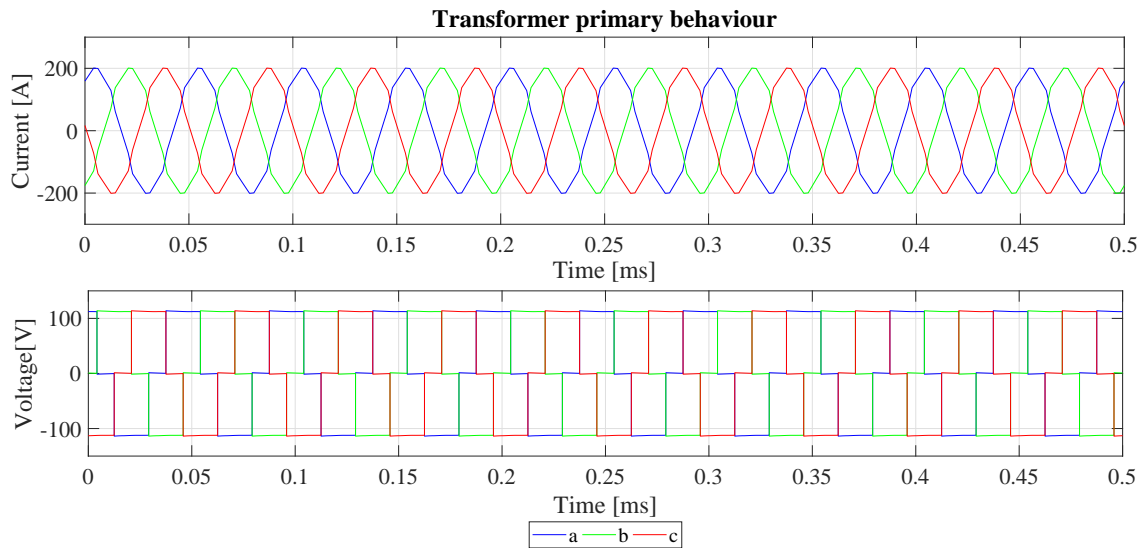
Figure 4-11: Transformer primary current and voltage.

4.2.2   High Voltage Capacitor Design

As in the case of the interleaved capacitor design, a film capacitor and an electrolytic capacitor are studied. Current and voltage are observed for the maximum discharge load and represented in Figure 4-13. Then using same equations as 4.4 a maximum current of 45, the minimum number of electrolytic capacitors needed will be 7.407, that means 8 capacitors again. Meanwhile using the same film capacitor than the interleaving case, only one capacitor could be used. The film capacitor allows a very stable bus with a ripple less than 60 mV.
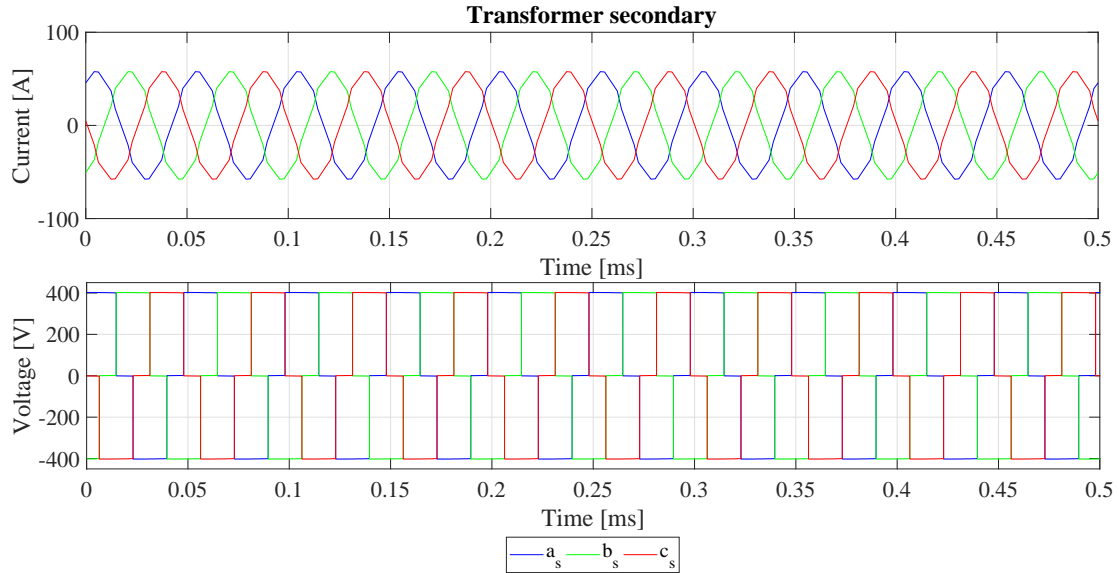
Figure 4-12: Transformer secondary current and voltage.

4.2.3 Semiconductor Selection

The type of the semiconductor chose is MOSFET for the same reasons that explained in previous section. In this case there are two different voltage a current level at the semiconductors. The primary side with low voltage and huge current and the secondary side with high voltage and reduced current. In order to select the proper
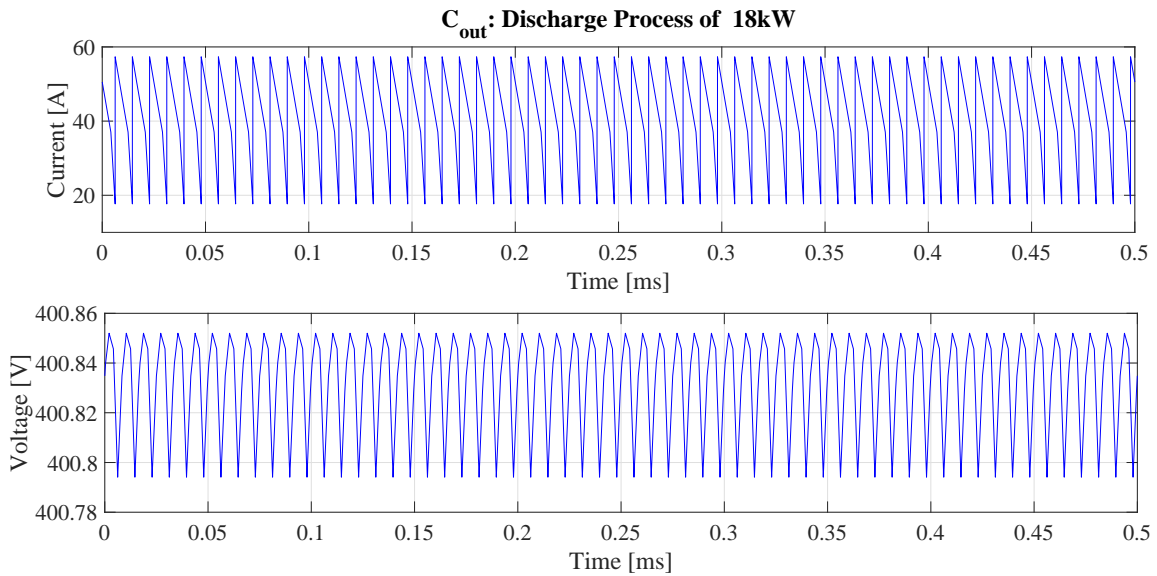
Figure 4-13: Output capacitor current and voltage for a 18kW discharge process.

45

device the study of both is done separately.

Low Voltage MOSFETs

As in the case of the interleaved this MOSFETs must withstand a DC link voltage of 115V and the current through the primary side. Figure 4-14 shows the current during one cycle through each MOSFET in steady state. Also the phase shift and complementary commutation can be appreciated.
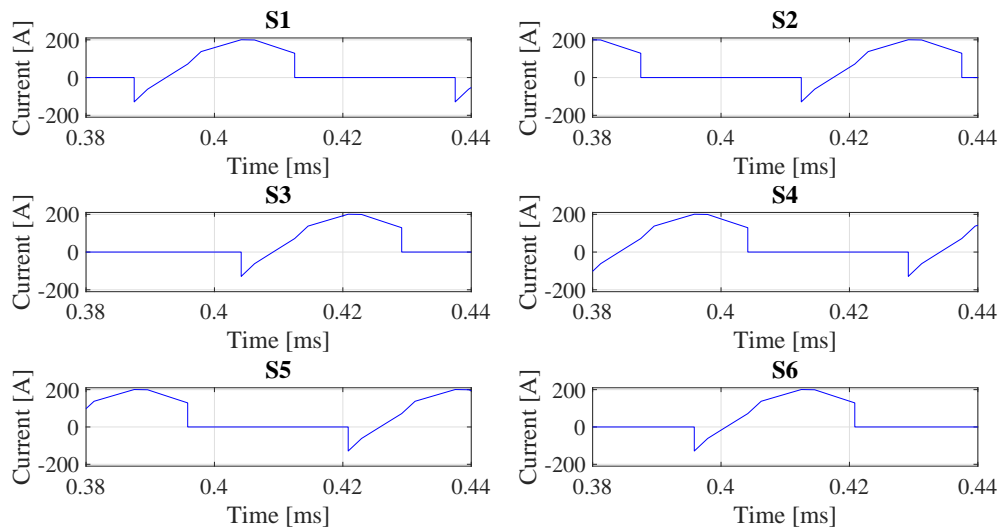
Figure 4-14: Low voltage MOSFETs Current.

With a peak current of 200 A and 115V in the primary, the same MOSFETs than the interleaved option are chosen, they can operate at this current and voltage level and the low on resistance will reduce the losses through the semiconductors.

High Voltage MOSFETs

As the previous case Figure 4-15 shows the current in steady state during one cycle for a 18 kW discharge process. As graph shows it must withsantd current of 58A. The maximum voltage now is the secondary voltage of 400V. The proposed MOSFET withstand this value, so is different for the other cases.
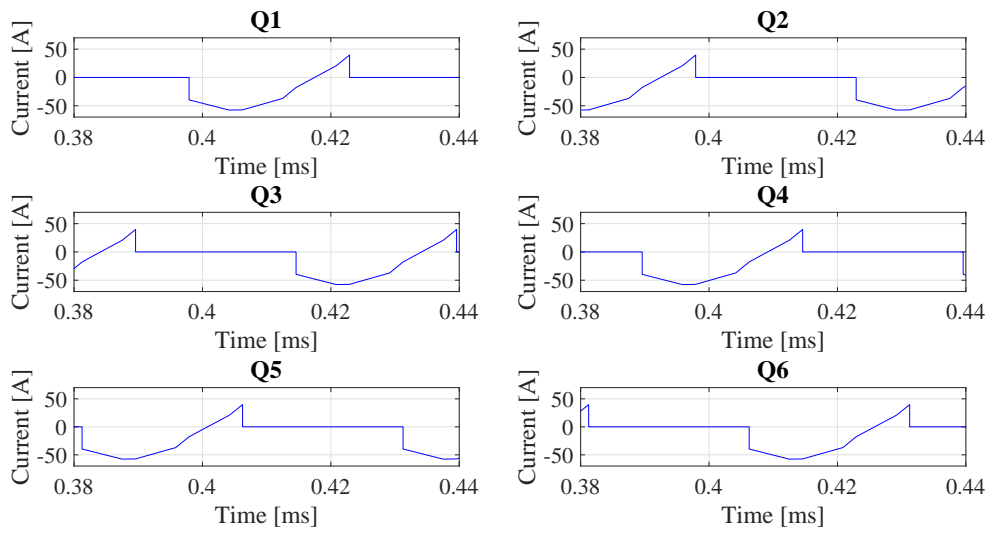
Figure 4-15: High voltage MOSFETs Current.

Chapter 5

Prototype Design

The previous selection of the key components of the proposed topology is not enough to build a functional prototype. This prototype must be designed to be mounted in a 580 x 440 x 340 mm case (wide x long x high). Walls or this case will have a thickness of 0.2 mm.

5.1 MOSFETs Driver

The first elemet to design mechanical elements will be the driver board. Every MOSFET need some device that adapt the signal from the control board to the gate levels. With a commercial driver that can control two gates with signal from 15V to -0.5V, each leg is controlled. The main disadvantage of this device is that it cannot be placed directly over the MOSFET so its necessary an interface board to send signal to the module. This board also must include all the necessary external circuits to provide active clamping, over-current protection and signal level adapters.

Then a first board prototype for two devices is presented. Since this driver can be used for all the devices of this system this interface prototype can be implemented as modular board, the same for all switches, increasing the modularity of the design.

5.2 Heat-sink selection

One critical factor in a power stage is the heat dissipation. Semiconductor devices generates heat during the working process, if this heat is not removed devices will fail.

In order to solve this problem the selection of a good dissipation system must be study. In order to know which is the stress of this devices, the system is simulated in PLECs to know losses in the devices during the nominal power transfer of the interleaved. During normal operation losses in the switches are 26.98,13.27,21.68 W for each interleaved, high voltage bridge and low voltage bridge devices, respectively.

With this values and considering a maximum ambient temperature of 40°C the heat-sink thermal resistor is designed to not over-rate the 90°C in the MOSFETs. Then three options are take into account:

- Option 1: All MOSFETs in the same device. This option will allow a compact design and only one heat-sink will be needed. Also the thermal resistor of this heat-sink should be lower, because it has to dissipate more heat.

- Option 2:Low Voltage side and stage 1 devices in one heat-sink and high voltage side in another heat-sink. This option allows put one heat-sink in one side of the transformer and separating in the other side the high voltage switches creating a more modular system and using higher thermal resistors, but now two heat-sink are needed.

- Option 3:Stage, high and low voltage sides each one in one heat-sink. Increase the thermal resistor, but three heat-sinks are used and its needed more space in the case.

Then to calculate the thermal resistor equation 5.1 is used.

$$R_{HS}^{th} = \frac{T^{limit} - R_{device}^{th} P_{device}^{loss} - T^{amb}}{P_{total}^{loss}} \qquad (5.1)$$

Where R_{HS}^{th} is the thermal resistance of the heat-sink, R_{device}^{th} is thermal resistance of the device, P_{device}^{loss} is the power losses in the device, T^{limit} the maximum allowed

temperature in the MOSFET, T^{amb} maximum ambient temperature and P_{total}^{loss} is the maximum power that the heat-sink will dissipate. From this equation the needed thermal resistor per option and per device is attached in Table 5.1. From this table is possible notice that the thermal resistor more restrictive is the stage one. So for the first option the maximum admissible value should be 0.121 °C/W, for the second option will be 0.154°C/W and 0.627°C/W. For the third option the ones attached in the table are the resistor of each heat-sink. The equivalent thermal circuit is shown in Figure 5-1, where 'D' can be 'M', interleaved, 'S', low voltage and 'Q', high voltage devices. The number of devices dependes the chosen option, R_{JC}, R_{CS} is set base on the data of the correspond device and P_{loss} based in the values calculated before.
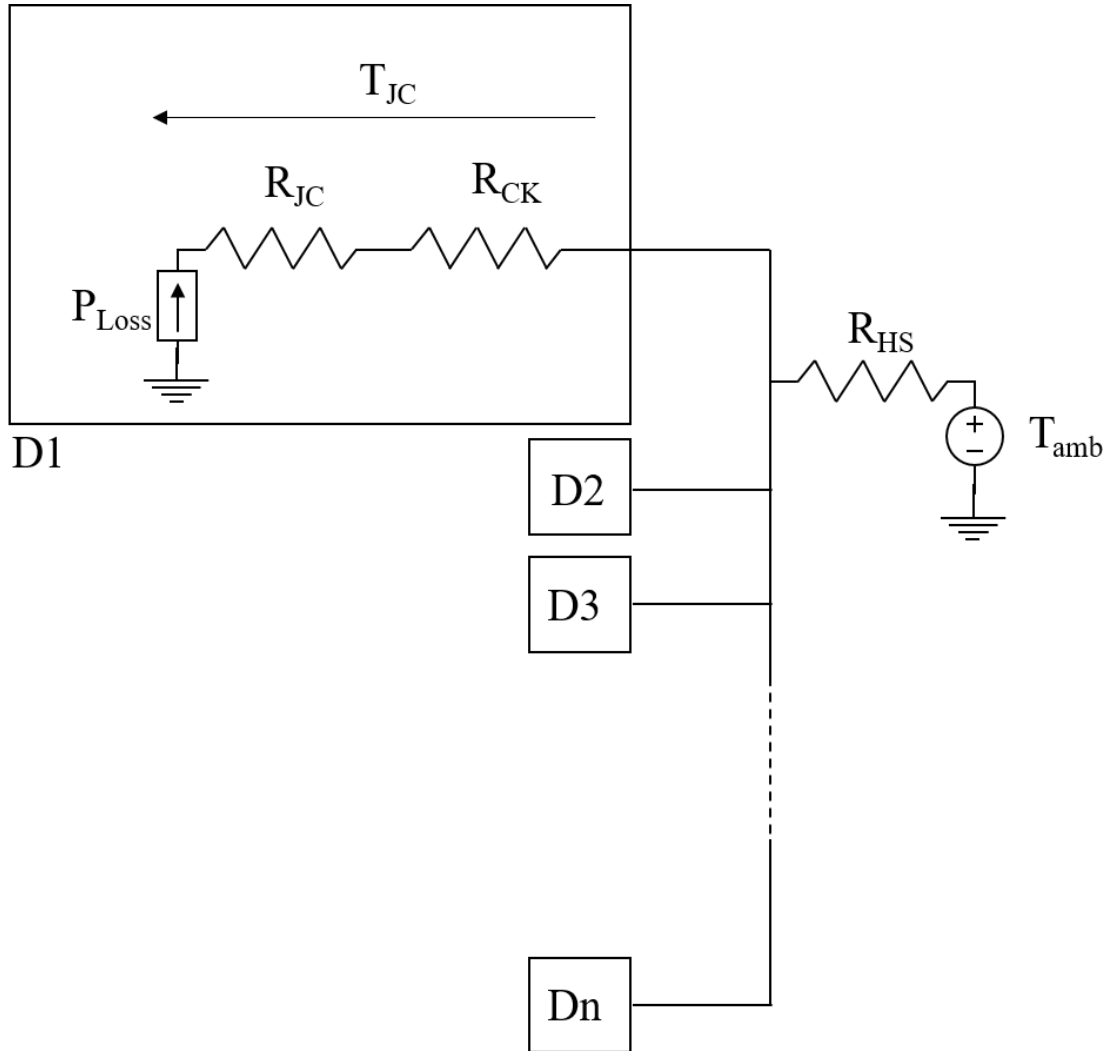

Figure 5-1: Equivalent thermal scheme.

Table 5.1: Possible Thermal Resistors in (°C/W)

Device	Option 1	Option 2	Option 3
Stage 1	0.121	0.154	0.277
Stage 2 (LV)	0.123	0.157	0.353
Stage 2 (VV)	0.134	0.627	0.627

The third option has a thermal resistance that can be achieved with active thermal dissipation cooling with air. This option will reduce the surface of the heat-sink with a more compact design than other options. For that reason this option is the chosen one for the heat-sink. Dimension selected must allow put all devices over the thermal heat-sink. For that reason a with a heat-sink with a thermal resistor of 0.0674°C/W, is used.

5.2.1   Heat-sink & driver mount

Considering that capacitors, DC link and driver will be put over this element, the best option is to put the DC link over one of the wall side of the case. Then Figure 5-2 shows the distribution in the case of the heat-sink and semiconductors over the heat-sink.

Over this elements, driver boards are connected as Figure 5-3 shows. Where each block represents the interleaved, low voltage and hide voltage power switches blocks.

5.3   DC Link & phase design

5.3.1   DC Link design

With dimensions of the Heat-sink and semiconductors distribution, the DC Link is designed to connect devices to the Capacitors, put the voltage sensors and connect the terminals to the output. To connect devices to the DC link a brass bars are used. With the needed separations from the driver board to allow the phase plates could be connected to semiconductors and leave a enough space to place the drivers. To achieve this goal, brass will have a length of 70 mm.
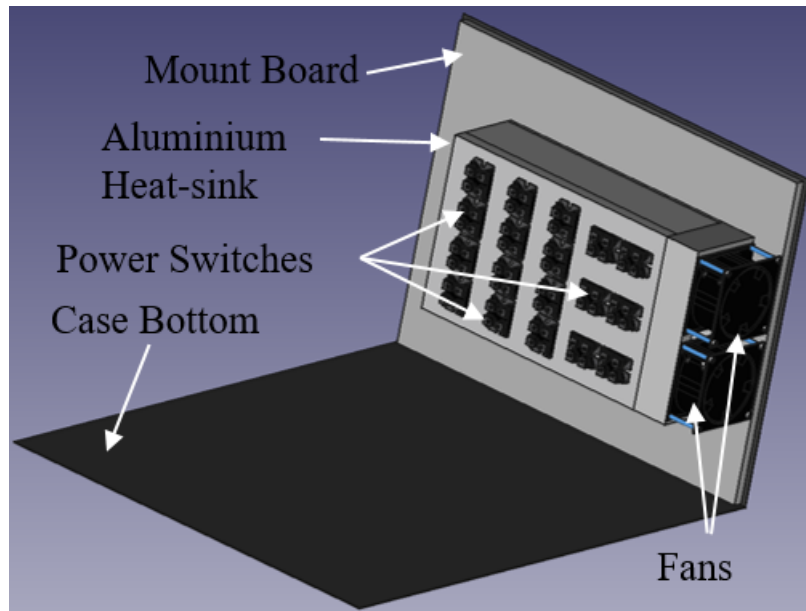
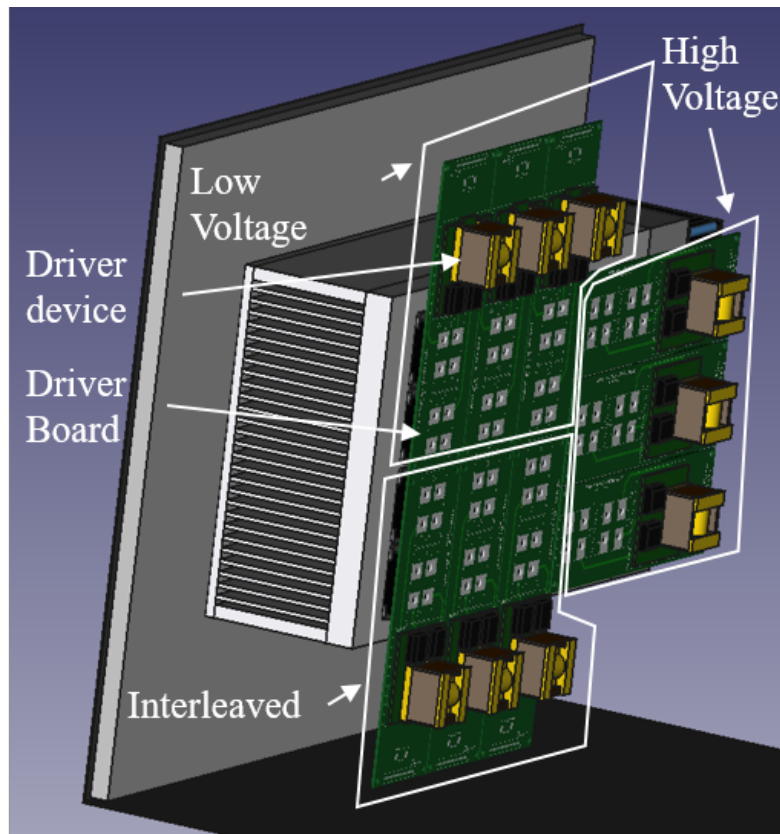Figure 5-2: Heat-sink and semiconductors mount, 3-D model.

Figure 5-3: Driver adapted board and block division, 3-D model.

With the length and the material the needed section of the brass bar will be calculated with equation 5.2.Where the admissible voltage drop (AV) will be 25mV.

$$Section = \frac{2\rho_{Brass}I_{max}length}{AV} = \frac{26.2\mu\Omega cm \; 200A \; 7cm}{25mV} = 1.915cm^2 \tag{5.2}$$

Then the radius of the bar will be 4,7 mm, and the same metric than the one used by the semiconductors is used for the screw part M4 with a length of 8,4 mm.

Copper plates are designed to connect all the brass bars and all capacitors. So the size of this plates will be the same with a high and length of 300 and 230 mm. The thickness of this plate is calculated base on the section for a maximum 200A. Using the table for copper for the DIN 43671, Table 5.2, the minumum length of the plate, taking into account there are holes for the brass bars, is 191.2 mm. The minimum section for a normalize current of 205 A is 40 mm, that implies a 0.3 mm of thickness, which results in 57.36 mm^2.

Also the DC plates has be connected to it correspond capacitor, so a cylinder of 12mm with a hole of 6 mm is connected to the copper plate through a drawing process. Since the DC link consist in 4 different pieces of copper, at different voltage levels, they are separated with a PVC plastic of 0.5 mm thickness. Those plates that are not connected with a determine bar, has a hole to let the bar and the nut pass without touch the plate, radius of 6.5 mm for the bars and 15 mm for the cylinders.

5.3.2 Phase plate design

With the previous configuration a plate must be connected to the medium point of this devices, so is designed to pass under the DC link and go through current sensor to the inductors and transformers. Then the connection until the current sensors will be a copper plate and the connection from current sensors to inductor and transformer will be done using flexible copper plates.

To connect phase plates to the DC link, the same brass bars are used, since requirements of current, screw metrics and admissible voltage are the same. Only change the length, but will be lower than the one used in the DC link so the voltage

drop will be even lower.

Phases for Low Voltage and Interleaved will be go under the DC link to the floor of the case. To avoid short-circuits between legs and add the possibility of an isolated support bar between them a space of 17mm is left between one leg and another. The driver device has a 27mm of high, so the phases are separated 30 mm from the board in order to not contact with the driver and be the most possible closed to the board. Then the length of the brass bars will be 30 and 47. For the case of the High voltage side, the plate go from the boards to the wall, and brass bars should be close as possible to the driver board with enough separation from the driver. So 30 mm of length are chosen as the interleaved case.

Plates has to avoid contact with the DC link brass bars. So they are designed to go in the space between board and board keeping a symmetrical distribution at the current sensor place. This space allows a 20 mm plate. In addition, these plates will be bended 90 degrees. Because the interleaved current will be measured in order to see how differences between real inductors affect the current ripple, these legs will be pass through a sensor current: LEM 510. So the length from the surface of the board mount to the phases of the interleaved will be at 35mm. And the low voltage plates will also at 35 mm from the another phase in the blended part. The same current sensor is used for the high voltage side, so the 35 mm are also used, but now they are mounted in the wall of the case.

Following the same procedure that in the case of the DC link copper plates, Table 5.2, so to withstand a 200 current they are designed for a section of 40 mm^2, so the thickness in this case is 2mm. Some holes of a radius of 3.5 mm for the places where the supports are connected are added, and a hole at the end of the plate of 3.5 mm is included to connect the flexible plates. Holes for the bars has the same radius that DC link bar holes.

5.3.3   Copper plates and Brass bars mount

The first step to mount copper plates is screw all screws and bars in the semiconductors, as is show in Figure 5-4. Then the plates for the interleaved and for the high

Table 5.2: Current base on section, DIN 43671

Section mm	Plates n°: 1
24	125
30	155
40	205
60	245
75	300
100	325

voltage side are placed, Figure 5-5. Over this plates the low voltage side plates are mounted, being complete the mount of the phase plates. All plates are attached to the bars using nuts.

Once the phases are mount the DC link plate is put over all. The DC link counts with 4 copper plates. The mount is done as Figure 5-7 shows. The procedure to mount it is the following

- 1: Mounting -115 volts plate.

- 2: Mounting Isolated PVC board.

- 3: Mounting +115 volts plate.

- 4: Mounting Isolated PVC board.

- 5: Mounting +400 volts plate.

- 6: Mounting Isolated PVC board.

- 7: Mounting -400 volts plate.

- 8: A voltage sensor board is mount using plastic pieces.

Once the DC link is mounted the final step is add the Capacitors over the up cilinders. This capacitors will be supported at the end of it body with a mounting board atached at the front wall, Figure 5-8.

Once the transformer and inductors will be made by the company they will be implemented in the free space over the capacitors. At the moment, with this configuration is possible check commutation, voltage and current stress over the presented module.
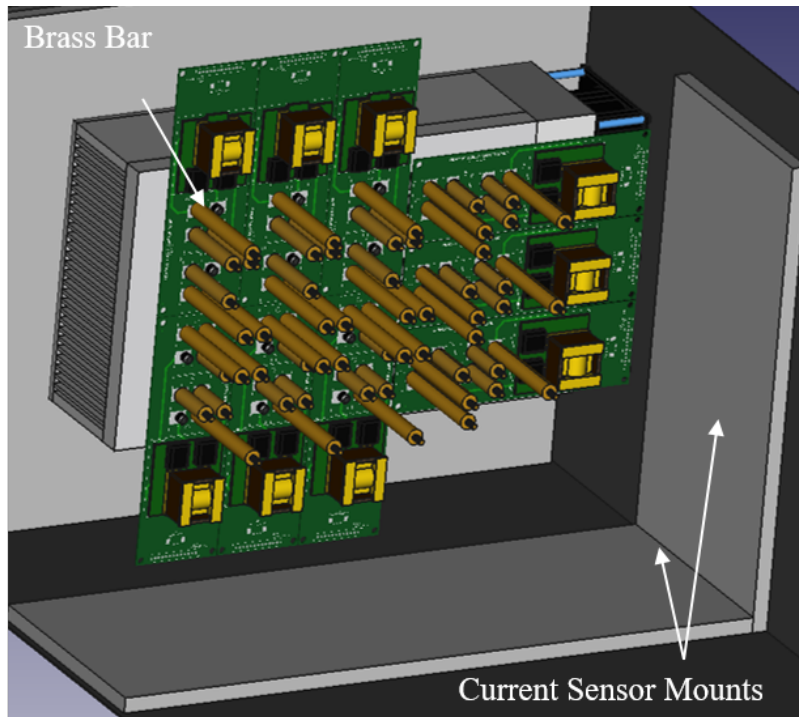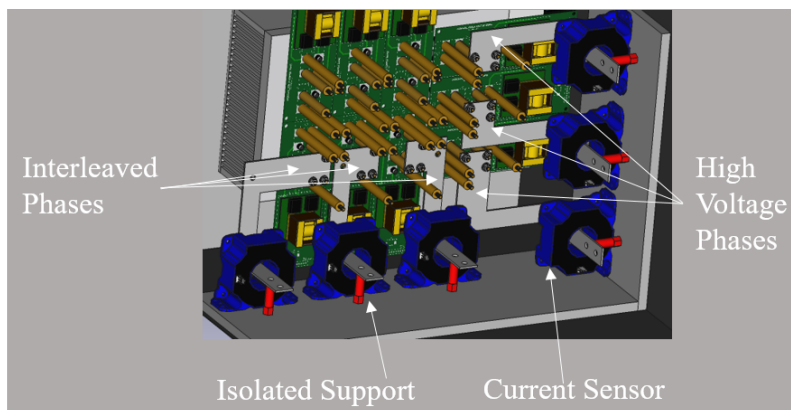

Figure 5-4: Brass bars mount, 3-D model.

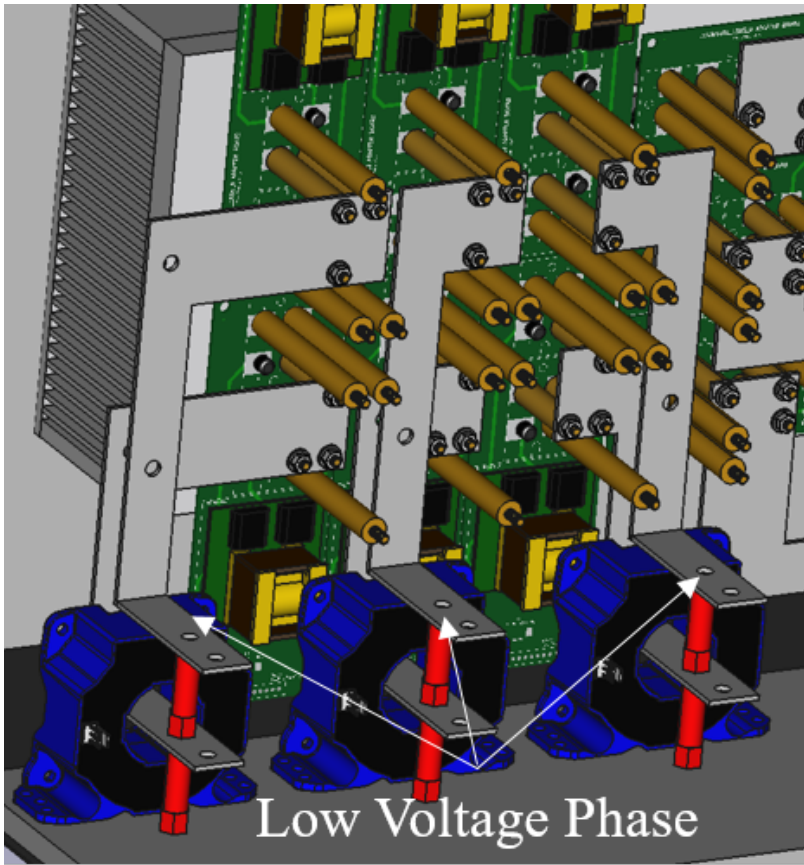Figure 5-5: Interleaved and high voltage plate mount, 3-D model.

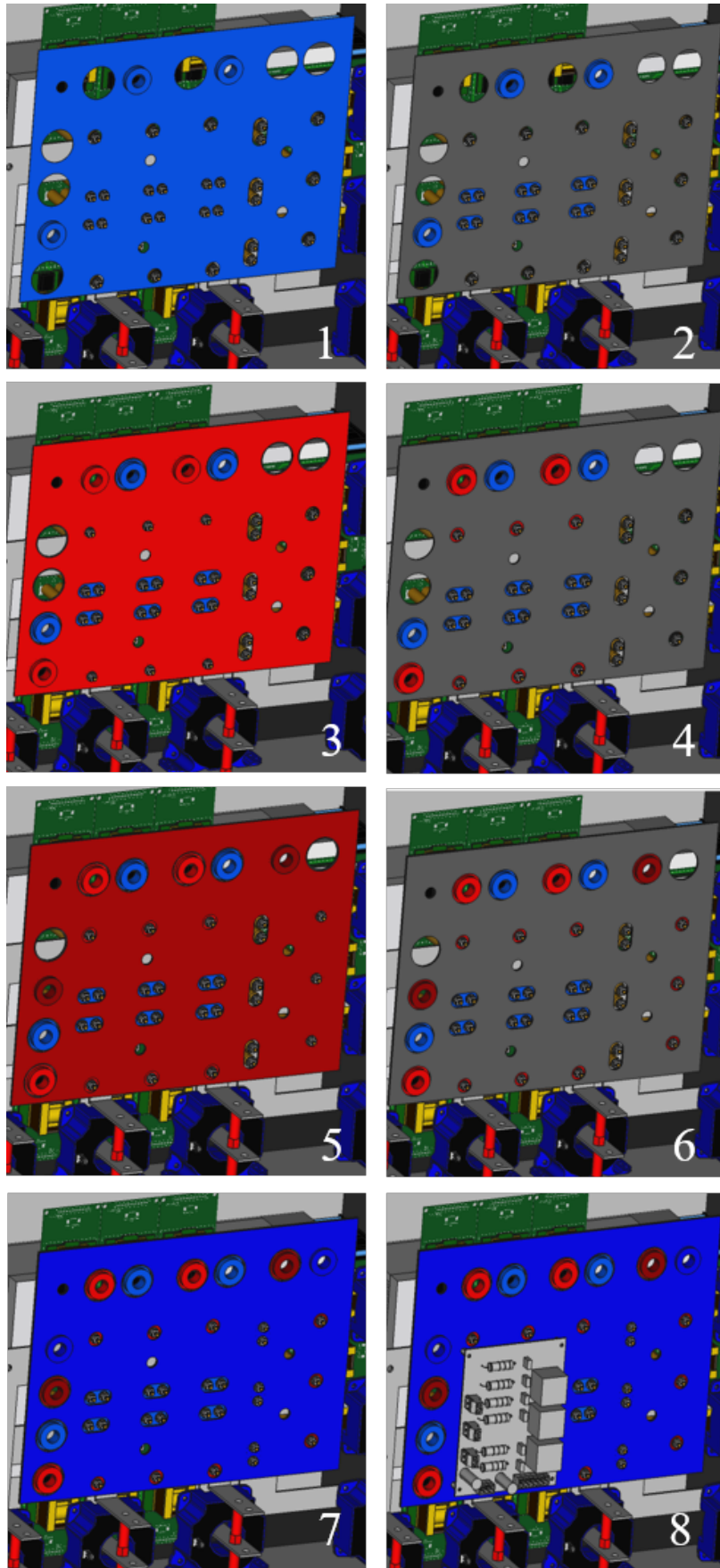Figure 5-6: Low voltage plate mount, 3-D model.

Figure 5-7: DC link mount, 3-D model.
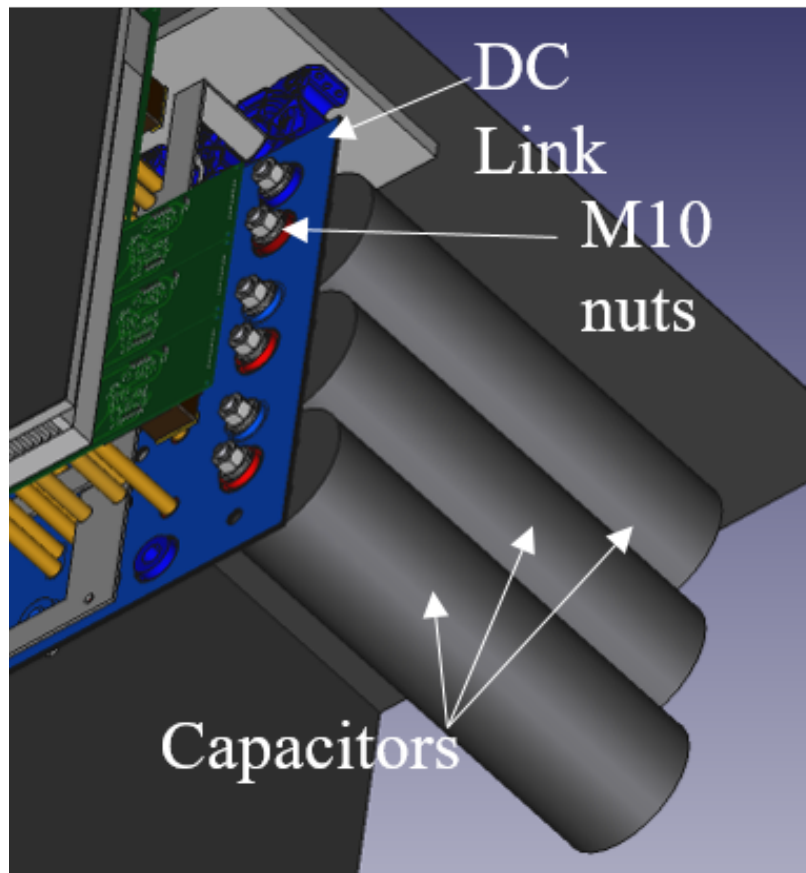
Figure 5-8: Capacitors mount, 3-D model.

Chapter 6

Control System

To test the proposed double stage, a simulation was implemented in simulink & PLECs. PLECs allows two different ways to carry a simulation: Standalone or Blockset. PLECS Standalone is an autonomous software package for time-domain simulation of power electronic systems [23]. It allows steady state simulations, thermal analysis and faster simulations, but control architectures are not implemented as PID controller or signal switches, but allows C-blocks that can be used to program a C code. PLECS Blockset is a unique tool for the fast simulation of power electronic circuits within the Simulink environment [23]. In this work is used to implement the topology in Simulink and control it.

6.1 Open Loop Study

The first open loop study was performance in Chapter 4 in order to determine semiconductors and passive components of the stage, so this section is focused in the thermal, analysis study and soft start transient implementation.

6.1.1 Thermal Analysis

A thermal analysis can be implemented in this program adding the curves attached in the datasheets of semiconductors. So using data in [21] and [22] and using the

thermal extension of PLECs the system of Figure 6-1 and 6-2 is implemented.

To carry a thermal analysis a steady state simulation is done. The main idea of steady state is simulate a few cycles of switching that occurs when the system is stable, that implies no dynamics. So Battery and DC link are modelled as ideal voltage sources. The battery is set to the worst case voltage 41 Volts and the output at 400 Volts, the rated value. Inductors, capacitors and semiconductors implemented in this simulation are the ones presented in Chapter 4.

The action signals, duty ratio for the case of the stage one and the phase shift for stage two are calculated using the steady state equations. Using equation 4.2 for the presented case the duty ratio is set to 0.6435. Now using equation 4.6 phase shift is obtained for a power equals to the nominal of the battery discharge (180 A at 41V = 7.38 kW), because higher power are only allowed during a few seconds. Then the phase shift is 24°.

Including the thermal resistor of the proposed heat-sink a steady state analysis is performance and temperatures are attached in Table 6.1
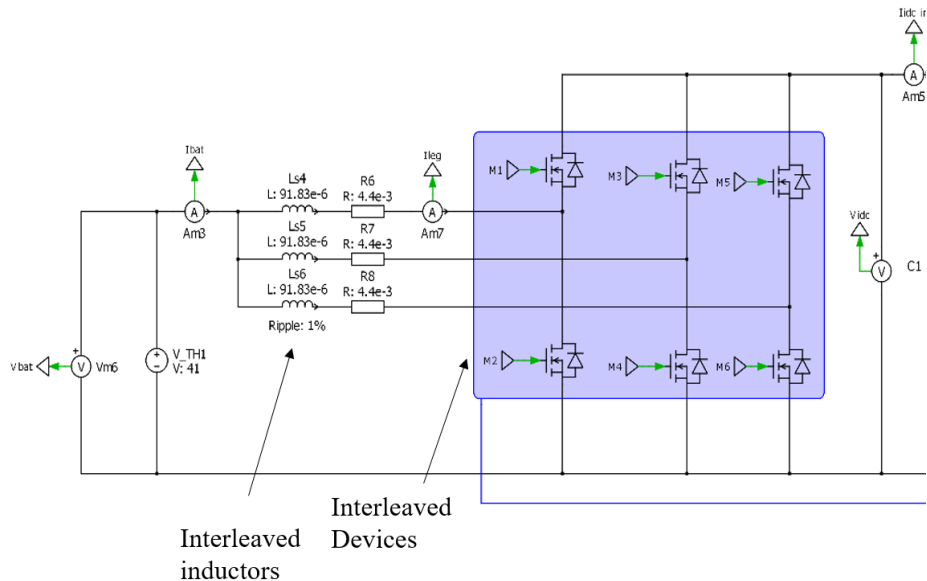

Figure 6-1: PLECs schematic used, stage 1.
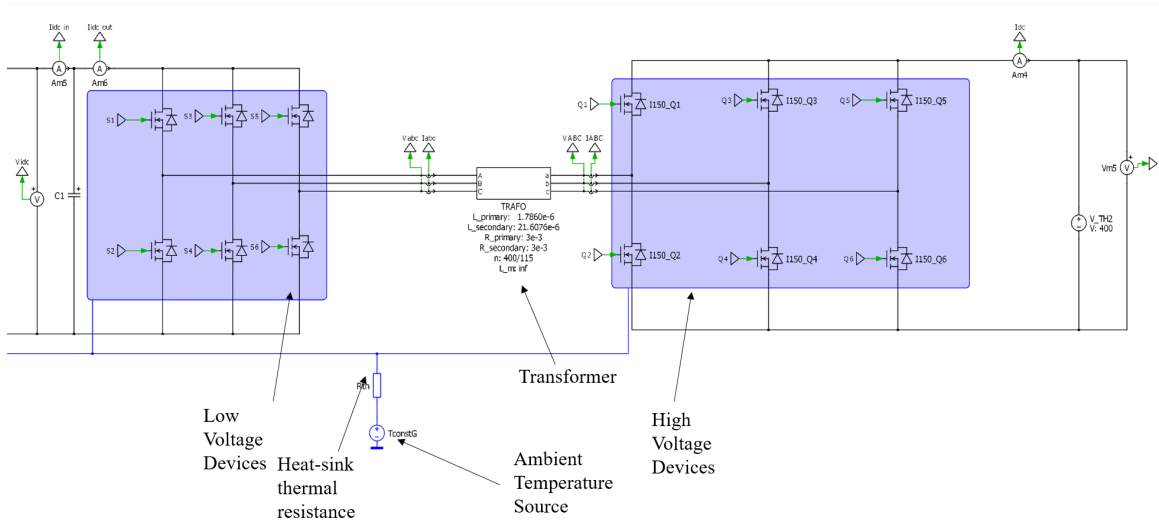
Figure 6-2: PLECs schematic used, stage 2.

Table 6.1: MOSFETs Tested Temperature

Stage 1						
MOSFET	M1	M2	M3	M4	M5	M6
TEMPERATURE (°C)	83.55	77.85	83.54	77.855	83.557	77.856
Stage 2						
MOSFET	S1	S2	S3	S4	S5	S6
TEMPERATURE (°C)	77.55	77.54	77.55	77.55	77.55	77.55
MOSFET	Q1	Q2	Q3	Q4	Q5	Q6
TEMPERATURE (°C)	66.37	66.37	66.37	66.37	66.37	66.37

Table 6.1 shows that the proposed heat-sink keeps under 90°C the temperature of all device, so this results confirms that the previous design of the heat-sink is correctly implemented.

6.1.2 Efficiency Analysis

Analysis of the efficiency was performance at the lowest voltage in the battery (41V), keeping interleaved voltage at 115 volts. Then the load changes moving the phase shift from the maximum power in discharge to the maximum power in charge. In power calculations, PLECs do not take into account losses produced during switching and conduction, so they are calculated with the thermal module and then added for a more accurate efficiency analysis result.

63

Then Figure 6-3 shows the efficiency evolution for all the operation range of this converter, from 18 kW in discharge, positive phase shifts, to 7380 kW in charge, negative phase shifts. Despite the converter presents a symmetrical power flow, as is shown in Figure 4-10, and the maximum power in charge could be 3C the battery module do not allow this demands, for that reason demand current higher than 1C is not taken into account.
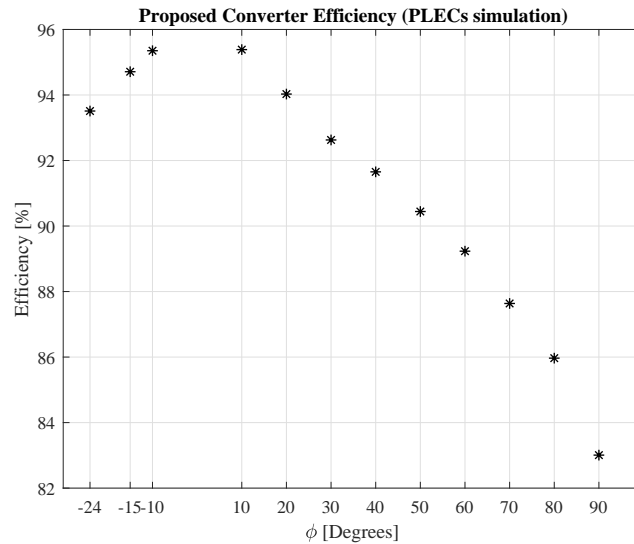
Figure 6-3: Double Stage Efficiency, positive values correspond to discharge and negative values to charge.

Results shows that efficiency decreases at higher power values. Being a problem for heavy power loads. Despite of this behaviour, the modular converter is designed to work most of the time at rated load, 1C, that are related with cycles between -24° and 24°, where the efficiency is around 93-94%. Also if the efficiency wants to be increase, some soft-switching strategies could be implemented.

6.1.3 Capacitor Precharge

One key element in this kind of topology is the precharge of capacitors. To avoid inrush current in the transformer both stages starts with a duty of 0. First the interleaved capacitor is charged increasing slowly the duty ratio to the nominal value. When the DC link capacitor is charged the TPDAB starts to charge the output

capacitor increasing the duty ratio from 0 to 0.5. Also the TPDAB needs a positive phase shift to charge the capacitor, so it sets to 90 degrees. Voltage and current results for precharge are attached in Figure 6-4. This results show there is a huge current during the precharge of the system, which can produce saturation in the leakage inductance and produce some problems in the devices.
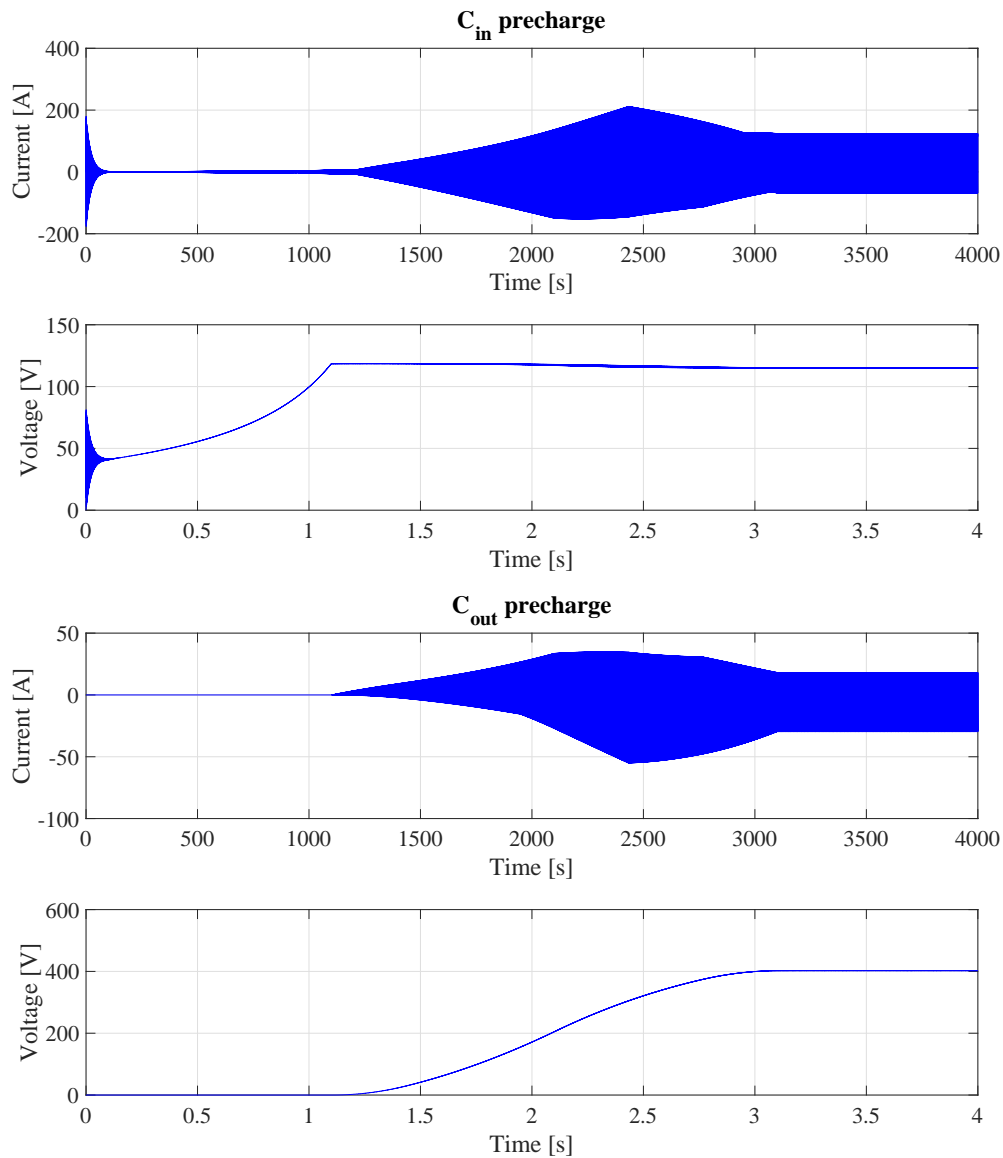

Figure 6-4: Voltage and current in the capacitors during the pre-charge of the system.

6.2 Close loop implementation

With the steady state study the close loop control model is designed. The presented control loop system is a preliminary method that will be improved in future stages of the project.

As commented before the stage 1 is controlled with the duty ratio of the interleaved devices and the stage 2 is controlled through the phase shift. Therefore the main idea to control the system is control the 115V DC link through the duty ratio and the 400V DC link through the phase shift. Then to implement controllers the systems are divided in two independent systems. Also to test the proposed controllers each stage is reduced to the average model. With both models the system is analysed under different charge/discharge situations. Once the system is tested with the average, the full simulation is done for one single charge/discharge reference.

One of the more challenge control design is make large time simulations because this converter is switching at high frequency, 20 kHz. So in order to saw one degree of phase shift in the transformer the minimum step time should be 138 ns. To solve this problem, average models are designed and to validate the avaliavility of the design a short simulation will be implemented with the detail model and compared with the average model. Therefore control design is divided in two different parts: Average Model and Regulator Design.

6.2.1 Stage 1: Control Design

The presented stage consists in an interleaved boost converter. Despite the modulation is phase shifted between each leg, the duty ratio (d) is the same for the tree legs. Then the system can be reduce to a single boost converter, where the inductor is the sum of the three inductors, as Figure 4-3 and 4-4 show, being the system to study represented in Figure 6-5.
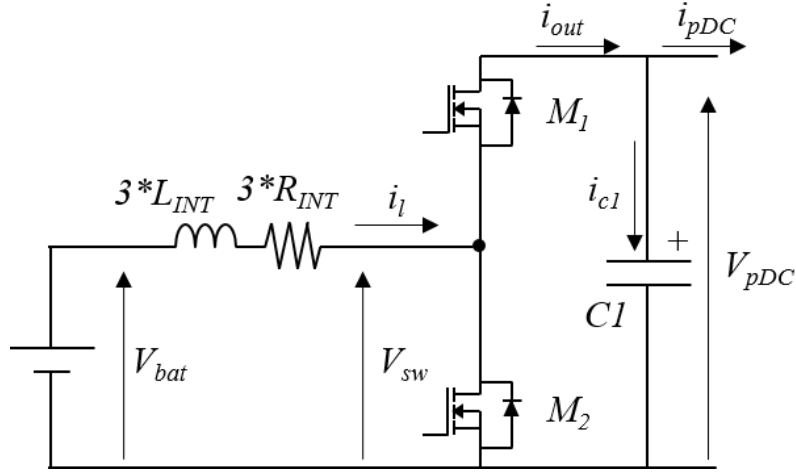
Figure 6-5: Bidirectional boost converter simplify model.

Average Model

Bidirectional boost converter is one of the most common topologies used in DC/DC bidirectional applications. The duty is directly applied to M_2 and M_1 works in complementary mode. So both switches can be replaced by a continuous transformer model [25], assuming an ideal efficiency of 100%: lossless model. So the system is study in average during one cycle of switching. So $\hat{V}_{sw}$ can be written in average as equation 6.1. This equation fulfils the relation in steady state for a boost converter where parasitic resistor is neglected and inductor behaves as a short circuit for DC signals, so $V_{sw} = V_{bat}$ in steady state.

$$\frac{\hat{V}_{sw}}{V_{pDC}} = 1 - d \rightarrow \hat{V}_{sw} = (1-d)V_{pDC} \tag{6.1}$$

So both switches can be replaced by a controllable voltage source with a value equal to $\hat{V_s}w = (1-d)V_{pDC}$. With the lossless model the current through the capacitor can be calculated as equation 6.2.

$$Pin = Psw = Pout \rightarrow V_{pDC}I_{out} = V_{sw}I_l \rightarrow I_{c1} = V_{sw}I_{out}/V_{pDC}. \tag{6.2}$$

Now, substituting the equation that relates input voltage and output voltage with the duty ratio for a boost converter, equation 6.1, the current can be expressed as

equation 6.3.

$$I_{out} = (1 - d)I_l \tag{6.3}$$

So the average model can be designed as Figure 6-6, considering that i_{pDC} is a perturbation that will be rejected with the control system.
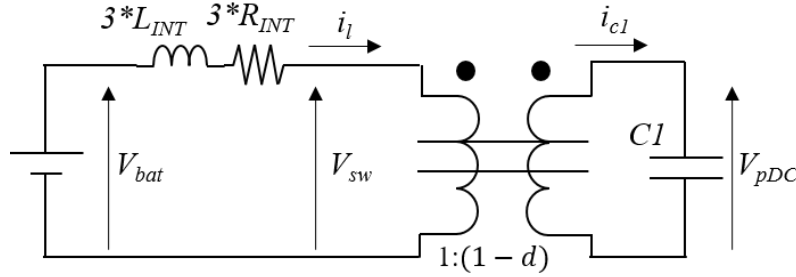

Figure 6-6: Bidirectional Boost Converter Average Model with DC converter model.

Control regulator design

Voltage across the inductor can be write as equation 6.4.

$$3R_{INT}i_l + \frac{di_l(t)}{dt}3L_{INT} = V_{bat}(t) - V_{sw}(t) \tag{6.4}$$

And current in the capacitor could be expressed as equation 6.5.

$$\frac{dV_{pDC}(t)}{dt}C1 = i_{c1}(t) \tag{6.5}$$

The proposed control is a cascade control, with an inner current control of the current through the inductor and an external voltage control of the capacitor voltage. Then the first step is control the current plant give by equation 6.4. Since is a linear model, the Laplace transform can be written as equation 6.6.

$$\frac{i(s)}{V_{sw} - V_{bat}} = \frac{1}{3L_{INT}s + 3R_{INT}} \tag{6.6}$$

This system is a first order system with a pole located in the negative real part

of the root locus, so a zero-pole cancelation is implemented where integral and proportional gains of a controller can be calculated with equation 6.7. Being bw the bandwidth that is set to 500 Hz.

$$K_p^i = 3bwL_{INT}$$
$$K_i^i = 3bwR_{INT}$$

(6.7)

This controlled is tune to control the system of equation 6.6, so adding equation 6.1 is possible relate the duty ratio with V_{sw}. So the final current control diagram block is shown in Figure 6-8.
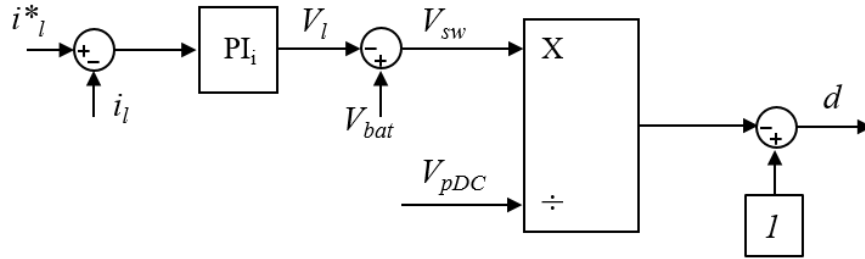
Figure 6-7: Current Control diagram block.

For the voltage control loop, equation 6.5 can be expressed as transfer function, equation 6.8.

$$\frac{V_{pDC}(s)}{i_{c1}(s)} = \frac{1}{C1s}$$

(6.8)

This system has a pole in the origin, so to implement a PI the pole of the controlled is set in the origin and the cero is placed at the half of the bandwidth, the the gain is tune to force the system to be in the real axis at the negative part of the root locus. So gains can be tune with equation 6.9 for a bw_v of 50 Hz.

$$K_p^v = 2bw_vC1$$
$$K_i^v = bw_v^2C1$$

(6.9)

The output of this controlled is the current through the capacitor (i_{c1}) so its necessary refer with the current through the inductor. To avoid algebraical loops for this design the control do not take into account the relation between the duty ratio, i_{out}, i_l and i_{pDC}, assuming a unity factor. So the diagram block for the voltage control is shown in figure 6-8.
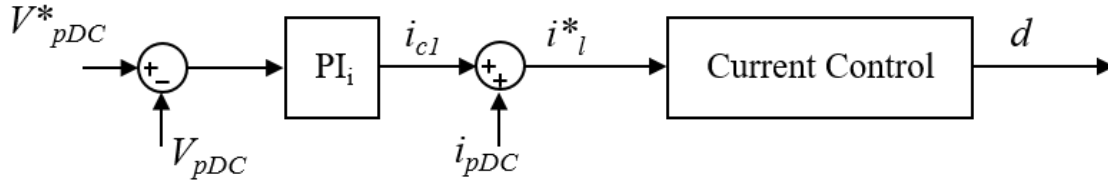

Figure 6-8: Voltage Control diagram block.

Modulation Scheme

With this control scheme is possible keep a the desired values the voltage of the capacitor, but for a real scheme duty must be translate to gate signal levels. The idea of this stage is used an interleaved structure. Figures 4-3 and 4-4 show how the current in the battery is obtained. So every leg works with a phase shift of 120°. Then Figure 6-9 shows the modulation scheme for the stage 1 devices. Where the duty is compared with a triangular waveform with a frequency of 20 kHz and peak to peak value of 0 to 1.

6.2.2 Stage 2: Control Design

For this case the control design is implemented assuming that transformer can be replaced by it equivalent inductor. That's implies a three phase system where the inductor is placed between two controllable sources, so bridges of Figure 4-8 can be replaced by sine voltage sources, where its fundamental value is $\pi/4$ times the peak voltage of the DC link for each case. A one line diagram can be represented in Figure 6-10.
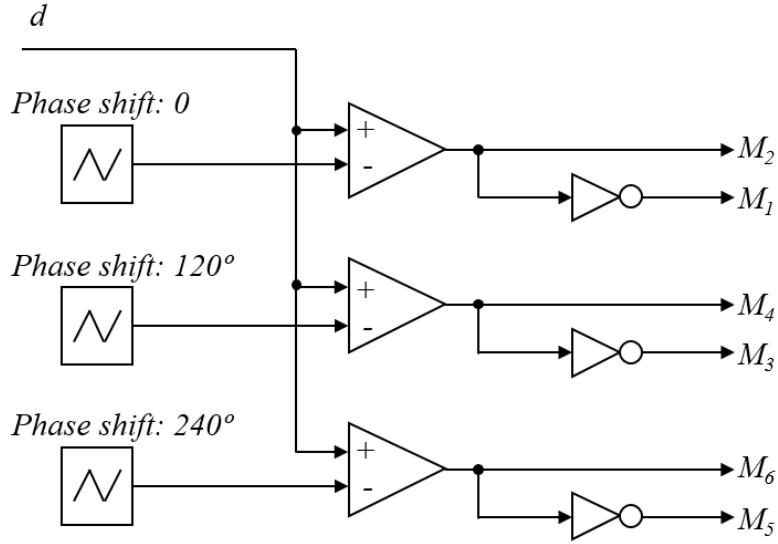
Figure 6-9: Stage 1 modulation scheme.
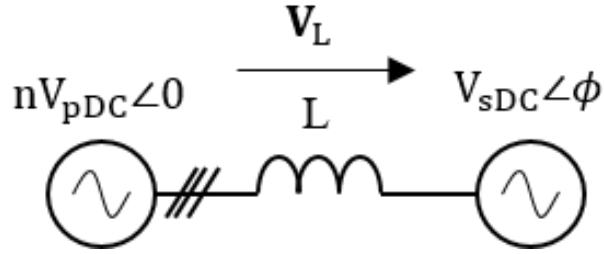
Figure 6-10: Plant Model for the TPDAB.

Average Model

The presented circuit of Figure 6-10 shows a 3 phase system with a frequency of 20 kHz. To reduce the step time the system is studied over one cycle, an average model.

In this case the average model can be implemented through the α and β transform of a three phase system. This vector transform is shown in [Lipo] and relates a three phase system with α and β as equation 6.10, everything refer to the secondary side and considering same duty ratio for both signals.

$$V_{p\alpha\beta} = \frac{2}{3}n(V_{ap} + V_{bp}e^{(j2\pi/3)} + V_{cp}e^{(-j2\pi/3)})$$

$$V_{s\alpha\beta} = V_{p\alpha\beta}e^{-j\phi}$$

(6.10)

71

Where n=400/115. Considering the parasitic resistor of the inductor, the impedance (Z) of the equivalent inductor and resistor can be expressed as equation 6.11.

$$Z = R + L2\pi F_{sw}j \tag{6.11}$$

With this value of impedance the current through the inductor can be calculated as equation 6.12.

$$I_{L\alpha\beta} = (V_{p\alpha\beta} - V_{s\alpha\beta})/Z \tag{6.12}$$

Now power can be calculated as equation 6.13.

$$P_{output} = real(sqrt(3)(V_{s\alpha\beta}\ \bar{I_{L\alpha\beta}}))$$
$$P_{input} = real(sqrt(3)(V_{p\alpha\beta}\ \bar{I_{L\alpha\beta}})) \tag{6.13}$$

The reason to refer everything to the secondary is that now the current through the capacitor can be expressed as equation 6.14.

$$I_{sDC} = P_{output}/V_{sDC} \tag{6.14}$$

Then the average model for the TPDAB converter is presented in Figure 6-11.
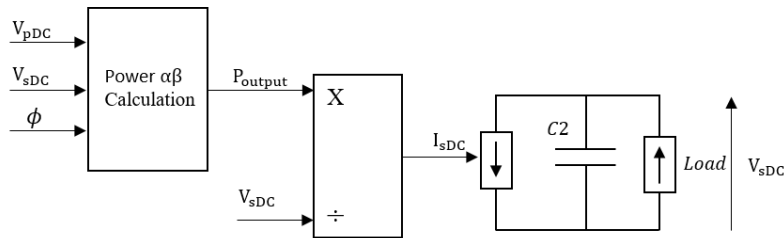

Figure 6-11: TPDAB Average Model.

Regulator Design

With the average model is easy to see that current in the capacitor is directly controlled with the power flow that it's related with phase shift. The equation that relates the voltage of the capacitor and current is presented in equation 6.15.

$$\frac{dV_{sDC}(t)}{dt}C1 = i_{c2}(t) \tag{6.15}$$

As in the previous case of stage 2, the system is a first order system with a pole in the origin, so following same procedure than the voltage regulator of stage 1, regulators can be tune with equation 6.16 for a bandwidth (bw_{v2}) of 50 Hz.

$$K_p^{v2} = 2bw_{v2}C2$$
$$K_i^{v2} = bw_{v2}^2 C2 \tag{6.16}$$

But now to reduce overshoot the effect of the implemented zero in the regulator is reduced using a prefilter with a gain equals to the gain of the zero, equation 6.17

$$Prefilter = \frac{K_i^{v2}/K_p^{v2}}{s + K_i^{v2}/K_p^{v2}} \tag{6.17}$$

The output of this controller is the current of the capacitor, so in order to related it with the power to obtain the needed phase shift the output of the PI is summed by the i_{sDC} and multiplied by the V_{sDC}. Then phase shift and power are related with equation 6.18, that is the same that 4-10 but for all range of ϕ.

$$\phi = asin(\frac{2\pi FhzL}{nV1V2}P_{ref}) \tag{6.18}$$

Then the final control diagram block is represented in Figure 6-12.

Modulation Scheme

As in the case of stage 1, the stage 2 need some modulation to translate phase shift to gate signal. In this case, duty is set at 0.5 and the phase shift is variable. Therefore
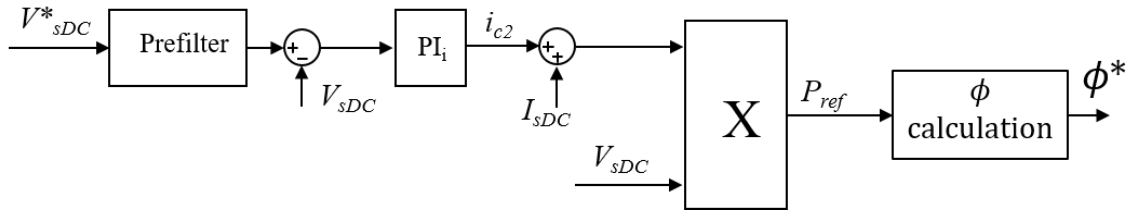
Figure 6-12: Stage 2 voltage control diagram block.

the simplest option to control two converters is a six-step modulation. Based on the usefull states of a 3 phase inverter, the six-step configure the position of each device based on the value of the angle for the complex vector generated. Then Figure 6-13 shows the six possible configuration, being $0 = 0V$ and $1 = V_{pDC}$ or V_{sDC}, depending the inverter.
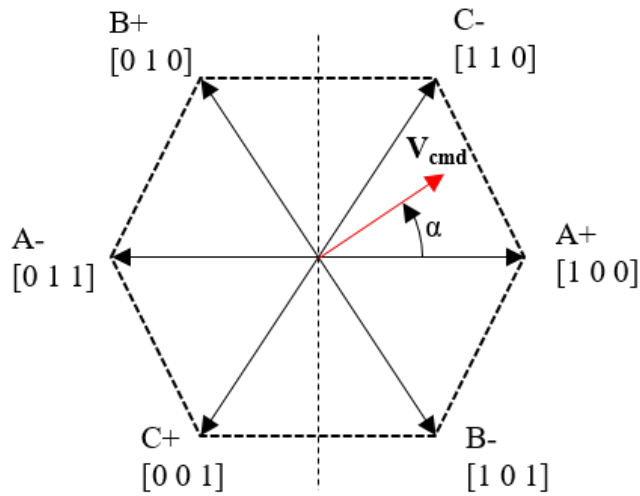
Figure 6-13: Six-step, space vector representation.

To implement this modulation in simulink the angle reference (α) is rotating at 20 kHz with the correspondent phase shift. From Figure 6-13 is notice that the state of one leg change between $[\pi/2, 3\pi/2]$ for phase a, $[\pi/3, 4\pi/3]$ for phase b and $[2\pi/3, 5\pi/3]$ for phase c. So if the value of the angle is between this ranges for each one the output of gate 1 is the high level, logic 1, and gate 2 is the low level, logic 0, out of this limits is the inverse mode. So implementing the scheme of Figure 6-14 is possible obtain the gate signals for each device.

Since the control has been designed to manage the power through the phase sift
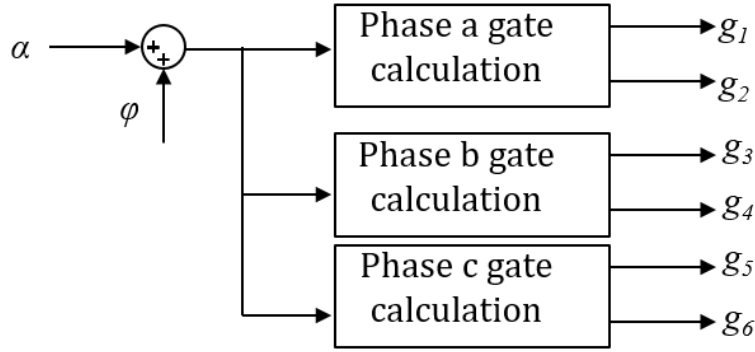
Figure 6-14: Six-step general description.

between primary and secondary the final modulation scheme is presented in Figure 6-15.
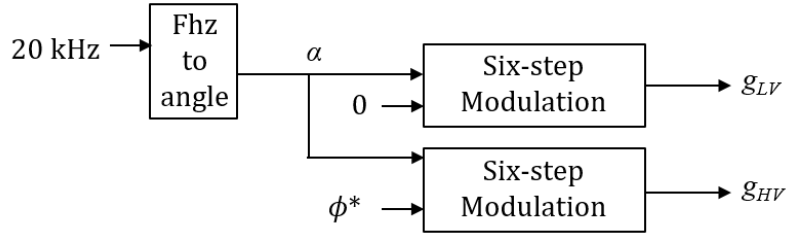
Figure 6-15: Stage 2 modulation scheme.

6.3 Simulation Result

6.3.1 Average Model Results

With the previous control design and average model a simulation in simulink with the PLECs blockset feature added was carry. Both average models are added together conecting the V_{pDC} of each stage. Then different load cycles was carry in order to see the aviavility of the design.

Light Load

Figure 6-16 shows load current, battery current, the voltage at the primary and voltage at the secondary for light loads: 1/8 of C, 1/4 of C, 1/2 of C. These results

shows that until 1/2 of C the system behaves as expected under the voltage and current limits for all devices.
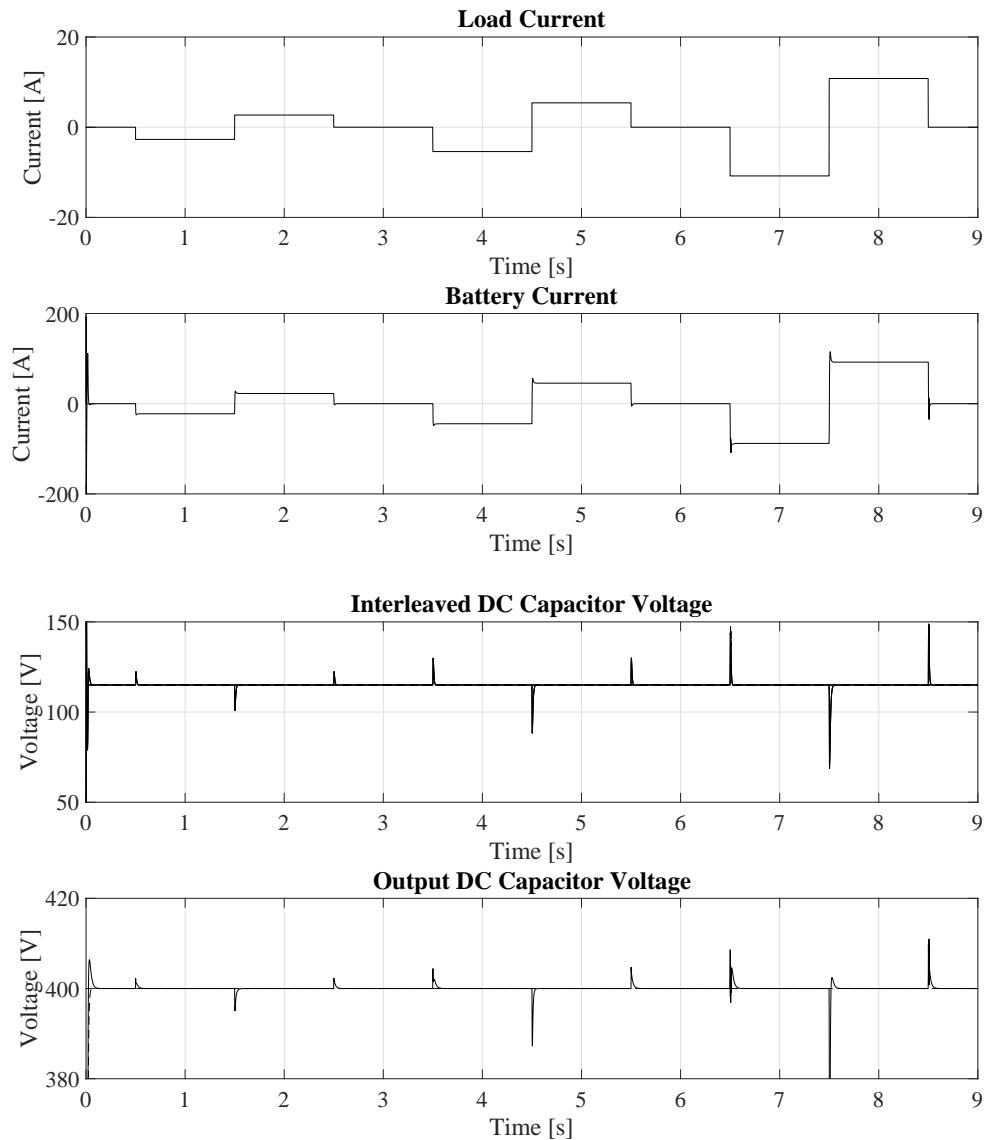
Figure 6-16: Average Model control test 1: Light Loads.

Nominal 1C current

Once the light loads are introduced the nominal current to the battery is demanded. Figure 6-17 shows the evolution of load current, battery current, interleaved voltage and output voltage. First is notice that overshoot in DC Capacitors increase,

also there are some noisy behaviour during transients, but the control can manage this problems and reject perturbation. Despite it can be controller, proposed semiconductors cannot manage those voltage levels so new control techniques should be implemented in future works in order to reduce this overshoots.

Figure 6-17: Average Model control test 1: Nominal Loads.

Heavy Loads

The last test performance is the heavy load test. During this test a 2C and 3C load are demanded, because the maximum allows charge is the nominal value charge process are set to 1C.. Figure 6-18 sho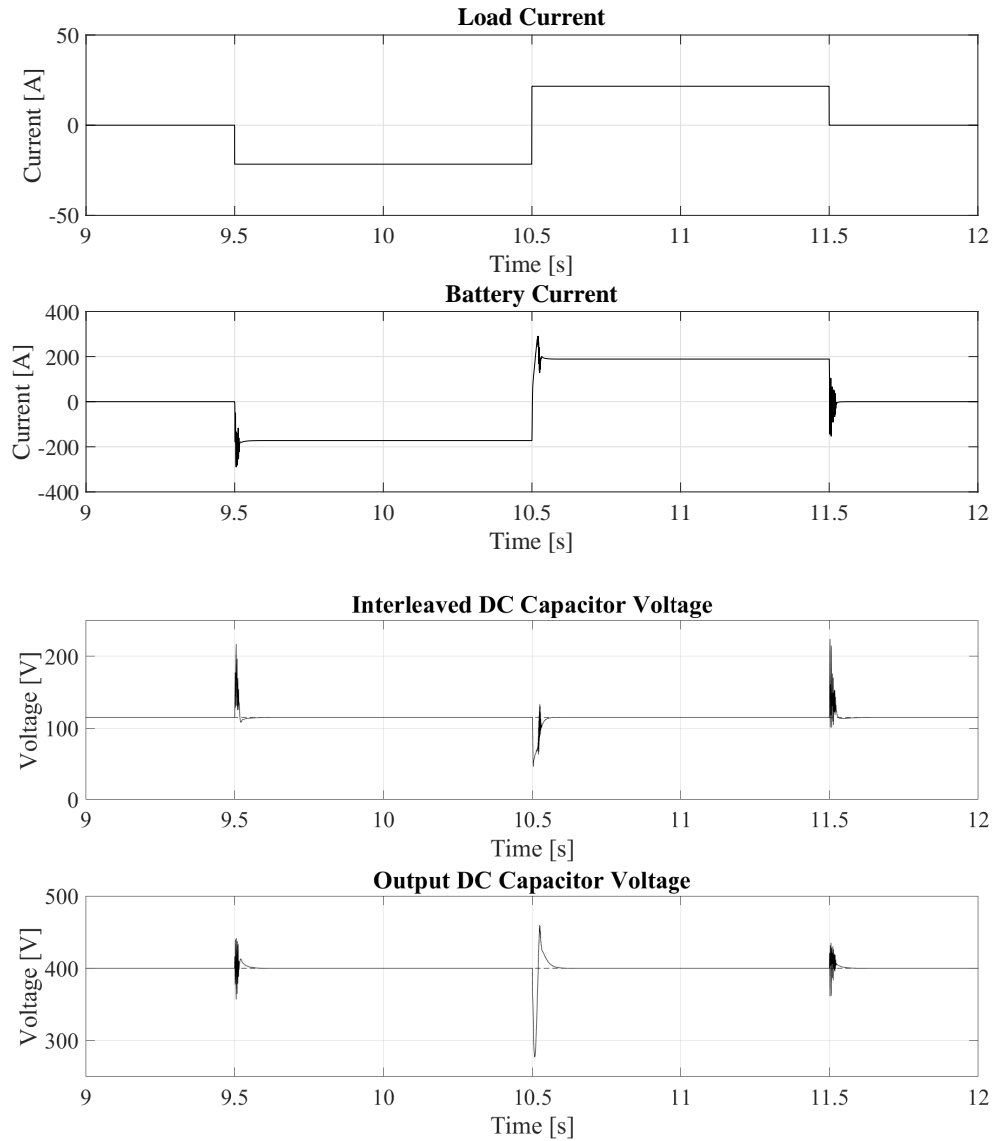ws the same signals that previous tests. In this case the output capacitor is completely discharged, so output power will be always zero. The average model, that used the power to calculate the current through the output capacitor is now zero, then the capacitor is never charge and the output cannot recover the 400V.

6.3.2   Detailed Model Results

After the average tests, a detailed model with the switching behaviour is analysed with a light load of 1/4C and is compared with the correspondent average response. Then Figure 6-19 shows load current, battery current, interleaved capacitor and output load capacitor.

The first different between detailed and average model is the huge ripple in the detailed. Due to the feedback of voltage and current, ripples add some noises to the control. Another difference is the overshoot and steady state response. This difference is related with the main assumption of a lossless model, that in this simulation is not real, because the model has losses in the parasitic resistors and switches.

However, the detailed model rejects the perturbation and keep the voltage at the rated level with a voltage ripple around the 1.25% in the worst case and voltage in the interleaved are under the maximum allowed by MOSFETs. Then this graphs demonstrate that the proposed control system works for this converter.
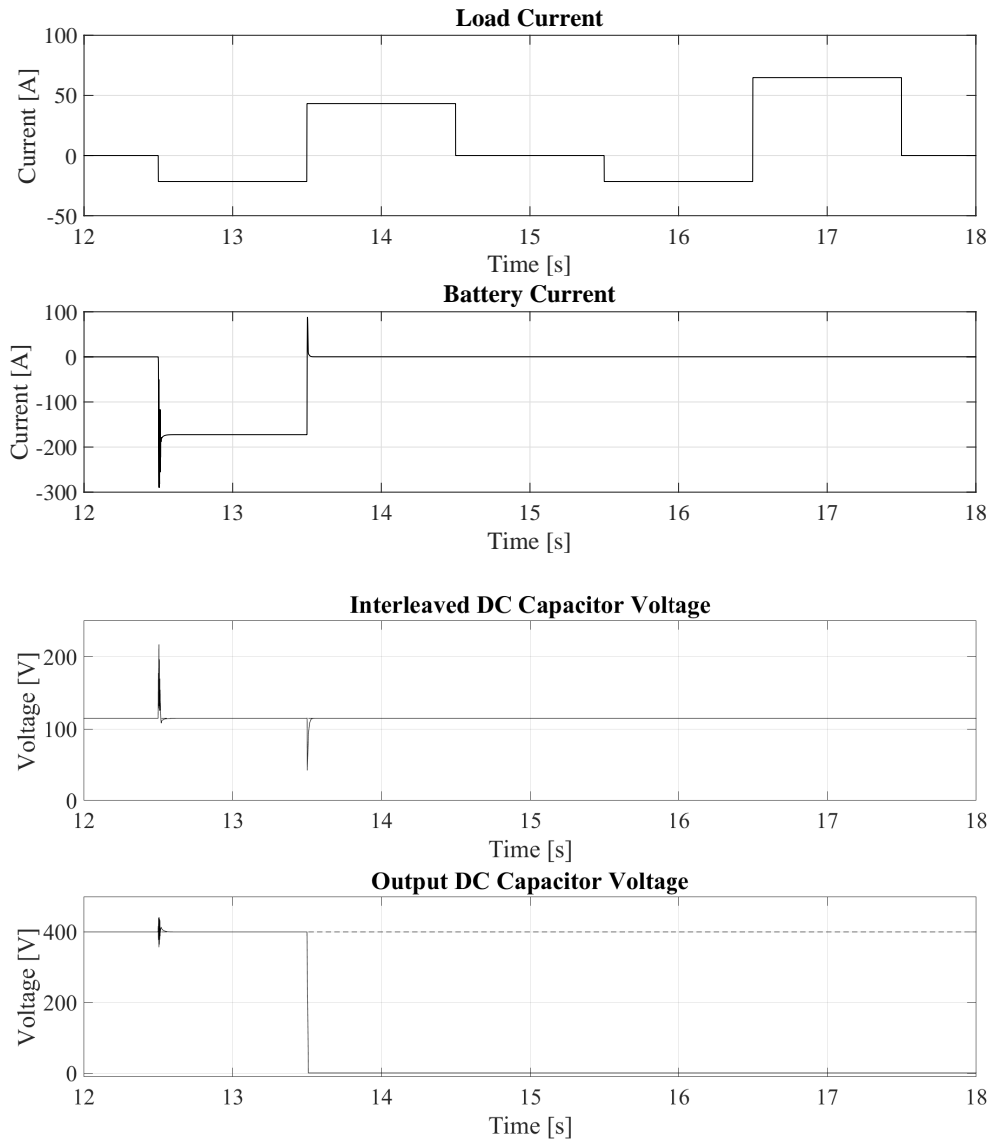
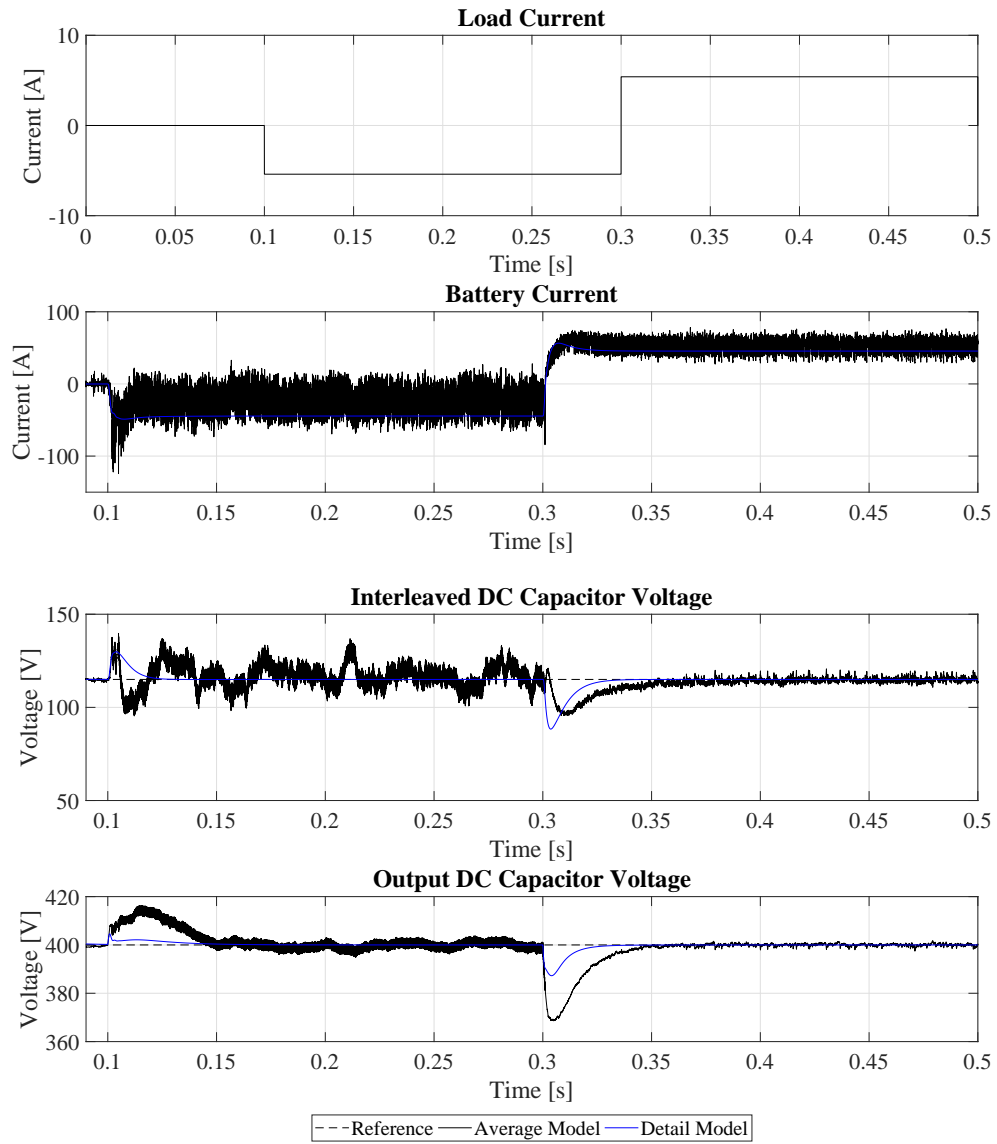Figure 6-18: Average Model control test 1: Heavy Loads.

Figure 6-19: Average Model control test 1: Heavy Loads.

Chapter 7

Conclusion and Future Work

Topology of a double stage formed by an interleaved bidirectional boost converter and a three phase dual active bridge have been presented, analysed and studied. Using software tools Simulink & PLECs for electronic analysis and FreeCad for mechanical design is possible to conclude that the topology can be implemented with proposed specifications with a good performance, low current stress in the battery and managing a stable 400V boost.

This Master Thesis demonstrate how a combination of two different topologies can improve the behaviour of the overall converter. The first comparison between availability DC/DC converters study the different option in terms of cost, efficiency and reliability. This section demonstrate how the main converters could be adapted for this battery pack, and how a combination between two circuits compensate problems of each topology. Simulation analysis prove the availability of the design: How interleaved structures can reduce stress in semiconductors, batteries and passive components avoiding the problems of parallel MOSFETs, how three phase currents are generated in the transformer at 20 kHz and the reduction of current through TPDAB semiconductors. Film capacitor selection evidence that is possible to obtain a good voltage ripple and the capability to manage huge currents with few capacitors, reducing the size and cost.

Modularity of the proposed converter is really easy to implement. Adding more interleaved legs and resizing TPDAB series inductors allow more power management

without a significantly increase in the cost or changing the main structure of the converter. Following the same idea, proposed converter can be redesigned for light power applications, deleting interleaved legs, without change any parameter in the transformer or reducing the series inductance. Another capability of this design is the option to work with variable voltage sources without any change in the presented topology.

An advantage presented in this project is the possibility of implement MOSFETs as switching devices, having the capability to increasing switching frequency and reducing passive components, maintaining switching and conduction losses at similar levels.

Thermal, steady state and open loop study demonstrate the validity of selected components. Moreover, efficiency analysis presents a good ratio between 86 to 93% achieving one of more the important goal in modular converter: a high efficiency converter.

Control design exhibit the possibility to create two independent close loop controls for both stages, making easy to implement a control for many devices. Besides, average models exhibit that is possible fast and accurate simulations when higher switching frequencies are used.

7.1 Future Implementations

The proposed control scheme is a preliminary design which only manage light loads. For that reason next steps will improve the control of this system to operate at the maximum capacity of the system, new methods to reduce noise in control signals, complex pre-charge process to reduce current peaks at the start of the converter to avoid saturation of leakage inductors in the transformer, new schemes to reduce voltage overshoots and soft-switching strategies to improve the efficiency at heavy loads.

From the point of view of the mechanical design, the proposed size of this converter could be reduce including modular semiconductors, where one leg or the six devices

are introduced in only one package reducing the needed heat-sink surface and DC link and phase plates sizes. This future implementation will be translate in a more compact design.

At project level the converter will include communication modules to exchange information with the EMS master. In addition the modular system will be tested to operate in a modular structure with another DC/DC converters in parallel, everything manage with the EMS.

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