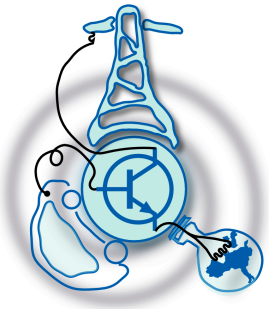
Analysis of the Switching Characteristics of GaN HEMTs Using Double-Pulse Test and a Buck Converter

by
Rafael García Villa



Submitted to the Department of Electrical Engineering, Electronics, Computers and Systems
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Abstract

In this thesis, the rising and promising switching power technology of the *Gallium Nitride* (GaN) transistors will be studied. It has been observed that the evolution of Silicon (Si) transistors has almost reached its theoretical limits, so new technologies are being studied to find new improvements that allow the power conversion field to continue developing and increasing.

During this project, the aforementioned GaN technology will be evaluated in several ways. First, a deep theoretical study will be carried out, explaining the main characteristics of these devices. Then, a set of tests will be performed to analyse the behaviour of the GaN transistors, which include the double-pulse test and a synchronous buck converter. In both cases, the power devices will be evaluated experimentally and in simulations, in order to compare both results. During the tests, different operating points will be studied (different voltages and current levels). To carry out these analyses experimentally, an evaluation kit of *GaN Systems* will be employed, as well as a Digital Signal Processor (DSP) of *Texas Instruments* to control the commutation of the devices. In the case of the simulations, the latest version of the simulating program *PSIM* will be used, which allows to include the real behaviour of the power devices.

The obtained results will be exposed and commented, trying to identify the particularities of these devices and making a comparison between the simulation and experimental results.

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Chapter 1

Introduction

1.1 Problem Background

During the last thirty years, metal oxide silicon field effect transistors (MOSFETs) have experienced a continuous development due to their power management efficiency and cost improvements. However, the rate of progress has been decreased in recent years since this technology has almost reached its theoretical limits.

In 1976 power MOSFETs appeared as an enhanced alternative to bipolar transistors. These new devices were introducing important improvements such as an increased ruggedness, faster switching behaviour and the capability of manage larger current levels. This fact gave rise to an important increase and development of the power electronics field and their utilization in different applications, such as desktop computers, variable-speed electric motor drives, DC-DC power supplies, low-voltage (LV) renewable generation, ligthing and home appliances, battery chargers, transportation, industry tools and many other applications [3].

One of the most important challenges to overcome in electrical energy conversion consists in reducing as much as possible the power losses of the converters, which directly implies to develop more efficient transistors. Since there is no much more margin to improve the Si devices efficiency, new solutions are being investigated. Other relevant features that must be present in a new semiconductor to be economically viable are: reliability, power density, manufacturability and modularity. Different

options can be used as an enhanced alternative to Si power MOSFETs. For high frequency high power applications, Gallium Arsenide (GaAs) devices represent one of the most powerful alternatives. However, they do not satisfy the ever-increasing performance requirements, so there is an emergin interest in other wide band-gap materials and device technologies that inertly satisfy the performance demand thanks to their material properties [44].

Although there are still some improvements to achieve in power MOSFETs (which will reduce the cost of these devices), Gallium Nitride (GaN) transistors are becoming one of the most promising technologies for low and medium voltage power conversion in the following years. This technology offer higher power densities and higher operating efficiencies than power MOSFETs and GaAs devices, and it is expected to become dominant in many commercial and space applications of power devices. In addition, thanks to the AlGaN/GaN heterostructure, the basis for the generation of the high electron mobility transistors (HEMTs) that rely on a two dimensional electron gas (2DEG) for conduction is provided, leading to excellent properties such as increased current density and output power. GaN-based HEMTs are suitable for high power high frequency applications due to their high thermal conductivity, large polarization fields, and saturation drift velocity [34]. The largest operating frequencies achieved with GaN HEMTs are around 94 GHz [33] and highest power densities than 30 W/mm [11]. Furthermore, due to the high breakdown-field, it is possible to use this technology in high-power switching appliances. However, GaN-based devices have not reached yet their maturity for high power high frequencies applications. This technology still has many features to improve and that is why its research and development is on the rise.

1.2 Objective of the Thesis and Report Outline

In this thesis, the promising switching power technology of GaN HEMTs will be evaluated in different ways: theoretically, in simulations and experimentally. The objective of this project is to evaluate the switching characteristics of these devices

by carrying out different experimental and simulation tests. For this purpose, an evaluation platform of *GaN Systems* will be used in the experimental analyses, as well as a Digital Signal Processor (DSP) of *Texas Instruments*.

The thesis will be constituted by the following chapters:

- **Chapter 1:** Introduction and report outline.
- **Chapter 2:** Theoretical analysis of the GaN HEMTs. In this chapter, a theoretical study of the main characteristics of the GaN high electron mobility transistors will be carried out. The principles of operation of these devices will be explained, as well as the device structure, the electrical features, and the driving considerations.
- **Chapter 3:** During this chapter, a theoretical explanation of the tests that have been performed to analyse the switching characteristics of the GaN transistors will be included. The practical implementation of these tests will be also included, for both the simulation and experimental evaluations.
- **Chapter 4:** In this chapter, the results of the analyses carried out experimentally and in simulations will be commented, observing the switching characteristics of the power devices and making a comparison between the experimental and simulation results.
- **Chapter 5:** The conclusions of the project and the future work will be included in this chapter.

Chapter 2

Gallium-Nitride HEMTs

In this chapter, the main characteristics of the GaN devices will be explained. Particularly, a brief comparison of the material properties of these transistors with respect to Si and SiC technologies will be performed, and later the GaN devices will be studied in more detail, analysing the fundamentals of operation, the device structure, types of GaN devices, the electrical characteristics and the driving features.

2.1 Material Properties and Advantages of GaN

As commented in Chapter 1, silicon devices have assumed a central role in the design of semiconductor devices in the last thirty decades. However, they have almost reached their theoretical bounds, due to the Si intrinsic material properties such as low breakdown voltage, low saturation velocity, high device resistance and low inversion layer mobility [2]. For this reason, there is an increasing interest in studying and developing new and improved semiconductor materials to design switching devices.

Wide band-gap semiconductors such as GaN or Silicon Carbide (SiC) represent one of the most promising materials that are able to meet the requirements for high-power, high temperature switching applications. In table 2.1 [34], [37] the main material properties of Si, SiC and GaN semiconductors are exposed:

Table 2.1: Material properties of Si, SiC and GaN [26]

Material Property	**Si**	**SiC**	**GaN**
Band Gap [eV]	1.12	3.26	3.39
Critical Breakdown Electric Field [MV/cm]	0.23	2.2	3.0
Electron Mobility [cm^2/V-sec]	1350	950	1500
Electron Saturation Velocity [$10^7 cm/sec$]	1.0	2.0	2.5
Thermal Conductivity [Watts/cm K]	1.5	3.8	1.3

In this table, the advantages of GaN over its main competitors in the semiconductor market can be observed. The band gap defines the strength of the bonds between the atoms in the lattice, that is, the difficulty for an electron to jump from one site to the next. As it can be checked, GaN and SiC have larger band gaps in comparison with Si. This improves the blocking performance for a given temperature, and provides avalanche rugedness.

It can be seen that GaN has the highest electrical breakdown field (an order of magnitude higher). For a given voltage rating, much higher doping levels can be used, achieving better on-state performance with reduced thickness, which implies less charge accumulation effects and in turn, improved switching characteristics. Conversely, for a given chip thickness, devices with much higher voltage ratings can be achieved.

The electron mobility and saturation velocity are also higher in GaN material, which implies a better conductivity of the devices. This advantage is illustrated in Figure 2.1: for same sized transistors, rated for the same breakdown voltage, as the breakdown voltage increases, the on-resistance increases as well for all de materials, but GaN shows the best performance in this characteristic, achieving the lowest on-resistance when comparing the different materials at the same breakdown voltage level.

The large electron sheet densities (around $1 \times 10^{-13}\, cm^{-2}$) and the high electron mobility also allow to achieve large drain currents of grater than $1\ A/mm$. However,

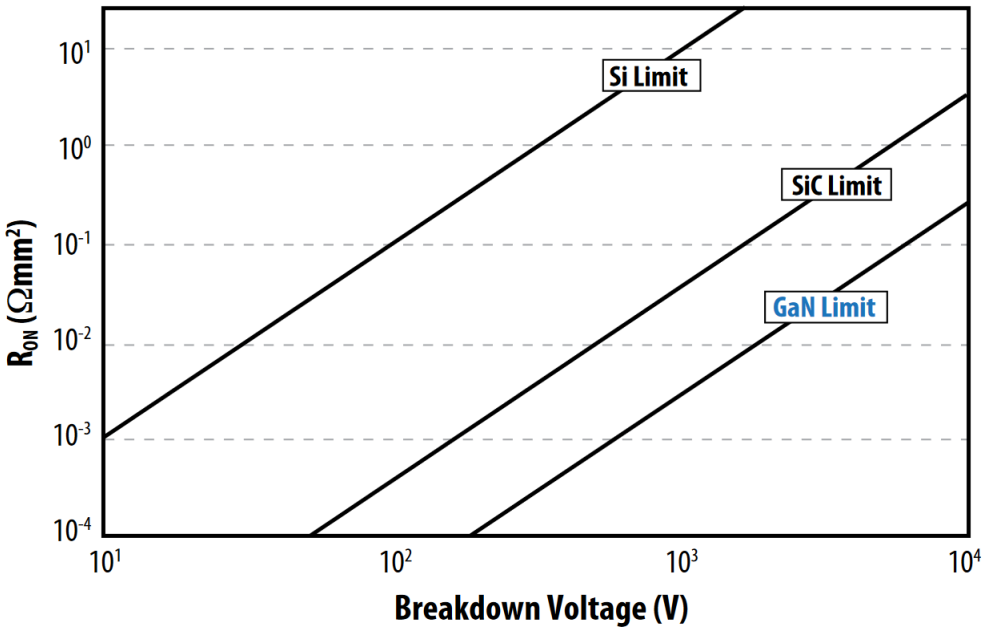


Figure 2-1: Theoretical on-resistance vs blocking voltage capability for silicon, silicon-carbide, and gallium nitride [3].

GaN shows a similar thermal conductivity than silicon, which is much lower than that of SiC (over three times lower). This means that the the efficiency to dissipate heat is significantly worse, which implies a better thermal management from part of GaN devices when compared to SiC.

Another remarkable characteristic particular from the wide-band semiconductor materials can be evaluated with the Johnson's Figure of Merit (JFOM). This function gives an idea of the material suitability for high-power high-frequencies applications, and can be calculated by using the following expression [30]:

$$JFOM = \left(\frac{E_c \cdot v_{sat}}{2\pi} \right)^2 \tag{2.1}$$

Table 2.2: Figures of merit of GaN and competing semiconductor materials in power electronics [5].

Property	**GaN**	**Si**	**GaAs**	**SiC**
JFOM	270-480	1.0	2	324-400

In Table 2.2 the values for the JFOMs for the different semiconductor materials are shown. As it can be observed, the JFOM of the GaN is around 270 to 480 times higher than that of silicon, about 135 to 240 times larger than GaAs and over 1.5 times greater than SiC. In general, wide-band materials offer the best performances to meet the modern-day power electronic requirements. But it is obvious that GaN is the best solution for high-power high-frequencies applications than their market competitors. With all these properties, it can be determined that GaN-based devices are ideal for microwave and millimetre wave amplifiers, RF amplifiers, space and radar electronics including local multipoint distribution systems, digital radio and base station transmitters [5]. In the power electronics field, GaN-based High Electron Mobility Transistors (HEMTs) represent a promising technology for electric and hybrid vehicles, electrical inverters, switched mode power supplies and motor drive circuits which operate in the voltage range of $600\,V$ to around $1200\,V$ [37] [40].

2.2 Fundamentals of 2DEG and HEMTs

Due to the aforementioned GaN superior intrinsic physical properties (such as wide-band gap, high breakdown electric field, high electron saturation velocity and high density carriers in the form of a 2DEG with high mobility), this material is suitable for high-power high frequencies applications. These devices present great performance improvements, and are also able to operate in harsh environments where silicon transistors cannot work.

An essential property of III-nitride materials (as is the case of GaN) is the capability to form a heterojunction with a ternary alloy made from another III-nitride semiconductor material such as aluminium gallium nitride (AlGaN). Thanks to the strong polar material properties, the modification of the material composition results in dramatic modifications of the polar crystal properties and hence of available carrier concentrations obtained at the heterojunction interfaces in the devices [5]. In this way, a two-dimensional electron gas (2DEG) is formed at the heterojunction, where the electrons are confined to move in two dimensions, in the plane perpendicular to

the surface of the device. This represents the conduction channel. Group III-Nitride semiconductors can be found in different common crystal structures. The natural structure of crystalline gallium nitride is a hexagonal structure named "wurtzite" (see Figure 2.2).

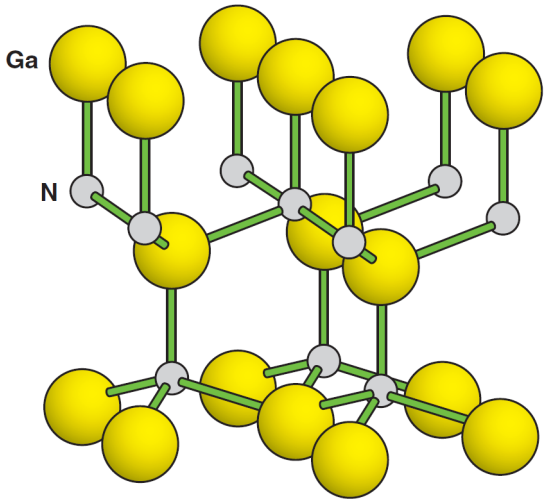


Figure 2-2: Schematic of wurtzite GaN [27].

This structure is really robust due to its high chemical stability and it is able to withstand high temperatures without decomposition. Piezoelectric properties are also provided to GaN by this crystal structure which gives the ability of achieving very high conductivity in comparison with other semiconductor materials. As commented before, by using a thin layer of AlGaN on top of a GaN crystal, a strain is created in the interface leading to the 2DEG (see Figure 2.3). Since the total charge must be neutral, the free electrons accumulate in the quantum well to compensate the high positive polarization induced sheet at the AlGaN/GaN interface. The electrons in the quatum create a two dimensional electron gas channel. This effect allows the efficient conduction of electrons when an electric field is applied between its terminals (see Figure 2.4) [6] [51].

Among other reasons, this layer has very good conductive properties due to the concentration of electrons in a very small region at the interface. Thanks to this phenomenon, the mobility of electrons is increased from about $1000 cm^2/Vs$ to $1500-$

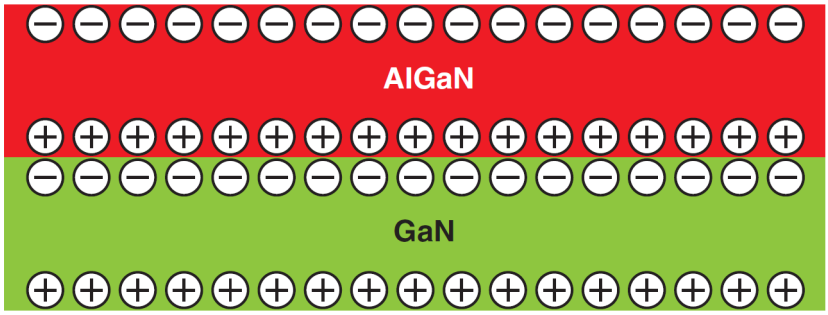


Figure 2-3: Simplified cross section of a GaN/AlGaN heterostructure showing the formation of a 2DEG due to the strain-induced polarization at the interface between the two materials [27].

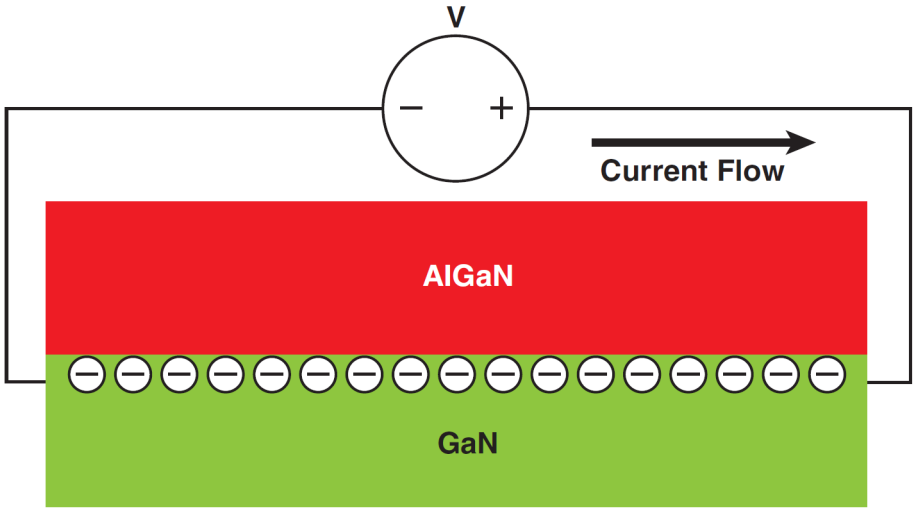


Figure 2-4: By applying a voltage to the 2DEG an electric current is induced in the crystal [27].

$2000\,cm^2/Vs$ in the 2DEG layer. The high concentration of electrons with very high mobility represents the basis for the high electron mobility transistor (HEMT) [27].

2.3 The Basic Device Structure

The structure of a GaN power transistors is composed by gate, source and drain terminals. The drain and source electrodes pass though the AlGaN material in order to create an ohmic contact with the 2DEG. This fact allows to conduct current

between the drain and source terminals, since a short circuit is created until the 2DEG is depleted. When this occurs, the GaN semiconductor crystal is able to block the current flow. The gate terminal is used and placed over the AlGaN layer to deplete the 2DEG. A negative voltage bias relative to both drain and source terminals should be applied to the gate electrode in order to deplete the electrons from the 2DEG. This is the simplest GaN transistor structure, and is called a depletion-mode or d-mode [27]. Notice that the structure of GaN HEMTs is different from that of the silicon metal-oxide field effect transistors (MOSFETs). The PN junction created from the p-region of the body to n+ region at the drain forms a body diode in a typical Si power MOSFET, which is not present in a GaN HEMT [26]. In the following figure, a representation of the GaN HEMT structure is depicted:

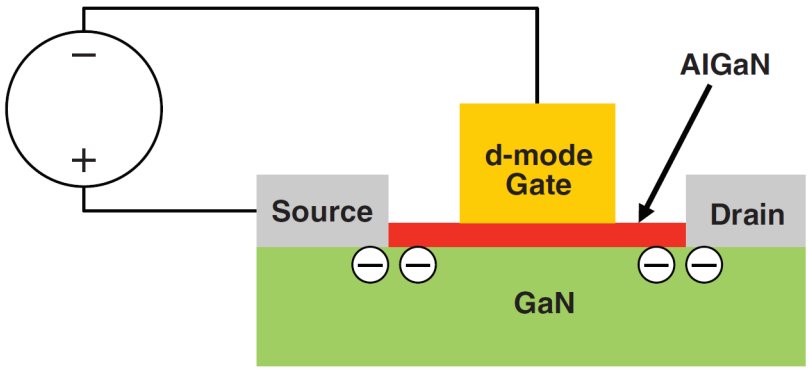


Figure 2-5: By applying a negative voltage to the gate of the device, the electrons in the 2DEG are depleted out of the device. This type of device is called a depletion-mode (d-mode) HEMT [27].

However, d-mode GaN HEMTs are not recommended for power conversion, since a negative bias must be first applied to the transistors at the start-up of the power converter. Otherwise, a short circuit could result. Also, since the normal state of these devices is ON, the lost of the gate drive circuit will maintain the device in on-state, which can lead to short circuits. Instead, other device designs can be used, which have normally off-state devices and a positive threshold voltage is required to turn-on the device. They represent a safer alternative, since the switches would turn-off when the power is lost in the gate drive circuit. Enhancement-mode (e-mode) devices are a good

representation of this solution, which will not experience the previously commented issues. When a zero bias is applied to the gate terminal, the e-mode device is OFF (see Figure 2.6 (a)), and will not conduct current until a positive threshold voltage is applied (see Figure 2.6 (b)). There exist different popular structures that have been designed to create an enhancement device, such as the recessed gate, implanted gate and cascode hybrid.

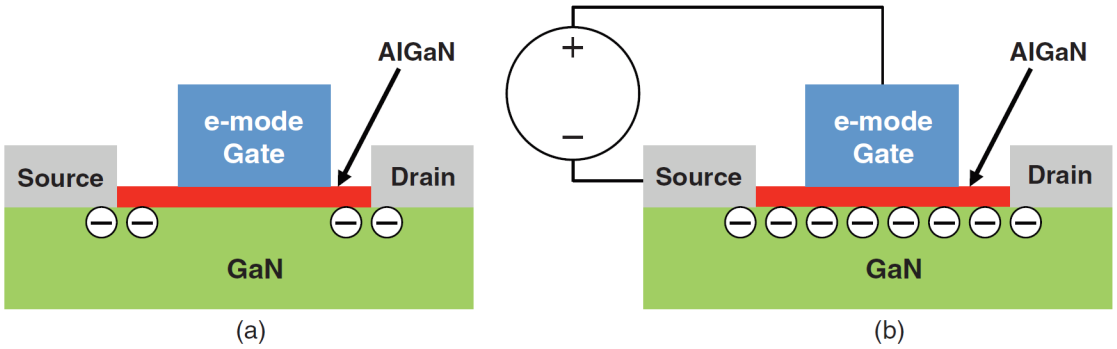


Figure 2-6: (a) An enhancement-mode (e-mode) device depletes the 2DEG with zero volts on the gate. (b) By applying a positive voltage to the gate, the electrons are attracted to the surface, re-establishing the 2DEG [27].

2.3.1 Recessed Gate Enhancement-Mode Structure

The idea of this structure consists in reducing the thickness of the AlGaN barrier over the 2DEG, in such a way that the voltage created by the piezoelectric field is reduced proportionally. When the generated voltage in the AlGaN/GaN interface is lower than the built-in voltage of the Schottky gate barrier, the 2DEG is depleted with a gate zero bias. When a positive bias is applied, the electrons are attracted to such interface and the circuit is closed, therefore allowing the current conduction [24]. One of the most critical aspects to consider in e-mode GaN devices is the small margin of gate voltage. This is due to the fact of the low gate breakdown voltage and the necessary fully turn on voltage is quite close to the gate voltage limit [15].

2.3.2 Implanted Gate Enhancement-Mode Structure

This method, uses an implant of fluorine atoms in the AlGaN barrier layer to create the e-mode device [8]. In order to deplete the 2DEG, the fluorine atoms create a "trapped" negative charge in the AlGaN layer. The enhancement-mode HEMT can be created by using a Schottky gate over the AlGaN interface.

2.3.3 Cascode Hybrid Enhancement-Mode Structure

The particularity that characterises a cascode GaN device is the incorporation of a low-voltage enhancement-mode Si MOSFET in series with a depletion-mode GaN HEMT [16], as shown in Figure 2.7:

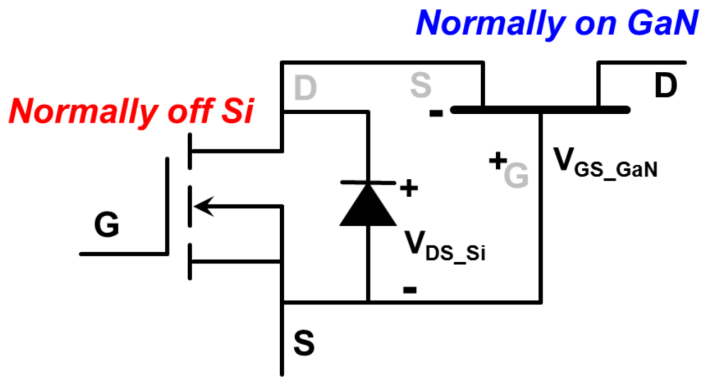


Figure 2-7: Cascode configuration combining a high voltage normally on GaN HEMT with a low voltage normally off silicon MOSFET.

With this configuration, when a positive voltage is applied to the gate terminal of the MOSFET to turn it on, the gate voltage of the depletion-mode GaN device downs to near-zero volts and turns-on. Therefore, the current can flow between the drain-to-source GaN transistor terminals and MOSFET. In order to turn the GaN device off, the voltage at the gate MOSFET electrode must be removed. In such situation, a negative voltage is created between the depletion-mode GaN transistor gate and its source terminal, turning the device off. This structure represents a good solution of an enhancement-mode transistor when the GaN device has a relatively high on-resistance compared with the low-voltage Si MOSFET. However, the previously

commented e-mode GaN devices present are slightly better than cascode transistors. This is because of the fact that the gate loop inductance is significantly reduced, since no additional MOSFET is required [15].

2.4 GaN HEMTs Electrical Characteristics

In this section, the electrical characteristics of GaN transistors to develop power converters will be commented with respect to the features seen in the previous sections. They will also be compared with the traditional Si power MOSFETs, studying their differences and similarities. The main electrical parameters to analyse in a power device are: breakdown voltage between the drain and source electrodes (V_{BD}), on-resistance ($R_{DS(on)}$) and threshold voltage ($V_{GS(th)}$). The parasitic capacitances, as well as the reverse conduction will be also evaluated to provide a complete analysis of the GaN transistor.

2.4.1 Breakdown Voltage V_{BD}

The breakdown voltage of a semiconductor material device is defined as the maximum reverse voltage at which can be submitted before it becomes electrically conductive. Particularly, a power transistor will suffer break down when the the critical electric field (E_{crit}) of any of the included materials is exceed. In such moment, the device will start to conduct current. Notice that the breakdown voltage between the source and drain electrodes is also influenced by the specific design of the device, the specific heterostructure, the internal insulating layers in the device structure above the gate, source and drain electrodes; and the underlaying subtrate material properties [29].

Higher electric fields are created near the drain and gate electrodes, where the contour lines are closer, as shown in Figure 2.8.

The breakdown voltage effect can be also be caused by the interaction between the metal used layers in the device. This phenomenon is produced when one of these layers is connected to the source electrode while a contiguous layer is connected to the drain terminal. In case the E_{crit} of the dielectric material which separates these

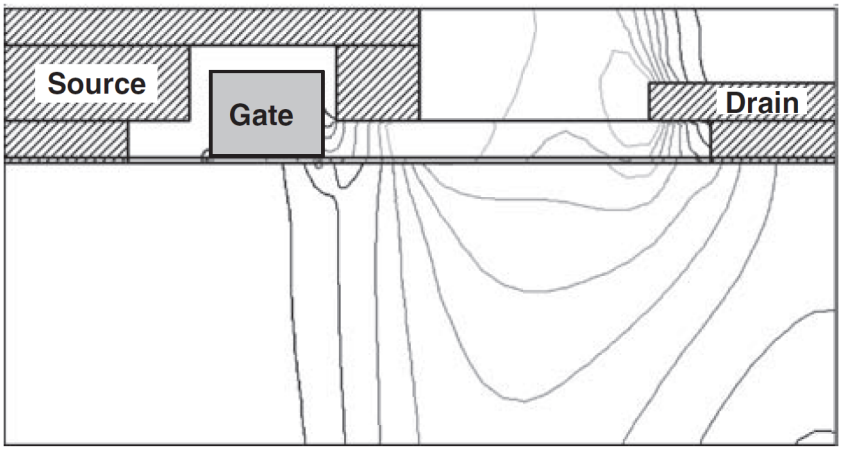


Figure 2-8: The device in Figure 2.6 showing the electric fields when voltage is applied from drain to source.

layers is exceeded, breakdown takes place [27].

The breakdown phenomenon leads to destructive results in HEMTs. Characteristically, if the effect is produced when the insulating layers exceed the critical electric field, the dielectric material will suffer a physical rupture [31]. In case the GaN layer exceeds its critical electric field and breakdown is produced in the GaN or AlGaN layers, a different phenomenon takes place: the generated electrons can destroy the 2DEG, causing the device on-resistance to widely increase [20].

2.4.2 On-Resistance $R_{DS(on)}$

The on-resistance of a semiconductor power transistor defines the conduction losses during the on-state operation [1]. Therefore, it is an essential parameter that requires a proper study and knowledge to optimise the performance of the device and hence of the power conversion system. It is composed by the sum of all the resistance elements that constitutes the device, as shown in Figure 2.9.

As it can be observed, the source and drain electrodes must connect the 2DEG with the AlGaN layer. This resistance component is known as the contact resistance (R_c). During conduction, electrons flow in the 2DEG with a certain resistance, called R_{2DEG}. In the following expression, a description of this resistance is exposed [50]:

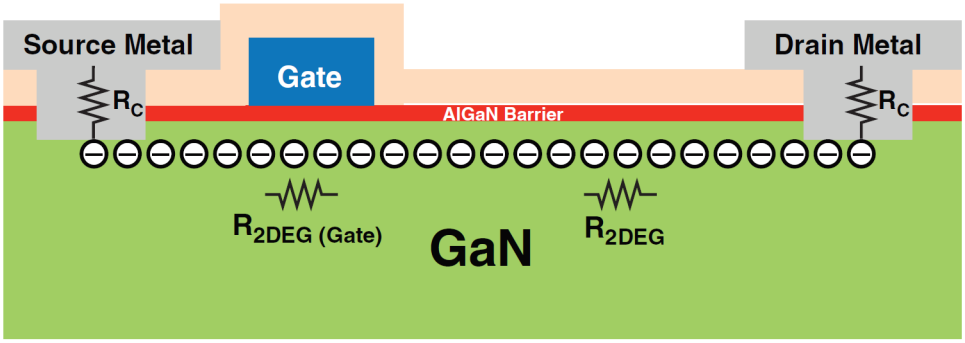


Figure 2-9: Cross section of a GaN HEMT, showing the major components of $R_{DS(on)}$ [27].

$$R_{2DEG} = \frac{L_{2DEG}}{q \times \mu_{2DEG} \times N_{2DEG} \times W_{2DEG}} \tag{2.2}$$

Where L_{2DEG} is the distance the electrons have to travel, q represents the universal charge constant (1.6×10^{-19} coulombs), μ_{2DEG} is the electron mobility, N_{2DEG} represents the number of electrons created by the 2DEG and W_{2DEG} is the width of the 2DEG. It is known that the number of electrons in the 2DEG is directly dependant on the induced strain in the AlGaN barrier. However, the electron concentration under the gate terminal can be lower than in the area located between the gate and drain electrodes, therefore leading to a different on-resistance component: $R_{2DEG(Gate)}$. This depends on the type of gate, the process used, the heterostructure and the applied gate voltage. Hence, an approximation of the transistor resistance can be calculated in the following manner [27]

$$R_{HEMT} = 2 \times R_C + R_{2DEG} + R_{2DEG(Gate)} \tag{2.3}$$

Finally, other parasitic resistances arising from different metal buses that conduct current from the electrodes to the terminals can be consider. Hence, the on-resistance can be calculated with the next equation:

$$R_{DS(on)} = R_{HEMT} + R_{parasitic} \tag{2.4}$$

Notice taht, although the channel and access resistances of AlGaN/GaN HEMTs are minimised by the effect of the high electron mobility provided by the 2DEG, this benefit is only ensured during static bias conditions. When drain current transients from a high-voltage off-state to low-voltage on-state take place, the on-state resistance is normally modified as compared with its static value (the on-resistance remains high for a period of time) [19]. This effect of increased dynamic on-resistance and the adjacent decreased on-state drain current is known as "current collapse", and is considered as one of the most important issues that must be addressed to achieve an efficient power conversion when using GaN-based HEMTs [23].

Another important consideration is the variation of $R_{DS(on)}$ with the temperature. In the following figure, a representation of the variation of the resistance with the temperature is depicted:

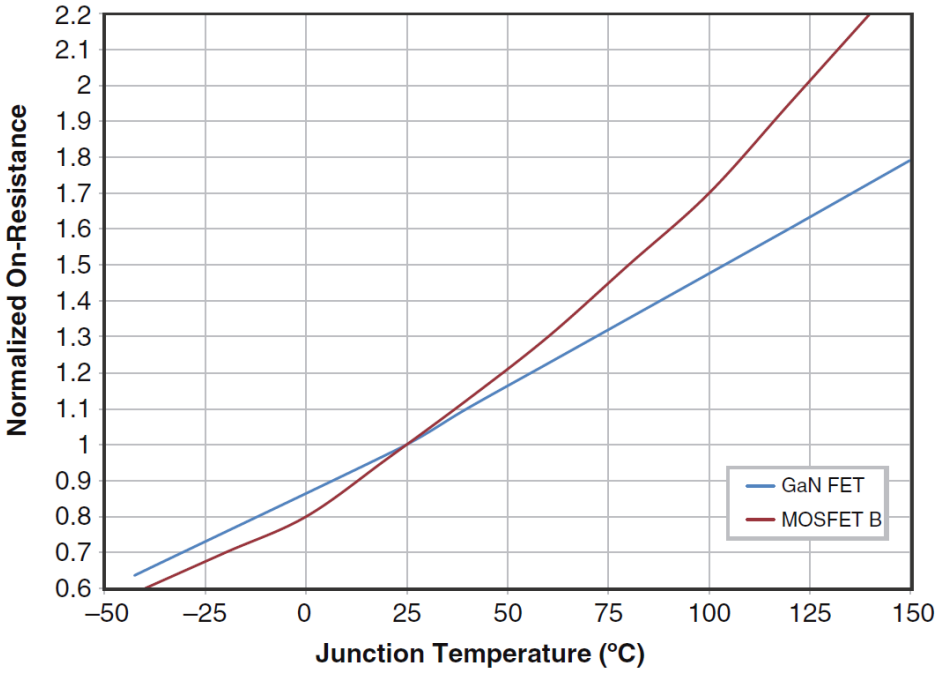


Figure 2-10: Normalized $R_{DS_{ON}}$ vs. temperature for a 100V enhancement-mode GaN transistor (EPC2010) compared with an Si power MOSFET with similar ratings [39].

As it can be observed, the normalised on-resistance is increased with the temperature for both, a GaN transistor and a power Si MOSFET. It can be seen that for temperatures below $25°C$ the MOSFET has lower on-resistance, but for higher

temperatures, the GaN device shows a lower $R_{DS(on)}$ value. It is also remarkable the lower variation with temperature of the resistance in case of the GaN device in comparison with the MOSFET. The reason why GaN transistors are much faster than MOSFETs lies in the fact that the theoretical on-resistance versus blocking voltage of GaN devices is at least three orders of magnitude lower than that of silicon [4].

2.4.3 Threshold Voltage V_{th}

As commented previously, the gate electrode is used to generate a Schottky barrier in GaN HEMTs which is able to control the carrier concentration in the channel layer below the interface. As the applied gate voltage decreases, the concentration of carriers below the gate terminal is decreased as well [13]. The threshold voltage for a power transistor is defined as the minimum gate-to-source voltage which is required to create a conducting path between the drain and source electrodes. That is, the required voltage level to turn-on the device.

Below the threshold voltage, the channel remains depleted of carriers, therefore blocking the current to flow between the drain and source electrodes. In case of a depletion mode HEMT, the threshold voltage is negative, and for enhancement-mode HEMT a positive threshold voltage is required.

The threshold voltage in GaN devices is produced when the 2DEG layer below the gate is completly depleted due to the voltage generated by the gate terminal. This phenomenon occurs when the voltage of the gate equals the volatge created by the piezoelctric strain in the AlGaN/GaN barrier. This voltage is compossed by the voltage applied externally to the gate (V_{th}) and the built-in voltage (produced by the characteristics of the gate material composition). Usually, the V_{th} of the AlGaN/GaN HEMTs depends on the epitaxial structure design (known as the Al composition), the doping concentration and the thickness of the AlGaN barrier [9]. Some mechanisms can be used to further modify the threshold voltage during the manufacturing process of the device, as for instance use a fluorine-based plasma treatment [7], where no change in AlGaN thickness is required and no reduction of the 2DEG density is produced.

The threshold voltage for enhancement-mode GaN transistors is lower than that of Si MOSFETs. This fact is due to the almost flat relationship between the temperature and the V_{th} together with the very low gate to drain capacitance. The device can start to conduct at low voltage levels, so care must be taken to prevent mis-operation caused by noise.

2.4.4 Parasitic Capacitances

The capacitances are used to determine the amount of charge that must be provided to the device terminals to change the voltage of the terminals. In fact, the amount of charge stored in the capacitor can be calculated by integrating the capacitance between the two terminals across the range of voltage applied to such terminals [27]. Therefore, the parasitic capacitances of a power transistor constitute an essential factor when analysing the energy required to turn-on or turn-off the device.

It can be distinguish three main different capacitances in GaN HEMTs: the gate-to-source capacitance C_{GS}, the gate-to-drain capacitance C_{GD} (also known as C_{RSS}) and the drain-to-source capacitance C_{DS}. A physical representation of these parasitics are depicted in the following figure:

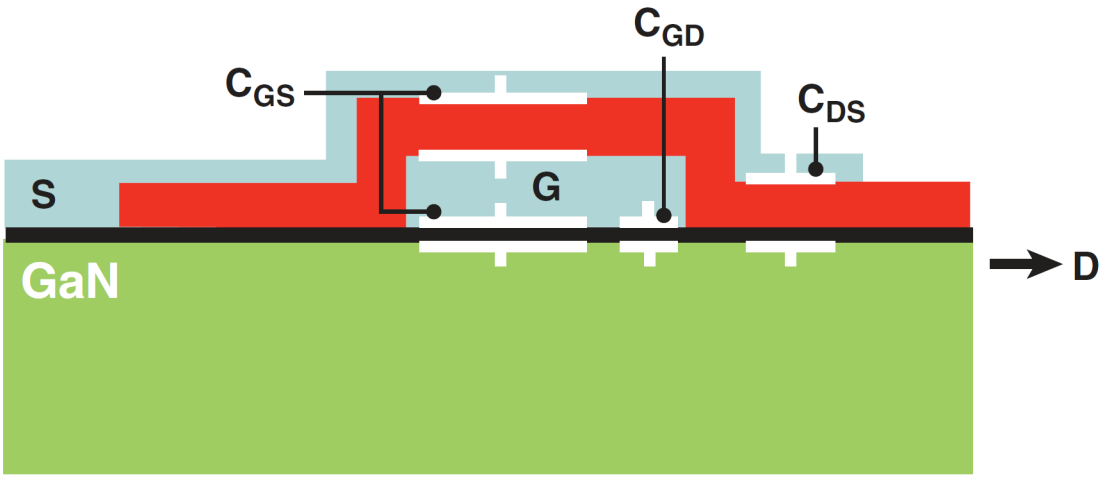


Figure 2-11: Schematic of GaN transistor capacitive sources [27].

It is normally interesting for the design and analysis of devices to group the capac-

itances in the input and output terminals: $C_{ISS} = C_{GD}+C_{GS}$ and $C_{OSS} = C_{GD}+C_{DS}$ (respectively). The gate-to-source (Q_{GS}) and gate-to-drain (Q_{GD}) charges are also of special interest since they are directly related with the device switching speed. There exists a parameter to analyse this effect: the Miller ratio, which is the quotient between (Q_{GD}) and (Q_{GD}). With this simple calculation it is possible to define the voltage at which the transistor will turn on.

Generally, the Si MOSFETs have larger parasitic capacitances than GaN devices. Normally, figures of merit (FOMs) consisting on the $R_{DS} \times Q_G$ are employed for comparing different MOSFET technologies with the GaN power devices. The results obtained show improvements of three to seven times.

2.4.5 Reverse Conduction of HEMTs

An interesting property of enhancement-mode GaN systems is the fact that they are naturally capable to conduct current in the opposite direction in the absence of a body diode [41]. This natural "body diode" effect and its variation with the drain current can be appreciated in the following figure:

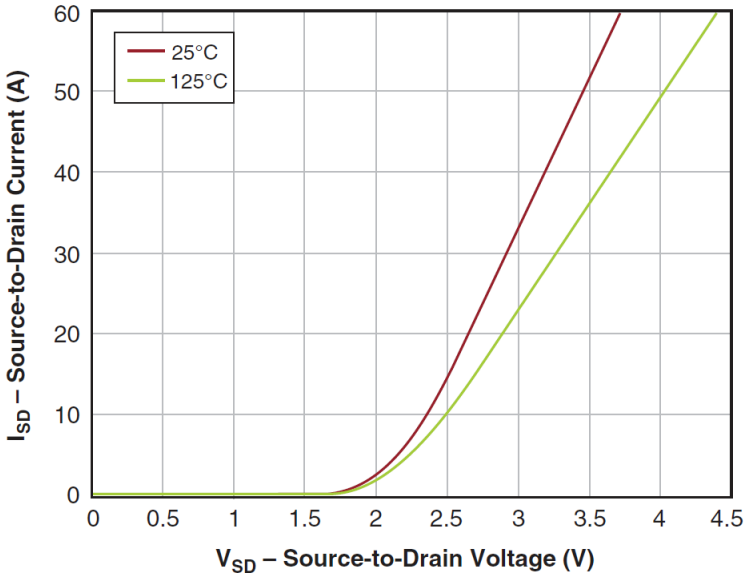


Figure 2-12: Body-diode forward drop vs. source-drain current and temperature by EPC2010 [39].

The condition for this phenomenon to occur is that the drain voltage must be higher than the gate voltage by at least the threshold voltage [27]. If this condition is satisfied, the 2DEG is restored under the gate channel (the 2DEG is turned on), and the current is able to flow from source to drain. Due to this fact, the forward voltage drop will vary with temperature. Notice that, if the gate voltage is decreased below $0\,V$, the forward voltage drop will augment proportionally.

Another significant parameter is the amount of charge which is dissipated when a body diode is turned on (Q_{RR}). Since e-mode HEMTs has no minority carrier conduction, the transistor will turn-off just when the forward bias between the gate and drain channels is removed. Therefore, there will not be reverse recovery losses. This feature can be really interesting in some power conversion applications, especially when comparing GaN HEMTs with Si power MOSFETs: the natural body diode has higher voltage drop but no reverse recovery charge relative to Si [38].

2.5 Gate Drive Voltage Considerations

As commented in previous sections, the control of the device (either for e-mode transistors or cascode configuration) is achieved by supplying or removing the gate charge from the gate electrode. Driving a cascode device is identical of driving a Si device. Even so, the technique for driving e-mode devices differs in some aspects and requires special considerations. The most important considerations are [14]:

- Low gate threshold voltage.
- Very small margin of applicable gate voltage.
- Parasitic effects.
- Layout considerations.
- dV/dt and dI/dt constraints.

Typically, for e-mode devices, the maximum gate-to-source voltage (V_{GS}) is not greater than $6\,V$, and around just $3\,V$ - $4\,V$ are necessary to fully turn the device on, which lead to a very small margin. Therefore, gate voltage ringing must be avoided, so device breakdown will not ocur. An important phenomenon is the presence of stray elements in the circuit, whcih can lead to oscillations on the gate voltage, particularly if there is a commom loop inductance between the gate and power loops. To solve this effect, GaN manufacturers provide e-HEMTs packages with kelvin connections for the gate loop, effectivly reducing or removing the common inductance. In contrast, cascode devices (which use a Si MOSFET to achieve normally off state behaviour) can be driven with around $20\,V$. On the other hand, the threshold voltage of the GaN is very low ($1 - 2\,V$), leading to the risk of unintentional turn-on of the transistor when the device is used in high dV/dt applications [10]. These gate voltage issues can be addressed by critical damping the gate-drive turn-on of the switching power loop. Notice that the turn-on and turn-off actions are different processes, so different damping requirements are necessary for each activity (use of independent gate resistors to adjust the turn-on and turn-off gate loop damping). In the Figure 2.13, a representation of the gate voltage versus time is included.

As it can be observed, different charge components are present. Particularly, four regions can be appreciated:

1. The charge required to bring the gate electrode up to the device threshold voltage, which will cause the drain-to-source current to start flowing (start of conduction).

2. The necessary charge to complete the current rise transition time (t_{CR}) and reach the Miller plateau voltage (V_{pl}).

3. The charge supplied to complete the voltage transition time (t_{VF}). The current provided to the gate terminal is used to discharge the gate-to-drain parasitic capacitance (C_GD), almost no current is used to charge the gate-to-source parasitic capacitance (C_{GS}). As a consequence, the Miller plateau appears.

4. The charge required to drive the gate to steady-state gate voltage.

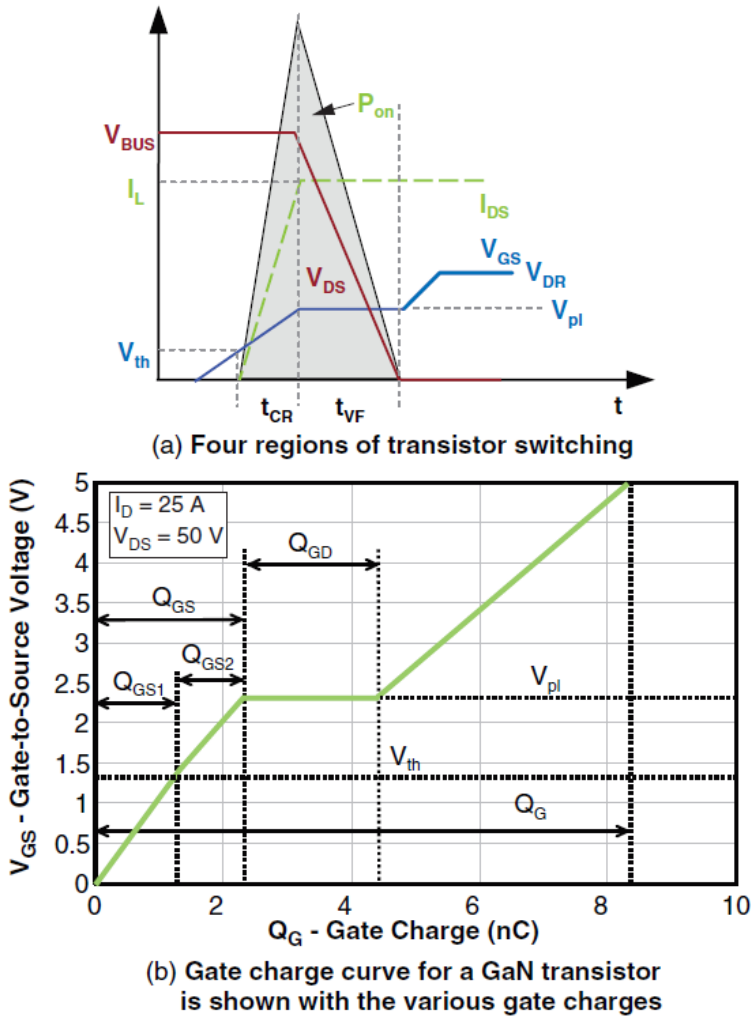


Figure 2-13: Gate charge vs. gate voltage showing different gate charge components for an EPC2010 GaN transistor [39].

Therefore, as Figure 3.13 shows, it can be noticed that the switching speed is dependant on the gate-to-source and gate-to-drain capacitances. The following modifications are expected in the switching waveform if the gate-to-source capacitance is increased [42]:

- An increase in the turn-on and turn-off delay between driver input and device output, as the time to charge the capacitor to reach the threshold voltage will last longer.

- Increased turn-on and turn-off time for the device drain current, since the time

to charge the capacitor to reach the Miller plateu from the threshold value will be increased as well.

- Increased operating time with increased on-state resistance, since it takes longer time to charge the capacitor from the plateau voltage to the steady-state value.

In the following table, a comparison of the gate characteristics of the GaN E-HEMTs with respect to Si MOSFETs, IGBTs and SiC MOSFETs is exposed:

Table 2.3: Gate drive voltages for GaN HEMTs, Si MOSFET, IGBT and SiC MOSFEt [48].

Gate drive voltage level	**GaN HEMT**	**Si MOSFET**	**IGBT**	**SiC MOSFET**
Maximum rating	-10/+7V	+/-20	+/-20V	-8/+18V
Transient maximum	-20/+10V		+/-30V	

As it can be checked, the gate voltages used to drive GaN HEMTs are different with respect to the technologies compared. A lower gate drive voltage is required, as commented before, with a lower voltage transient with respect to other technologies. The negative gate voltage in GaN HEMTs improves gate drive robustness but is optional. On the other hand, a much smaller gate-charge is required in GaN devices, since they do not have parasitic body diode, which implies lower drive losses, and faster rise and fall time.

Chapter 3

Theoretical Frame of the Analyses

In this chapter, the analyses performed to study the GaN devices experimentally and in simulation will be explained. In this project, the double-pulse test was used to analyse the GaN HEMT performance, and a synchronous-buck converter was used to test such devices in a real application. The initial idea was to perform more tests in other converter topologies, but due to the setbacks produced during the experiments it was not possible to carry out more analyses. The practical implementation of the performed tests will be also explained in this chapter.

3.1 Double-Pulse Test

3.1.1 Theoretical Background of the Double-Pulse Test

In order to analyse the switching transients and the switching power losses of the GaN transistors, the double-pulse test (DPT) has been used. The circuit used to perform this test is mainly composed by two power transistors, a DC voltage source (with a parallel capacitor) and an inductor as the load. This configuration is shown in the following figure:

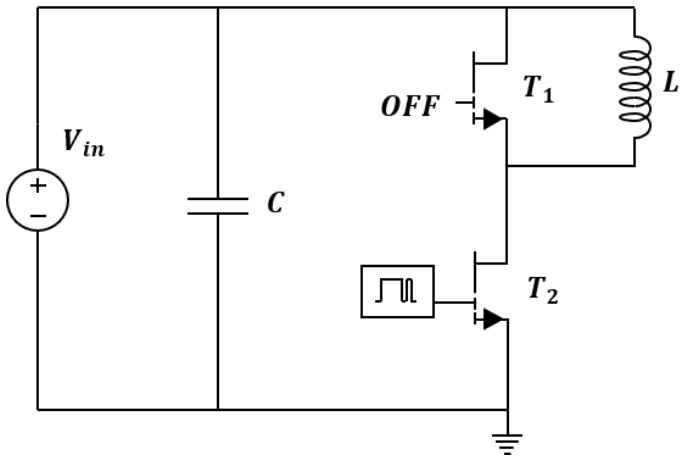


Figure 3-1: Double-pulse test circuit - Inductive load.

In this test, the upper transistor will be used to perform the function of a diode, since these devices do not need an anti-parallel diode. This means that the switching commands to the gate terminal of this transistor will never be forward biased, but reverse or no biased, depending on the E-HEMT desired operation (explained in Section 2.3).

The test is carried out acting on the lower device, just by using two pulses of different duration, therefore avoiding heating the device. The first pulse is used to increase the current through the load up to the desired test level, and thus be able to analyse the transistor turn-off behaviour at the end of this pulse. Then, a break is produced to give way for a second pulse, which is used to study the transistor turn-on. Notice that the sequence to perform this test must be large enough to provide time for the inductor to discharge, otherwise the load current could increase and damage the components. The ideal pulse waveform to perform the DPT is depicted in the Figure 3.2.

As it can be observed, the first pulse is a wide pulse used to charge the inductor, therefore reaching the desired current level to analyse the turn-on, while the second pulse is used to analyse the turn-off, so it is thinner. To reach the test current, it will be necessary to properly adjust the width of the first pulse commanded to the gate channel.

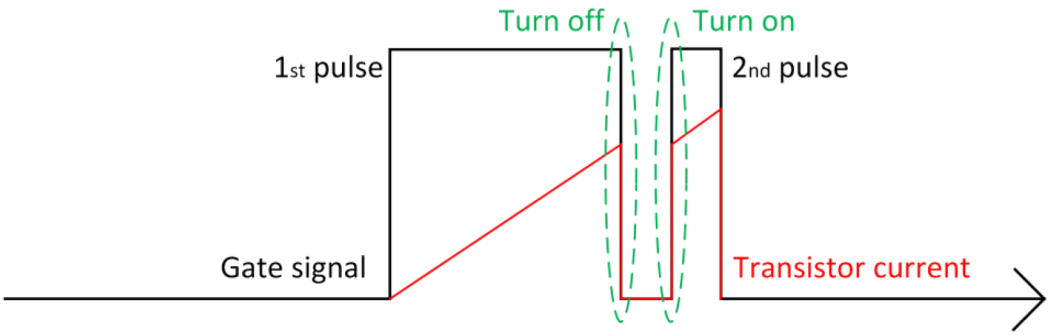


Figure 3-2: Double-pulse test signals - Inductive load.

3.1.2 Simulation Implementation of the Double-Pulse Test

For the simulation implementation of the double-pulse test, the power electronics software *PSIM*® (Version 11.1.3) has been used. Thanks to the latest improvements of this program, it is possible to model, simulate and evaluate the performance of real devices. This is possible due to the interface connection together with the simulating power devices software *LTSpice*® (Version XVII).

Different voltage waveforms have been used in order to create the different pulses (with their respective duration) to apply to the gate terminal. In the analyses, the first pulse duration has been varied for each test with the purpose of evaluating the switching transients during the turn-on and turn-off of the GaN device at different current levels. Particularly, the evaluated current values are comprised between 5 A to 30 A in steps of 5 A. Alternatively, the input voltage has been varied from 50 V to 300 V in steps of 50 V. In this way, for each evaluated voltage level, all the previously mentioned current values have been tested.

The key aspect of these analyses relies in the fact of using close-to-reality power devices. In the manufacturer web-page of the experimentally used GaN devices (*GaN Systems*) there are available the transistor SPICE models that allow the user to perform close-to-reality tests. As commented before, the characteristics provided in this files can be now used in *PSIM* in a similar way than in *LTSpice*. The user can easily create a subsystem to model the desired GaN transistor and link the required

characteristics to such subsystem by using a LTSpice netlist with all the required information.

As it can be observed in Figure 3.1, the upper power device is a GaN transistor too. In this case, such device is performing the function of the diode used typically in DPTs. As commented in previous sections, GaN devices do not have body diode, but thanks to the 2DEG they are able to conduct reverse current. Therefore, this upper transistor does not need to be driven by any gate voltage signal.

It is also important to include in the simulation model the parasitic elements that may have the mother board (PCB) used in the experimental results. In this case, the parasitic inductances have been included following the example available in the GaN Systems web-page of a double-pulse test simulation [45]. The rest of the parameters of the simulation have been selected according with the DPT implemented in the data sheet of the module used. They are described in the following table:

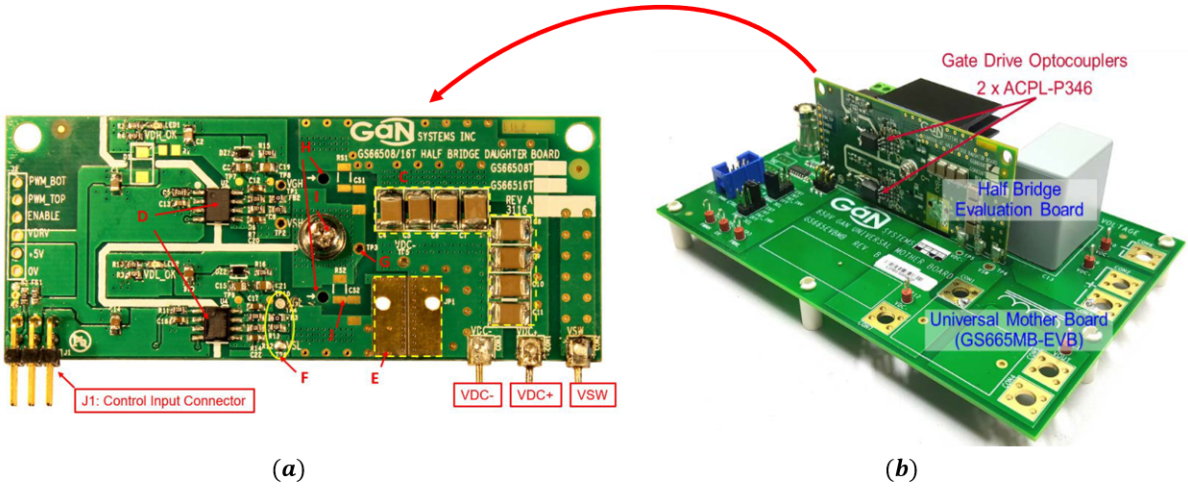
Table 3.1: Parameters used for the DPT simulations.

Parameter	**Value**
V_{test} *[V]*	50-300
I_{test} *[A]*	5-30
L_{test} *[μH]*	120
$R_{G_{ON}}$ *[Ω]*	10
$R_{G_{OFF}}$ *[Ω]*	2
V_{GS} *[V]*	+6/-3
L_G *[nH]*	0.5
L_{CS} *[nH]*	3

3.1.3 Experimental Implementation of the Double-Pulse Test

To perform the double-pulse test experimentally, the *GS66508T/GS66516T-EVBDB GaN E-HEMT* Daughter Board and the *GS665MB-EVB* Evaluation Platform was planned to be used at first. After performing the first test, at the lowest voltage level,

one of the power transistors exploded for no apparent reason. In fact, the pulses had not been commanded to the switches, only the DC-link voltage was activated, as well as the motherboard to power-up the drivers and the fan to cool the transistor. One of the main characteristics of this kit relies in the fact that, the daughter board (where the transistors are placed) can be easily removed from the motherboard, as shown in the following figure:



(*a*) (*b*)

Figure 3-3: (a) GS66508T/GS66516T-EVBDB GaN E-HEMT top side daughter board 650V. (b) GS665MB-EVB Evaluation Platform.

This feature allowed us to replace the damaged power transistor by a new and workable device. After that, all the conditions to perform the test again were examined in depth to avoid any type of failure: the pulses generated for the test, the connections from the pulses to the experimental kit, the DC-link voltage source, etc. However, this new device suffered the same issue than in the first case, it blew up in a similar way, just after power-up the motherboard and the DC-link voltage, but before commanding the pulses to the switches. At this point, it was clear that we had an issue somewhere in the assembly that had to be solved to perform the DPTs.

In the following figure, a scheme of the circuit that we had in the situation on which the transistors exploded is depicted:

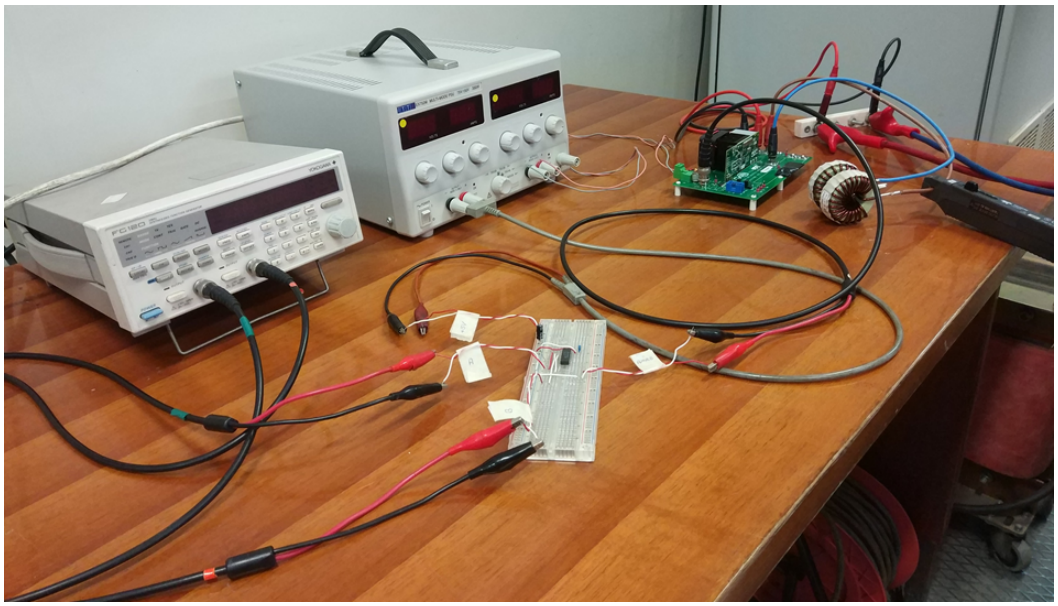


Figure 3-4: First assembly used to perform the double-pulse test.

As commented previously, there was no apparent reason for any of the transistors to suffer a failure before commanding the pulses, since an open circuit was produced, so no current could flow through the devices. After some days trying to investigate and identify the possible causes that could produce a fail that made the transistors to explode, it was found that, a critical point was the interconnection between the evaluation platform (where the transistors are located) and the motherboard (where the drivers and power circuit are placed). It was observed that such connection was really poor, since the evaluation platform and the motherboard were not firmly attached to each other. In fact, if the user touched the evaluation platform, it could be physically disconnected from the mother board. Of course, this fact supposed a huge problem, since the control is commanded to the motherboard and then, this signals are transmitted to the evaluation platform (and hence, to the devices) by means of a set of pins with a really unreliable, poor and dangerous conditions. This situation is shown in Figure 3.5.

From this circumstances, we noticed that the commanded pulses to the transistors could not be transmitted properly. It was highly likely that the switch was closed when the board was powered-up, thus creating a short-circuit and explaining the explosion of the device.

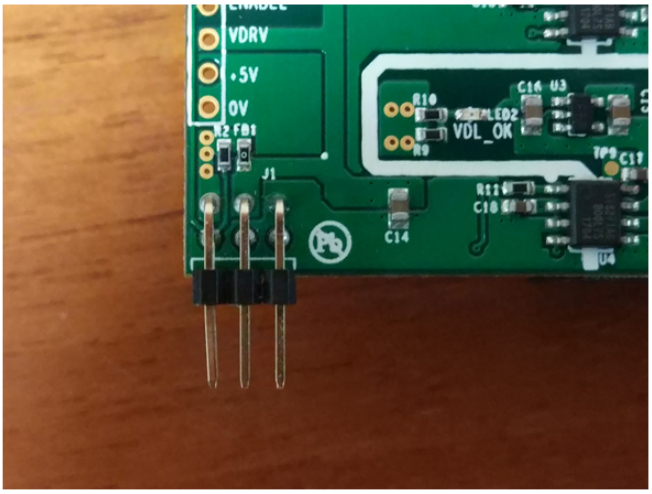


Figure 3-5: Poor pin connectors used to transmmit the control signals from the mother board (connected with the pulse source generator) to the daugther board.

Since this fact was a problem of the evaluation kit provided by the manufacturer and no easy solution was possible, we decided to contact the manufacturer commenting this issue, and to use another evaluation board for this test.

Experimental Evaluation Kit

To experimentally carry out the double-pulse test, the high power Insulated Metal Substrate (IMS) Evaluation Platform (from *GaN Systems*) and its corresponding motherboard GSP65HB-EVB was finally used. In the Figure 3.6, a representation of this kit is exposed.

This evaluation kit aims to provide good power density while simultaneously reducing the cost of the system. The IMS platform is used to cool the GaN Systems' bottom-side cooled power transistors. An IMS PCB is also known as Metal Core/Aluminum PCB [47]. This approach has been successfully used in automotive applications, industrial uses or energy storage systems.

As commented before, this evaluation platform consists up of a motherboard and two IMS evaluation modules, where the power devices are located. Each module is configured as a half-bridge and have a power rating of 4-7 kW. Therefore, by using

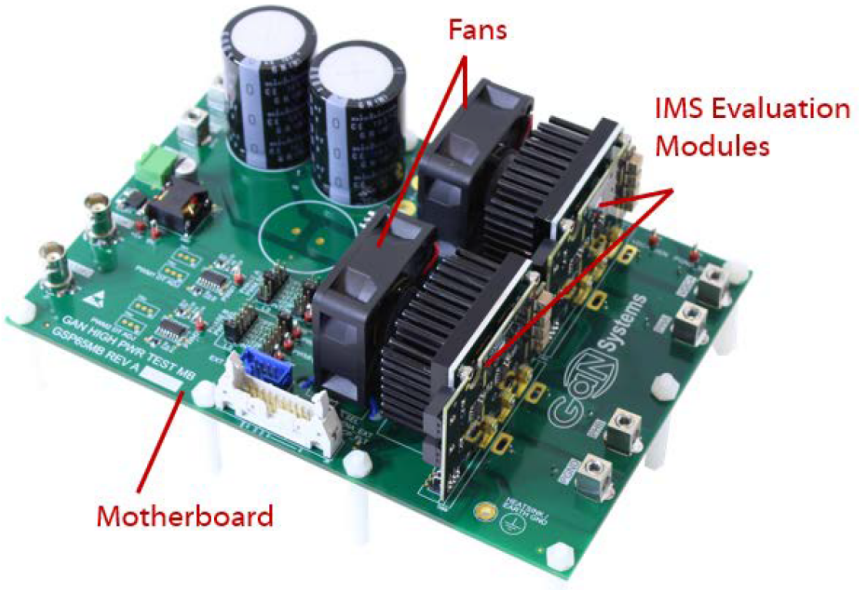


Figure 3-6: Experimental Evaluation Kit: GSP65RxxHB evaluation motherboard and 650V high power insulated metal substrate (IMS) evaluation modules.

the two modules it is possible to get a full-bridge configuration.

The used IMS evaluation module has the GaN E-HEMT rated at 650 V. The embedded GaN SMD package has the following features [47]:

- Dual symmetrical gate and source sense (kelvin source) for flexible PCB layout and paralleling.
- Large power source/thermal pad for improved thermal dissipation.
- Bottom-side cooled packaging for conventional PCB or advanced IMS/Cu inlay thermal design.
- Ultra-low inductance for high frequency switching.

The IMS evaluation module is composed by the GaN E-HEMTs, the gate drivers, the isolated DC/DC supply, the DC bus decoupling capacitors and a heatsink to form a fully functional half-bridge power stage. These modules are attached to the motherboard by using a vertical design concept (as shown in Figure 3.6), therefore achieving high power density.

The IMS board uses metal as the PCB core, typically aluminium. A dielectric layer and copper foil layers are bonded to the core. This configuration is shown in Figure 3.7, and it is commonly used in high power applications and high current applications where most heat is concentrated in a small footprint SMT device, since it offers superior thermal conductivity.

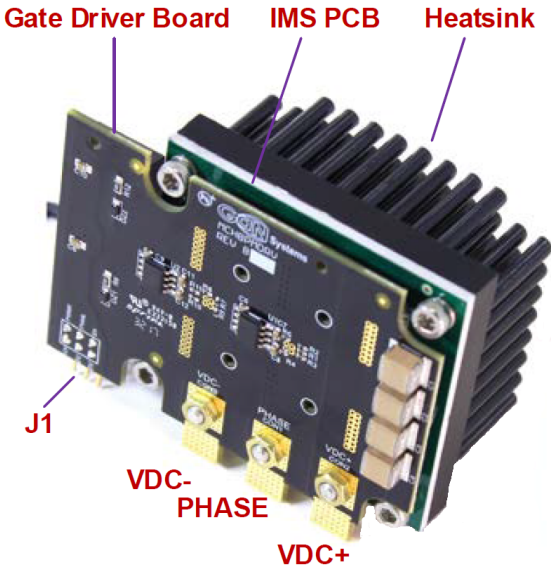


Figure 3-7: Insulated metal substrate (IMS) evaluation module used in the motherboard.

Since GaN technology is being adopted widely, the industry is trying to avoid through-holes (TH) packaging, and introducing surface mount packaging (SMT), as is the case of this manufacturer. Traditional TH devices produce high parasitic inductances and capacitances that can be avoided with SMT components, achieving better performances. These packages offer low inductance and low thermal impedance, enabling efficient designs at high power and switching frequencies.

In SMT devices, the thermal management must be approached differently than in TH transistors. In the latter case, the packages are cooled by attaching them to a heatsink, with an intermediary Thermal Interface Material (TIM) layer of electrical high voltage insulation. On the contrary, SMT power devices are cooled by using thermal vias tied to multiple copper sheets in a PCB. The IMS board presents another option which achieves a much lower junction to heatsink thermal resistance thanks

to the design commented in the previous paragraph. This fact allows a more efficient heat transfer out of the transistor, and is suitable for SMD devices intended for high power applications.

Other important characteristics of the module are described below:

- The half-bridge configuration (one leg composed by two transistors) is designed in a two-board assembly in order to address the drawbacks of implementing the design on a single layer IMS board. The gate drive circuitry is mounted on a multi-layer FR4 glass-reinforced epoxy material. On this PCB, the gate drivers ICs are included, as well as the isolated DC/DC converter to power the driver IC, and DC decoupling capacitors. On the contrary, the GaN E-HEMTs are assembled on the IMS board.

- To attach the IMS board to the FR4 driver board, small pitch low profile SMT headers are used. The short loop lengths reduce the parasitic gate inductances.

- It is well known that a large copper area helps to maximise the heat transfer to cool the devices, but the area of copper at the switch node (high dv/dt) needs to be minimised to reduce the parasitic coupling capacitances to the metal substrate. An IMS board with thicker dielectric layer was chosen to reduce this effect.

Another important feature of the experimental kit is the external PWM and control Input/Output (see Figure 3.8). As it can be seen, the PWM pulses can be commanded to the motherboard by two different mechanisms:

- PWM Input: In this case, the PWM pulses are commanded to the power devices by means of an external signal generator source. As it can be observed in the figure, there is also an integrated circuit responsible for the dead-time generation between transistors of the same leg. The duration of the dead-times in this case is controlled by selecting the value of a resistor included in the assembly.

- External PWM and control Input/Output (I/O): This pins control different functionalities of the board by means of an external DSP. As it can be observed

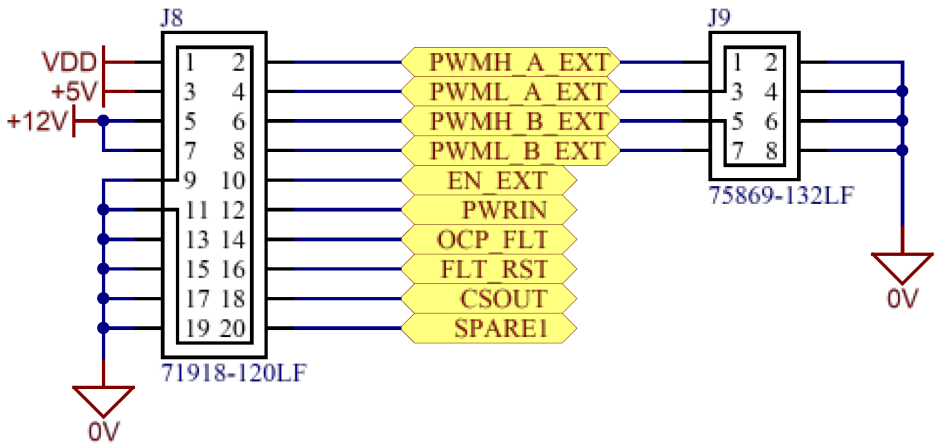


Figure 3-8: Pin connectors used to transmit the pulse signals to the gate drivers of the GaN HEMTs from the motherboard to the IMS.

in Figure 3.8, it includes the control of the PWM signals, the enable of these signals, current sense control, over current protection control, etc. For this project, just the PWM signals and the enable will be used.

In the case of the external PWM and control I/O pins, an interface between this ports and the DSP was necessary. The optimal solution would have been to use optical fiber to transmit the PWM and control signals from the DSP to the evaluation kit. However, this material was not available in the laboratory, so other solution was necessary. The most suitable solution with the available material was to use thin cables connected at the output pins of the DSP through individual headers for each cable, and connected to the motherboard by a female connector for the 20 pin header.

Notice that, to prepare the cables for this interconnection, it was necessary to first remove the insulator at both extremes of the cable, then to place the conductive header at the bare part and press it to attach it to the cable, and finally to place an insulator in the header part (attached by applying heat) to avoid electric contact between pins which could produce a short-circuit.

Unfortunately, when the PWM signals were checked in the motherboard (without powering-up the assembly), it was noticed that the PWM commands did not provide required dead-times and shapes due to the increased inductance created by these

thin cables to transmit the gate commands. Therefore, the length of them was highly reduced, minimising the distance between the DSP and the gate drive circuit. Even so, the optimal solution would have been to use optical fiber, as explained before.

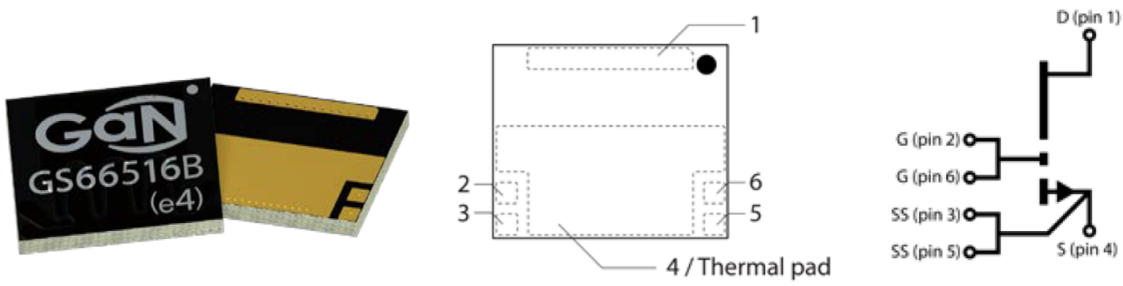
3.1.4 Characteristics of the GS66516B HEMTs

As commented before, the used GaN High Electron Mobility Transistors are provided by the manufacturer GaN Systems. In the following table, the main characteristics of these devices are presented:

Table 3.2: Parameters used for the DPT simulations.

Parameter	**Value**
Rated voltage [V]	650
Rated current ($I_{DS_{max}}$) [A]	30
$R_{DS_{ON}}$ *[mΩ]*	25
V_{GS} *[V]*	+6/-3
Transient tolerant gate drive [V]	-20/+10
Very high switching freq [MHz]	> 10
Small PCB footprint [mm^2]	11 x 9

As it can be observed in Figure 3.9, these power transistors use a smd technology. They are enhanced mode gallium nitride (GaN) on silicon power transistors. The properties of GaN allow for high current, high voltage breakdown and high switching frequency. The used small packages enable low inductance and low thermal resistance. Thus, device is a bottom-side cooled transistor which offers a very low junction-to-case thermal resistance for high power demand applications [46]. This combination of features allows to achieve very high power switching efficiency. Furthermore, no wire bond is used, so high reliability is achieved.



(*a*) (*b*) (*c*)

Figure 3-9: (a) SMD package for the used GaN HEMTs. (b) Terminals of the used GaN HEMTs in relation with (c), which shows the electrical symbol representation of the trnasistor.

In practice, these components are suitable for the following applications: high efficiency power conversion, high density power conversion, AC/DC converters, synchronous buck or boost converters, uninterruptible power supplies, industrial motor drives, solar and wind power, fast battery charging, traction drives, etc.

Gate Drive

In order to achieve an optimal $R_{DS(on)}$ and a long live, the recommended gate drive voltage is $0\,V$ to $6\,V$. The gate drive is able to withstand transients up to $+10\,V$ and $-20\,V$ for pulses up to $1\,\mu s$. If $6\,V$ gate drive voltage is used, the enhancement mode high electron mobility transistor (E-HEMT) is fully achieved and reaches its optimal efficiency. Lower voltage can lead to a lower efficiency. GaN systems do not require negative gate bias (as commented in Chapter 2) to turn-off. Negative gate bias ensures safe operation against the voltage spike on the gate, however it increases the reverse conduction loss [46]. Gate drivers with low impedance and high peak current are recommended for fast switching speed. An external gate resistor can be used to control the switching speed and slew rate.

Parallel Operation

In the case of these devices, special care must be considered in the driver circuit and PCB layout since the device switches at very high speeds (high dv/dt). It is recommend to design a symmetric PCB layout and equal gate drive loop length on all parallel devices to ensure balanced dynamic current sharing.

Source Sensing

This device has two dedicated source sense pads. The used package utilizes no wire bonds, so the source connection results in a very low inductance. Remember that, the common source inductance causes gate ringing and gate oscillations, and it is produced after the source terminal of the transistor. The dedicated source sense pin enhances the performance by eliminating the common source inductance if a dedicated drive signal kelvin connection is created [46]. This can be achieved by connecting the gate drive signal from the driver to the gate pad on the GS66516B and returning the source sense pad on the GS66516B to the driver ground reference.

Thermal

The substrate of these components is internally connected to the source/thermal pad on the bottom-side of the GS66516B. The design of the transistor aims to cool the device by using the printed circuit board. The drain pad is not as thermally conductive as the thermal pad. Even so, adding more copper under the drain pad will improve the thermal performance, since the package temperature is reduced.

Reverse Conduction

As commented in previous sections, GaN HEMTs do not have intrinsic body diode. However, they are naturally able to provide reverse conduction and exhibit different features depending on the gate voltage:

- On-state conduction ($V_{GS} = +6\ V$): The reverse conduction in on-state is similar to that of the silicon MOSFET, with the I-V curve symmetrical about

the origin, providing a similar $R_{DS(on)}$ than the forward conduction operation.

- Off-state conduction ($V_{GS} \leq 0\,V$): the features of GaN devices when off-state is present are different form silicon MOSFETs, as the GaN device has no body diode. In the reverse direction, the transistor starts to conduct when the gate voltage (V_{GD}) exceed the gate threshold voltage. This characteristic can be modelled as a body diode with slightly higher V_F and no reverse recovery peak charge. Notice that, if negative gate voltage is applied in this state, the source-to-drain voltage must be higher than $V_{GS(th)}+V_{GS(off)}$ in order to further turn-on the device. This phenomenon produces an additional reverse voltage drop V_F, therefore increasing the conduction losses.

Blocking Voltage

The blocking voltage (V_{BD}) is defined by the drain leakage current. The unrecoverable breakdown voltage is approximately 30% higher than the rated V_{BD}. Maximum drain-to-source rating is $650\,V$ and doesn‘t change with negative gate voltage. A transient drain-to-source voltage of $750\,V$ for $1\,\mu s$ is acceptable. Notice that GaN HEMTs do not have avalanche breakdown.

3.1.5 Tests with the Signal Generation Source

The first approach to perform the DPTs experimentally was based on a Direct Digital Synthesis (DDS), which is a technique employed by frequency synthesizers with the purpose of creating an arbitrary waveform from a single, fixed-frequency reference clock [35]. That is, to use a signal generator to create the two pulses necessary for the test. This device can be set in a mode that allows the user to trigger an event of a certain frequency and phase (such that, the duration of the pulse can be determined) when a certain button is pressed. Then, it could be activated manually. In addition, the source was equipped with two output channels. This characteristic was a perfect solution to create the two pulses by using a OR gate, as depicted in the figure below:

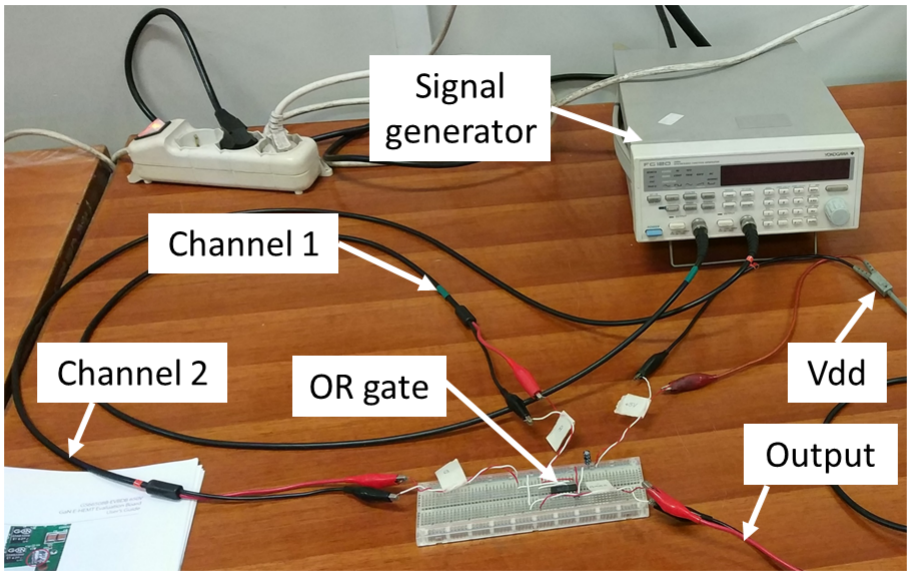


Figure 3-10: Assembly used to create the required double pulses to perform the double-pulse test with the signal generator and the OR gate.

The reason why the OR gate should be used, is because the pulse generator can generate an signal each time the trigger button is pressed (of a certain phase and frequency), but the DPT requires two pulses of different duration, so two channels and an OR gate are required to get a single output signal, as a result of the effect of the OR gate over the used input signals. Of course, it is necessary to determine in the most accurate way the delay between the two signals, and the frequency and phase of both pulses to achieve the desired conditions for the test (see Figure 3.11). For this reason, each of these parameters should be modified after each test, since different current and voltage levels were planned to be tested. A MatLab script was used to automatically calculate the required parameters to set in the pulse generator for all the desired conditions.

Unfortunately, after performing a few DPTs, it was noted that, when the phase-shift between both signals was larger than a certain value, the signal generator did not provide the expected pulses durations. In this conditions, it was not possible to

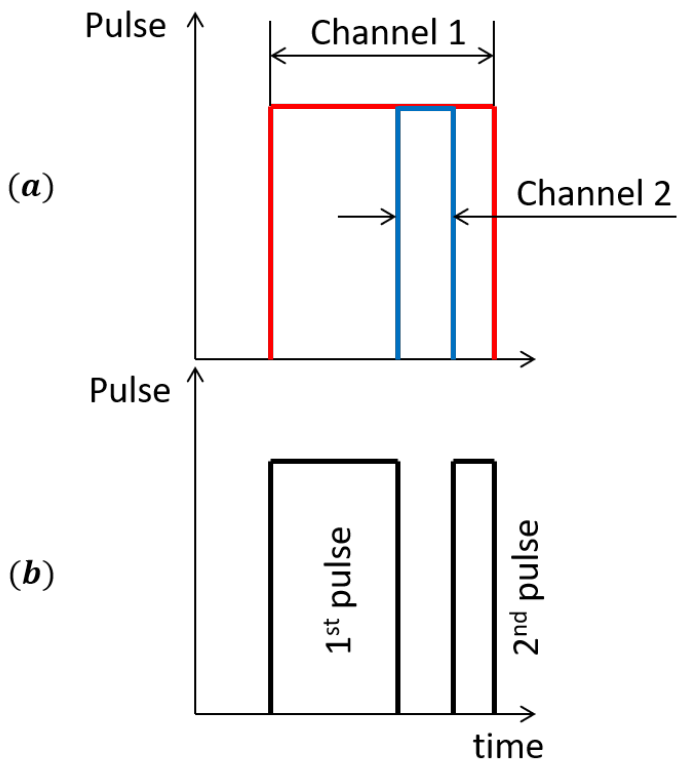


Figure 3-11: (a) Commands produced by the generator source channels. (b) Pulses produced by combining the signal generator commands and the OR gate.

continue with the tests, since the currents obtained did not match with the desired values, and most important, some of the components of the IMS evaluation platform could be damaged if the maximum current level of 30 A was exceeded.

3.1.6 Tests with the DSP

To carry on with the DPTs, since there were no more signal sources available in the laboratory, a new solution to generate the pulses was necessary. At this point, to program a microcontroller was the best option.

For these tests, just one phase of the experimental kit is needed, which implies to deal with two transistors: the upper transistor (which does not require any gate drive signal) and the lower transistor which represent the evaluation power device of the DPT. Therefore, it is necessary to command the two required pulses to turn-on

and turn-off the lower switch. In order to generate the gate pulses, a digital signal processor (DSP) from *Texas Instruments* was employed. Particularly, the DSP model *TMS320F280335* together with the *C2000 DIMM100 Experimenter's Kit* was used for that purpose. At first, it was studied to produce the pulses with the ePWM module of the DSP, but the required signals can be easily generated by using the General Purpose Input/Output (GPIOs) pins of the experimental board. Then, that signals can be transmitted to the IMS platform by using a flat cable and an IDC connector which stablish connection between the DSP experimental kit pins and the IMS board.

The high state of the commanded pulses has a voltage level of around $4\,V$, and a low state of $0\,V$, which is suitable with the IMS board requirements. Then, such board commands the required gate voltage levels ($+6\,V$ and $-3\,V$) to the transistor by means of the isolated DC/DC converters and the gate drive circuits (fed at $12\,V$ and $5\,V$ respectively).

The software used to program the DSP was *Code Composer Studio* (CCS - Version 5.5), which uses C as programming language. The idea used to generate the DPT signals was simple: set the required GPIOs as outputs, keep the necessary pin in high-state the required time for the first pulse, clean it (set it at low state) for the transition time between the two pulses, set again such GPIO as high to command the second pulse, and finally clean it again. To keep the pulses in high or low state, a delay function was used. Initially, an interrupt function was created and tested, but the times between interrupts provided by the DSP was not suitable for this test. Then, the delay function already included in CCS and created by TexasInstruments was checked. But the minimum delay time that this function was able to generate was $1\,\mu s$, and shorter delay times were necessary to achieve the different current levels. Therefore, a new delay function was created, based on a for loop on which a defined variable increases its value at the selected microcontroller speed. In this way, it was possible to estimate the necessary loop duration (loop condition) to generate the required delay time.

Notice that this test cannot be performed repeatedly without enough separation

between consecutive tests. Otherwise, the inductor current will increase more each repetition and the devices would be damaged when reaching a certain current level. For that purpose, a variable was included in the code to generate the pulses, in such a way that just the user can produce the pulses when that variable is modified by hand from 0 to 1. In this way, once the user presses the "play" button, all the required GPIOs related to the PWM input signals of the evaluation platform are set automatically in the low state to have a safe state and ensure no undesired gate terminal commands which could activate the transistors and damage some component. Alternatively, the "enable" port (see Figure 3.8) is set as low initially to avoid any undesired PWM signal that could be commanded from the DSP through the flat cable to activate the switches. Therefore, once the program is running, it is "doing nothing", and to generate the pulses, the user has to manually change the state of the previously commented variable.

In Figure 3.12, a representation of the code execution is depicted. As it can be observed, the program is doing nothing in a while infinite loop until the variable which enables the generation of the pulses is modified. Once the pulses have been created, the variable is set again to its initial state. Notice that the user can also change the value of the first pulse duration while running the program, so that the DPTs can be rapidly done for different current values.

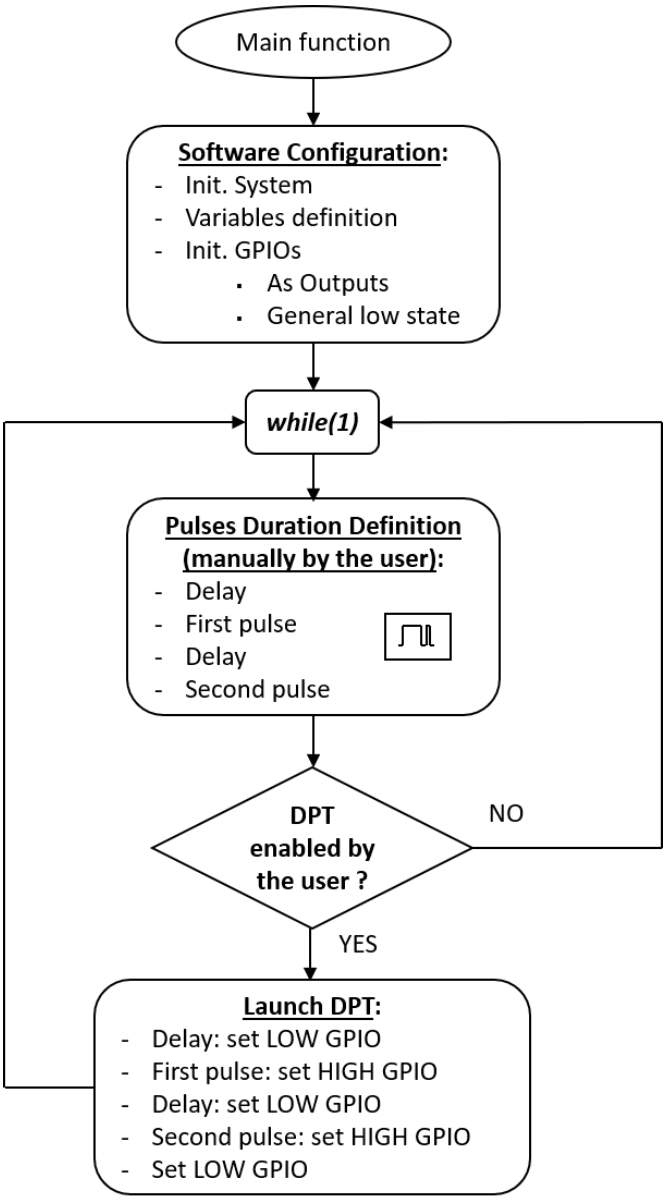


Figure 3-12: Flow chart of the program created to generate the pulses for the double-pulse test.

3.2 Buck Converter

3.2.1 Operation of a Buck Converter

A buck converter, also known as step-down, is a DC/DC converter. This topology is constituted fundamentally by a switching transistor S, a diode D, an inductor L, an output capacitor C and the load R_L. The buck converter is used to cut down the input voltage V_i and reduces the output voltage V_o as a function of the duty cycle employed in the control of the power transistor. In the following figure, a representation of a buck converter is shown:

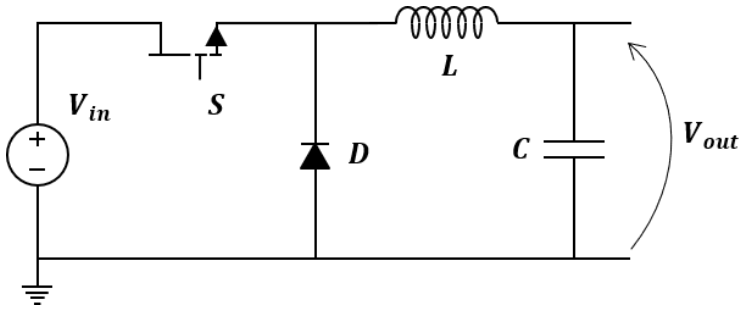


Figure 3-13: Electrical scheme of the buck converter.

The transistor as well as the diode represent the switching network of the circuit. Particularly, the switching network cuts down the input voltage and produces a square waveform applied to the input of the $L-C-R_L$ low pass filter. This filter converts the square waveform into an average output voltage and current. The power transistor is controlled by using Pulse Width Modulation (PWM), which switches the device ON and OFF at a determined switching frequency. The duty cycle is determined by:

$$D = \frac{t_{on}}{t_{on} + t_{off}} = f_s \times t_{on} = \frac{t_{on}}{T} \tag{3.1}$$

In the figure above, the gate driver is represented by its ideal Thevenin's equivalent voltage source V_{GS}. Typically, the buck converter is difficult to drive due to the fact that the gate of the transistor is not referenced to ground. This topology is operated at hard switching, since the transistor driver voltage is squared and the device is

turned-on at high voltage. The buck converter is able to operate either in continuous conduction mode (CCM) or in discontinuous conduction mode (DCM). In this report, the converter will be analysed in CCM.

In the following figure, a representation of the circuit in ON and OFF state is depicted:

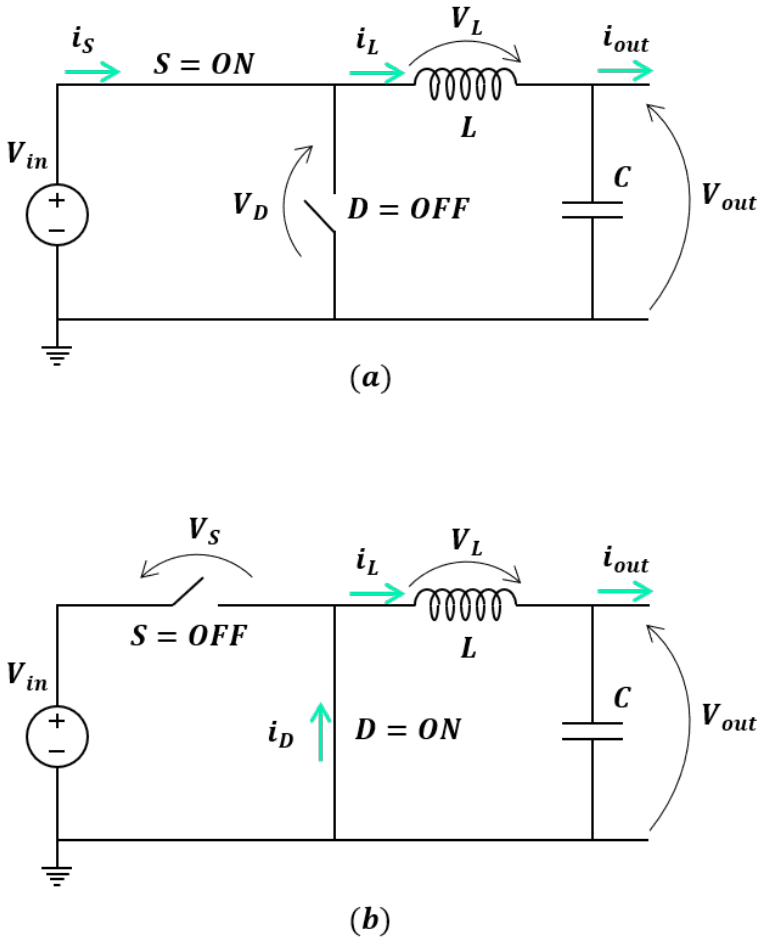


Figure 3-14: Equivalent circuit of the buck converter when operating in CCM: (a) Switch = ON and Diode = OFF; (b) Switch = OFF and Diode = ON.

The operating principle of the buck converter is represented in Figure 3.15, where. In the following paragraphs, an explanation of the two states is given:

- $T = ON$: At time $t = 0$, the driving voltage applied to the switch turns the device on. The inductor current starts to increase with a positive slope $V_i - V_o/L$,

in accordance with the voltage equation of an inductor $v_L = L \cdot di_L/dt$. During this interval, the inductor current circulates through the transistor, in such a way that the current of the device is equal than that of the inductor ($i_S = i_L$) [21].

- $T = OFF$: In this portion of the period, the driving gate voltage is applied in such a way ($0\,V$ or negative depending on the type of switch) that the power transistor is turned-off. In CCM, the inductor current will continue flowing in the same direction and will never become $0\,A$. The difference with respect to the previous state relies in the fact that now the inductor is providing energy, so the inductor current slope will be negative. In this way, the diode will be turned-on and the transistor now blocks a voltage equal to V_i. Since the source is disconnected from the circuit during this interval, the inductor together with the output capacitor maintains the output voltage V_o and output current I_o.

In this way, the switching network (composed by the power transistor and diode) converts the feeding voltage V_i into a square waveform applied to the input of the $L - C - R_L$ filter. This second order low pass filter converts the square waveform into a DC output voltage with a certain ripple (as small as possible). Notice that the average output voltage V_o is equal to the square wave average. The ON time of the switching transistor determines the width of the square waveform, and it is controlled by the duty cycle [12]. The input and output voltage are directly related by the duty cycle: $V_o = d \cdot V_i$, therefore being the variable factor that determines the output voltage level (for a given input voltage). Of course, the duration of the transistor ON state is also directly related with the amount of energy that can be transferred from the input source V_i to the output load R_L. In theory, the duty cycle can be varied from zero to 100%, but in the practice, the real range of variation for the duty cycle is from 5% to 95%. This means that the output voltage is inside the following range: $V_o \, \epsilon \, V_i \cdot (0.05 - 0.95)$. Another important aspect to consider is the maximum voltage that the switch will withstand, which in case of the buck converter is equal to the input voltage ($V_{DS} = V_i$).

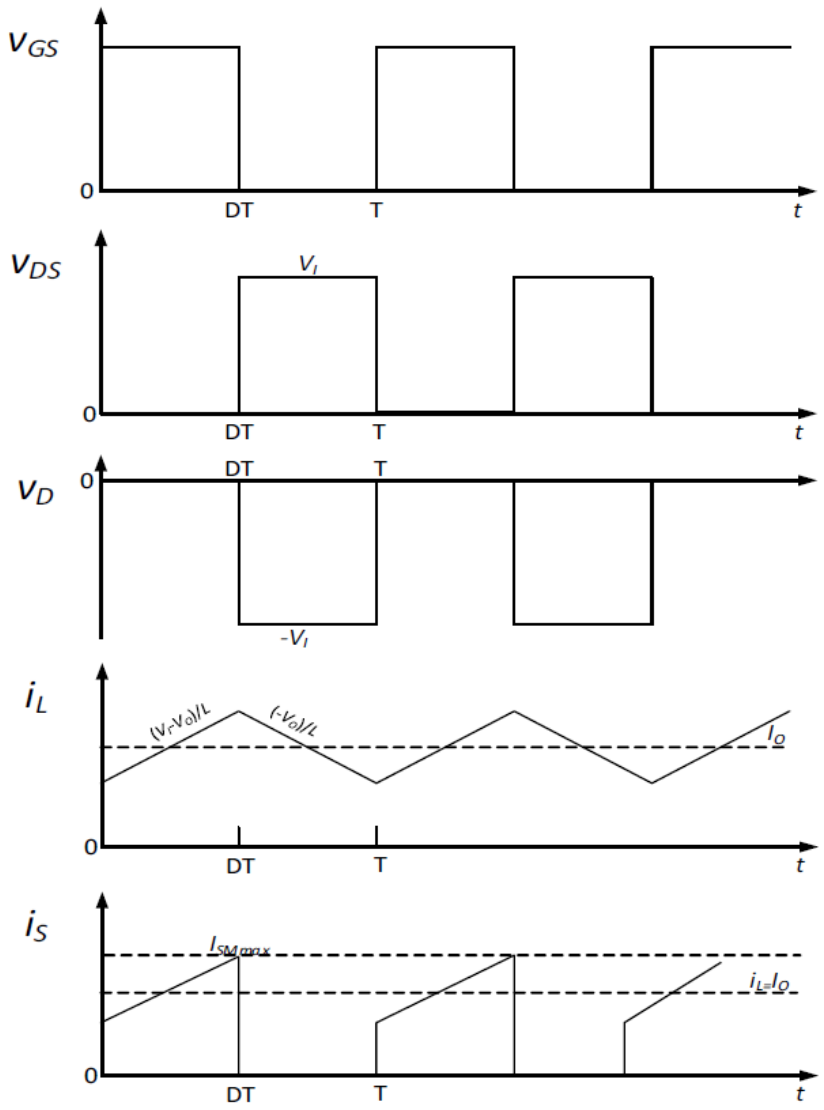


Figure 3-15: Buck switching waveforms corresponding to the two possible states when operating in CCM.

3.2.2 Synchronous Buck Converter

One of the most important aspects and trends in power electronics is to improve as much as possible the efficiency of the power converter. For this purpose, designers and researchers are continuously investigating new solutions that allow to create more efficient power converters trying not to increase the cost. This purpose is fundamental especially in applications where reducing power consumption by one watt means to save megawatts from the grid.

The synchronous rectification represents one of the solutions that have been recently developed by the semiconductor industry. The low cost DC/DC converters that employ synchronous rectification can achieve better efficiencies than those converters which do not use synchronous rectification. In a buck converter, the main difference between both variants is that the synchronous rectification converter uses a second power transistor instead of the power diode. This new transistor needs to be properly driven with the required dead-time in order to avoid a short-circuit that could seriously damage some component. The main advantage in a synchronous rectifier is that the voltage drop across the low-side transistor can be reduced with respect to the voltage drop across the diode of a non-synchronous buck converter. If there is no change in the current level, a lower voltage drop means that less power dissipation will be produced and a higher efficiency will be achieved [36].

As explained in previous sections, the non-synchronous uses a power diode, which must satisfy the specific reverse voltage value and the forward voltage drop requirements. These are the necessary specifications that the designer must consider when selecting the power diode. When the buck converter is operating at low duty cycles (close input and output voltage values), the power diode operate as a catch diode. In this situation, the diode conducts more current than the high-side power transistor, increasing the so-called conduction losses in the diode. Due to these conduction losses in the diode, the converter efficiency could be reduced. In [43] explains that generally, the use of a power transistor instead of a diode can reduce the voltage drop from $0.5\,V$ to $1\,V$ of a diode to a value of $0.3\,V$ or even less when using the transistor. This in turn increases the efficiency of the converter by a 5% or more [17].

Alternatively, the previous considerations must be take into account also for a switching transistor when a synchronous-buck converter is employed. Additionally, the complexity of the control is increased, since it is necessary to ensure that both transistors are not conducting simultaneously to avoid a direct path from the input to the ground.

3.2.3 Design of the Buck Converter

At the beginning, it was expected to perform several buck converter tests in several conditions. For that purpose, different DC-link voltage levels (from $50\,V$ to $300\,V$ in steps of $50\,V$) and resistive loads were studied. The idea was to use the material available in the laboratory as far as possible.

Resistor selection

In case of the resistive loads, there was available a resistor bank, composed of a total of 14 resistors of $24\,\Omega$ each. Hence, it was possible to design different combinations of resistors (in series and / or in parallel) to achieve the desired resistance values for the test. However, the bank was quite old, and some of the resistors were not providing the expected values, so it was necessary to measure all of them with an ohmmeter to check their resistance values. It was also necessary to consider possible variations of the values due to thermal changes during the test. Once everything was checked, a Matlab script was created to define all the possible combinations to get the desired load values.

Inductor selection

In case of the inductor included in the buck converter, there were several options available in the laboratory, but some of them were not suitable for the test, or were devices without a label defining the inductance value, since they were recycled from other finished projects, or were quite old. For this reason, it was necessary to measure their values. In case of the inductor, the procedure to define its value was not as easy as the resistor because the device to measure its value was not available in the laboratory. Hence, another mechanism was necessary. The idea was to create a very simple electrical circuit that allows to observe with the oscilloscope the slope of the inductor current for a given voltage, and hence obtain the di/dT relation. With this information, it is possible to determine the inductor value. In the following figure, a representation of the circuit used is included:

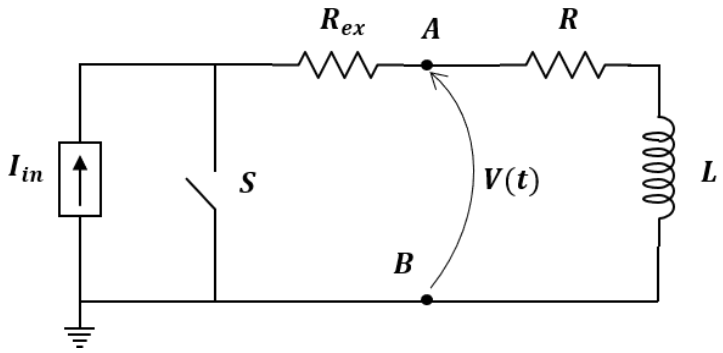


Figure 3-16: Circuit used to determine the value of the available inductors.

As it can be observed, the circuit is composed by the inductor that will be measured (L); the associated resistance of the coil (R); a resistor which provides a resistive load which will dissipate energy in terms of heat (R_{ex}); and a current source which allows to force a continuous current flow throw the circuit. Notice that the internal inductor resistance can be neglected in the calculations, since it is very small and it will practically not affect the results.

To perform the test, the source is configured at a voltage of $33\,V$ (it depends on the R_{ex} value) and a maximum constant current of $1\,A$. Once the source is turned-on and the switch is open, the defined voltage and the circuit parameters will determine the flowing current. When the switch is closed, a short-circuit is produced, leading to a situation on which the voltage provided by the source will be theoretically $0\,V$ (in practice very close to $0\,V$), and the current will be set by the maximum upper limit programmed in the current source. To carry out the test, once the source is turned-on, the switch must be closed. This condition leads to a flowing current of $1\,A$ through the inductor and $\sim 0\,V$. When the switch is opened the current decreases to the value defined by the voltage source and the resistor R_{ex} (mainly). But the rate is defined by the inductor, and can be observed with the oscilloscope. Hence, with this information it is possible to obtain the inductance value by using the following equation:

$$V_L(t) = L \cdot \frac{di(t)}{dt} \rightarrow L = V_L \cdot \frac{\Delta t}{\Delta i} \tag{3.2}$$

Several inductors were evaluated in the laboratory, and the most suitable value for the planned buck converter test was: $L = 1\,mH$. In the following figure, a representation of the real circuit used for this study is shown, as well as the results obtained from the oscilloscope:

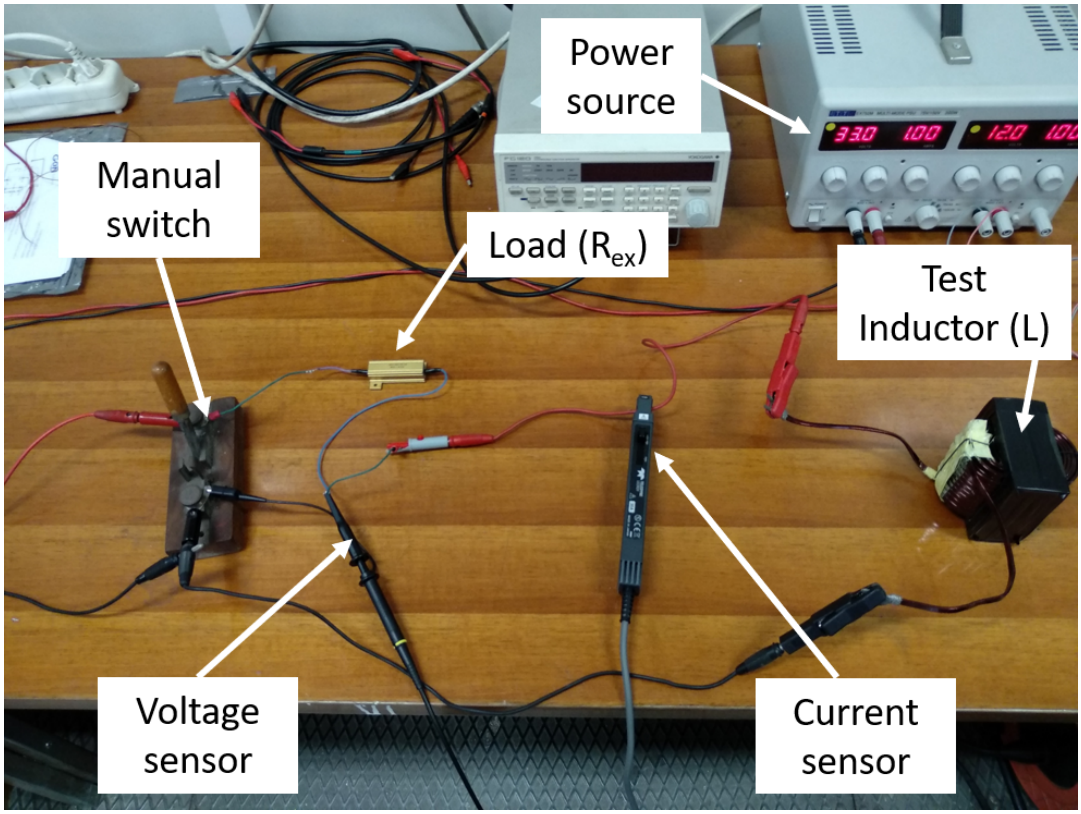


Figure 3-17: Real circuit used to determine the value of the available inductors.

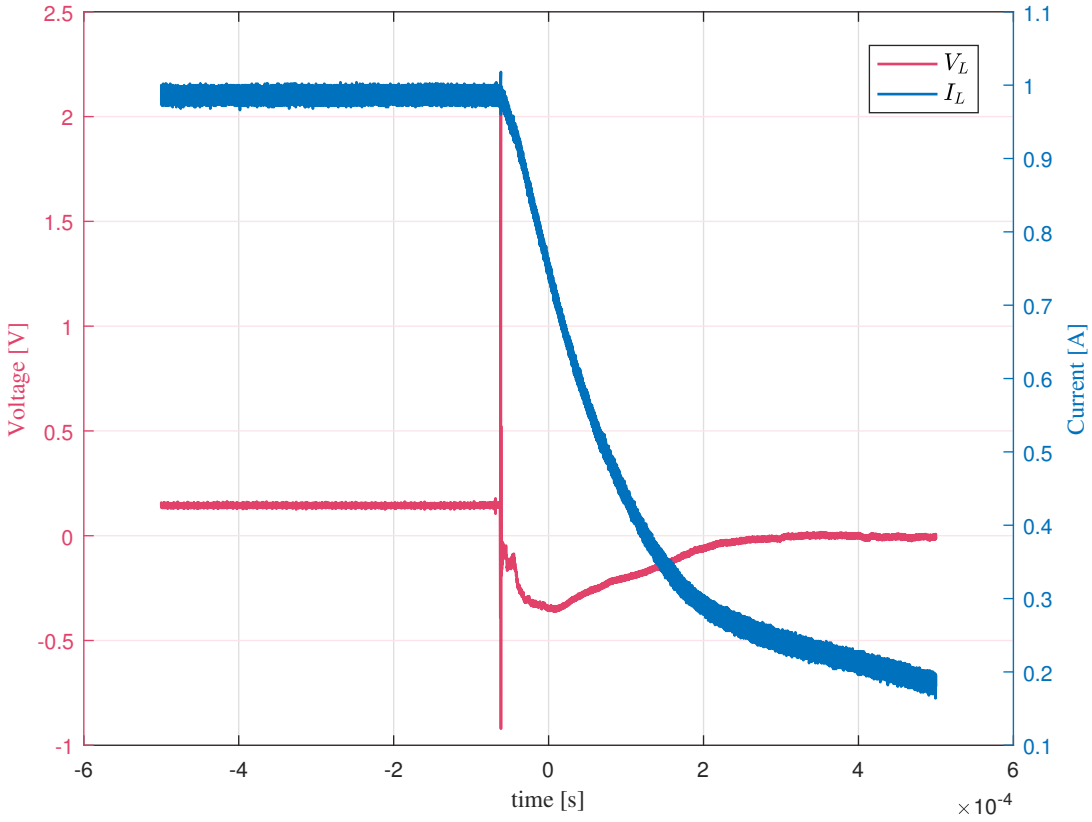


Figure 3-18: Inductor current and voltage signals obtained during the test performed to get the inductance value.

Capacitor selection

As well as in the case of the inductor, for the capacitor selection there were many options in the laboratory. The most important fact to consider in this process and with the given conditions, was the maximum voltage and current that the device was capable to withstand.

The available capacitors were able to withstand perfectly the maximum applicable voltage at the DC-link of 300 V. So, next step was to check in the datasheets the maximum current levels (around 5 A to provide enough margin in this application). Finally, a capacitor of 470 μF was selected for the buck converter output.

3.2.4 Dead-Time Generation

One of the most important considerations when generating the PWM signals to command to the gate drivers of the power transistors of a determined converter is the the required time delay applied in the switching signals to avoid a short circuit in the DC-link [18]. This causes a dead-time effect, which can produce an important error since, although it is individually small, the voltage errors are enough to distort the applied PWM signal when accumulated over an operating cycle [25], so it has to be considered in certain applications.

In the case of the synchronous buck converter, the control system must guarantee that the switches never conduct simultaneously (shoot-through) to avoid short-circuit and reduction of efficiency [32]. This is achieved by using a dead-time in each change of state, providing a new state on which both switches are turned-off. Notice that shoot-through is defined as the condition when both MOSFETs are either fully or partially turned on, providing a path for current to "shoot through" from the input voltage to GND [22]. As commented in previous chapters, GaN transistors do not have body-diode, so in this situation, when none of the devices conduct, the 2DEG of the HEMT is able to operate in the third quadrant and exhibits like a diode with $V_F = V_{th} + V_{GS_{Off}}$, where V_{th} is the required threshold voltage and $V_{GS_{Off}}$ is the applied gate voltage. Because of this effect, it is recommended to reduce the dead-time and use smaller or avoid negative V_{GS} if possible to minimize power losses [49]. Particularly, reverse conduction in HEMTs lead to a significantly higher conduction loss compared to Si MOSFET body diode conduction [28]. The solution to address this issue can also be to use a parallel diode or applying a good dead-time tuning.

In Figure 3.19, a representation of the complementary gating signals is depicted. As it can be seen, a dead-time is added to these commands. This function can be programmed in the TexasInstruments DSP for the practical implementation. In this way, one transistor will be allowed to turn-off completely before the other is turned-on.

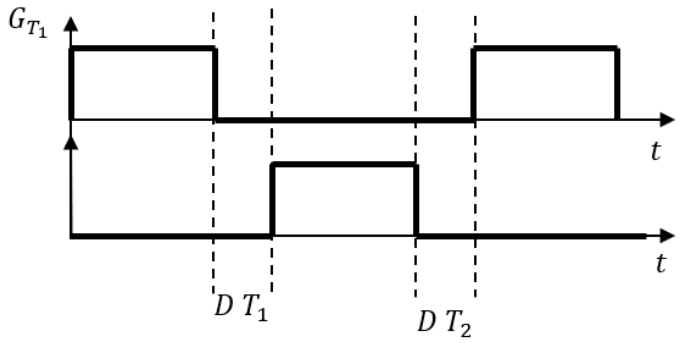


Figure 3-19: Deadtimes DT_1 and DT_2 are inserted between the gating signals.

Notice that, in case of the used GaN HEMTs, the following features must be considered [49]:

- Gate turn-on/off delay difference varies with R_G.
- The dead time must be set $> 30\,ns$ as minimum for the drivers used.
- However in practical circuit safety margin must be considered, typical $50-100ns$ is chosen for dead time.

3.2.5 Simulation Implementation of the Synchronous Buck Converter

As in the case of the DPTs, a real simulation model for the synchronous buck converter was created with the purpose of being able to perform a comparison with respect to the experimental analyses. In this section, the simulation model created in the program *PSIM* ® (Version 11.1.3) for this converter topology will be explained.

Again, the model will be constituted by the power GaN HEMTs that simulate the real behaviour of the devices (or as close as possible to reality, provided by GaN Systems). In order to explain properly the procedure followed to create the buck converter model, this section will be split in different parts.

Gate Drive Modelling

One of the challenges present in the modelling of the converter is the simulation of the gate drive. In this case, it was aimed at first to model all the parts included in the gate drivers' schematics of the experimental kit, with the purpose of reproduce the gate drivers signals as close as possible to reality. But it was not possible to carry out this idea due to the lack of information from part of the manufacturers of some components, as it was the case of the isolated DC-DC power supplies, or the high/low isolated gate drivers Si8271GB-IS (used to provide $+6/-3\,V$ to power the gate drivers). Therefore, a simplification had to be considered.

In the following figure, a representation of the used GaN HEMTs gate drives for the synchronous buck converter model simulation are shown:

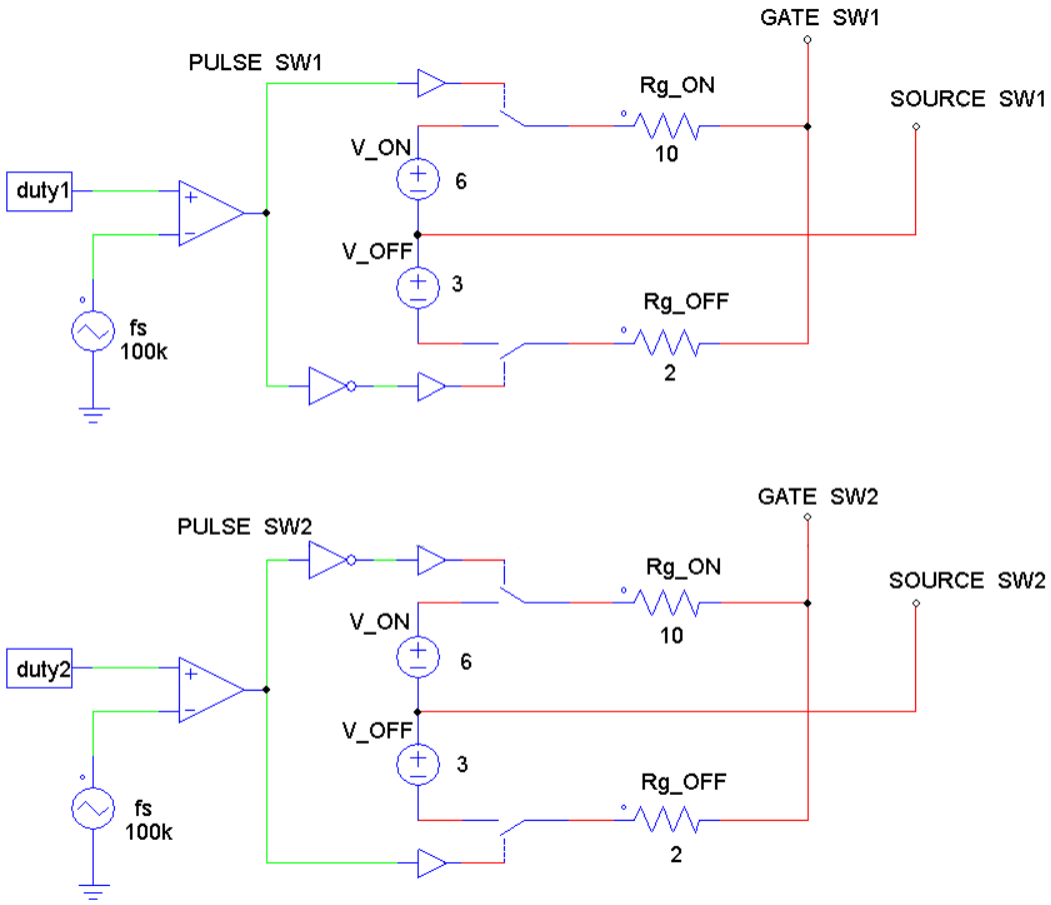


Figure 3-20: Gate drive circuit used to create the gate drive signals to control the buck converter.

As it can be observed, a non-common signal generation model to drive the power devices has been used. This is because, in contrast to the case of driving ideal transistors (which not require a negative voltage to switch-off), these devices have been driven by using a negative gate voltage to switch-off, as it is implemented in the gate drivers evaluation experimental kit. As it can be appreciated in the picture, a constant signal is compared with a triangular carrier. The constant signal defines the duty cycle, which has been varied in a determined range to evaluate different situations, and the triangular carrier imposes the switching frequency, which in this analyses has been set to: $f_s = 100\,kHz$.

Then, the resultant pulses are transmitted to two ideal switches (one of them negated) to form the system that allows to create the $+6/-3\,V$. This is possible thanks to the voltage sources connected in the same point to the source terminal of the GaN HEMT. After them, two resistors are included to control the switching speed and slew rate. The modelling of this part has been performed following the recommendations specified in the GaN Systems document for driving GaN HEMTs [48] and [49].

Especial care must be considered in the generation of the pulses when using dead-times (remember that a synchronous buck converter has been modelled). In Figure 3.21, the gate signals are represented. A saw tooth modulation has been used, as well as a phase delay for the two different power transistors. In Figure 3.20, it can be appreciated that the negated signals are just the opposite for the ideal switches that allows to generate the gate drive pulses for the GaN HEMTs. Let's focus on the upper signal of the comparator output (the other is just the opposite). As it can be appreciated in the first plot, the signals are overlapped. The larger pulse will command the $-3\,V$ (turn-off switch 1) to one switch, and the other will command the $+6\,V$ (turn-on switch 2) to the other switch. In this way, it is ensured that a dead-time is generated. The only thing to take into account, is to calculate properly the phase delays and the constant comparators to generate correctly the pulses with the desired durations. For this project, this has bee performed in a Matlab file, in

such a way that all the required parameters were automatically calculated for the evaluated duty cycles.

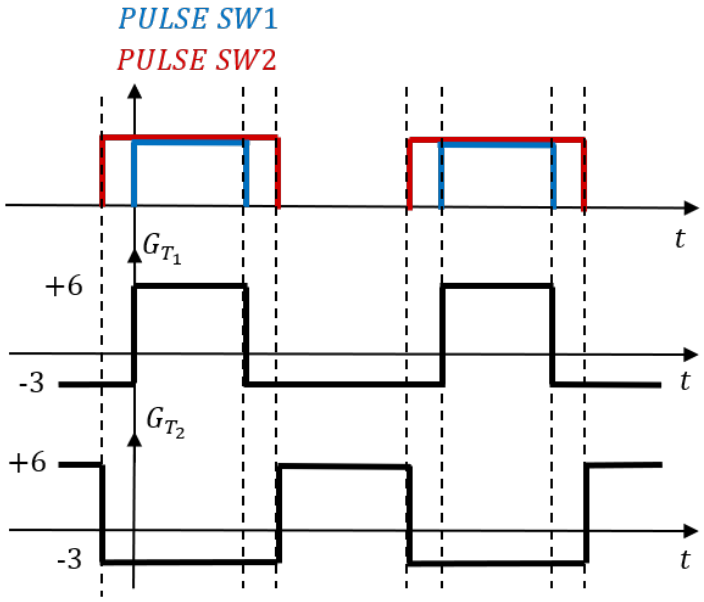


Figure 3-21: Gate drive signals used to control the synchronous-buck converter.

Power Circuit Modelling

Once the gate drive signals are properly created, the modelling of the power circuit for the synchronous buck converter can be done. In order to achieve an approximate-to-reality model, the documents [47] and [49] provided by the manufacturer GaN Systems has been used.

Additional inductors have been included in the model to reproduce a closer behaviour of the power circuit to the reality. With respect of the components, the following data has been used:

- DC Input Voltage Source: $V_{in} = 50$–$300\,V$ (in steps of $50\,V$)
- Inductor: $L = 1\,mH$
- Capacitor: $L = 470\,\mu F$
- Load: $R = 24\Omega$

3.2.6 Experimental Implementation of the Synchronous Buck Converter

As well as in the case of the experimental implementation of the double pulse test, several setbacks appeared as we tried to move forward in the analyses. These issues, delayed the work and it was not possible to implement all the studies that were plan to carry out for this project. In this section, the procedure followed to perform the experimental analyses with the synchronous buck converter will be explained.

Experimental Analyses Procedure

As commented previously, several designs for this converter topology were done to study different operating conditions. The components explained in Section 3.2.3 were employed for the test. In order to build the circuit at first, some cables with suitable "monster tips bananas" were used. With this fast assembly, it was possible to perform a first study of the converter working at $V_{in} = 50\,V$ and small duty cycle (which implies low current). But it was noticed that, the section employed could be not large enough for the experiments on which greater currents were going to be present. For this reason, the initial mounting was modified, and more robust cables were employed together with the appropriated connectors. To prepare this new assembly, the cables were cut particularly for this design and the terminals were pressed at the cable ends by means of particular long-nosed pliers. Then, the terminals were attached to the electrical components by using screws, nuts and washers.

Unfortunately, a new problem arose: it was observed that, due to the high switching frequency used ($f_s = 100\,kHz$) and the high slew rate (dV/dt), the switching pulses commanded to the experimental kit from the DSP were not reliable enough to carry out test at higher voltages due to the presence of a large ripple in the pulses. This was noticed for an input voltage of $V_{in} = 50\,V$, by observing the pulses at the gate drive circuits of the experimental kit, the inductor current and the load current. To solve this issue and improve the test assembly, several measures were taken:

- To reduce as much as possible the cables length of the power circuit to avoid

extra inductance effects in this part. Some components were attached directly at a single node (without any cable) by means of a screw and a nut, as it was the case of the inductor and capacitor.

- To reduce again the length of the control signal cables from the DSP to the experimental kit, in order to reduce undesired effects caused from the extra inductance created by these thin cables.

- To increase the dead-times to ensure enough time for the switches to turn-off before the other is turned-on.

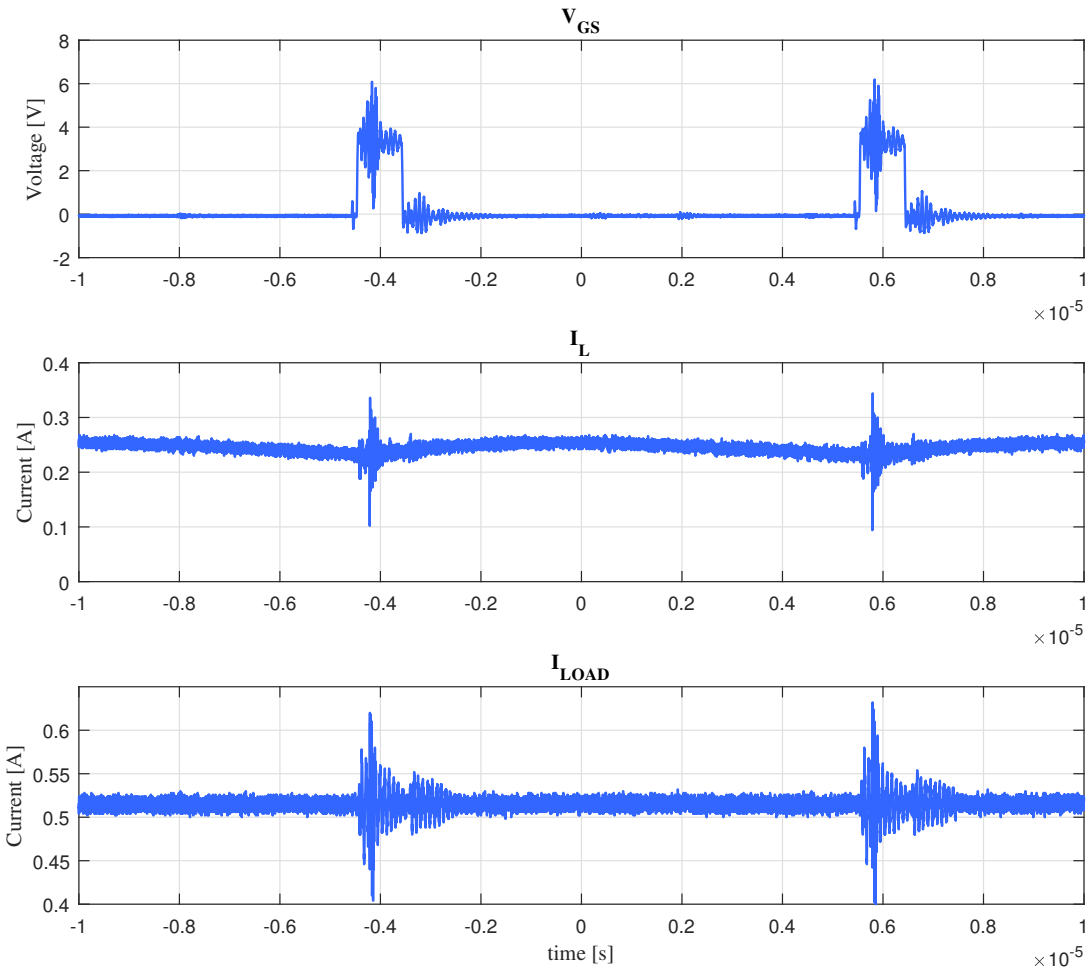


Figure 3-22: Wrong waveforms observed during buck tests.

In Figure 3.22, a representation of the waveforms obtained in this conditions with the oscilloscope is shown.

After implementing these modifications, an improvement in the pulse signals commanded to the gate drivers for the GaN HEMTs was observed. In the following figure, a picture of the mounting prepared in the laboratory to perform the analyses is included:

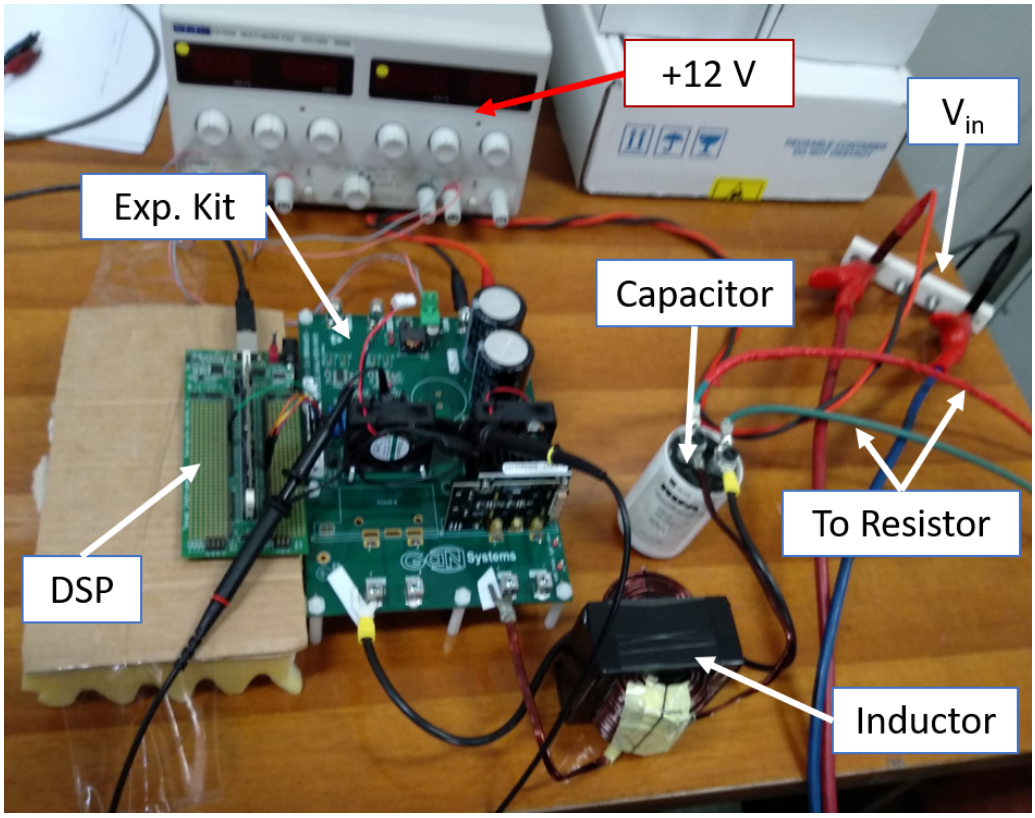


Figure 3-23: Physical assembly used for the buck converter.

Therefore, it was possible to continue with the experimental test for the synchronous buck converter. The analyses at $V_{in} = 50\,V$ and $V_{in} = 75\,V$ for different duty cycles were carried out. However, when $V_{in} = 100\,V$ was reached, another problem appeared. In this case, the issue was actually in the computer: as the voltage level was increased (and keeping the switching frequency and of course, the intrinsic slew rate of the GaN HEMTs), the ElectroMagnetic Interference (EMI) produced by the system was transmitted to the laptop (possibly by radiation and conduction). This

phenomenon caused the PC to switch-off suddenly, loosing the control of the power converter. Notice that, as well as in the case of the double pulse test, the computer was used to control the converter, enabling and enabling the signals, modifying the value of the duty cycle, etc. So, these operating conditions were not reliable at all to proceed with the experiments, since a short-circuit could be produced anytime, compromising the integrity of the power transistors and other components of the system, besides the fact that it was not possible to proceed with the analyses since the PC was necessary to increase the duty cycle. Notice that, the DSP was also directly connected to the laptop to power it up by means of a USB cable.

At this point, the most suitable solutions were:

- Employ optical fiber to transmit the pulse signals from the DSP to the HEMTs gate drive circuits in a most reliable medium.
- Use a filter between the DSP and computer.
- Use a filter between the DSP and experimental kit.
- Program the flash memory of the DSP (avoiding the use of the PC) and using peripherals to control the converter.

Since the first three options were not possible because the required material was not available at the laboratory, the last option was selected. Notice that the used DSP experimental kit did not include any peripheral suitable to control the converter, so a set of switches and cables connected to the GPIOs were welded to create control input signals. With the new assembly, a new electrical path was created due to the switches incorporated in the DSP experimental kit. This effect leads to a new problem: the warm-up of the microcontroller. Unfortunately, this phenomenon was not observed at first, so the DSP was seriously damaged. After replacing it by a new one, and repeating all the process with the welding of the switches and the flash programming, it was noticed a raise in the chip temperature when investigating a possible failure (the DSP was performing properly the programmed tasks, checked

with the oscilloscope). At this point, the system was not reliable at all to continue with the experiments, since the DSP could be damaged again.

Unfortunately, due to the different setbacks that were appearing during the experiments, and the time required to solve all of them with the means and material available in the laboratory, these were all the test performed, although more analyses were planed to be carried out at the beginning of the project.

Programming of the DSP

In order to control the synchronous buck converter functionalities, a DSP was programmed. The same device than in the case of the DPTs was used for this purpose: the *TMS320F28335* and the *C2000 DIMM100 Experimenter's Kit*. The software used to create the code was again *Code Composer Studio* (Version 5.5), programmed in C language. In this section, a brief explanation of the final version of the program used to control de converter with the DSP will be made. Notice that several programs and different modifications to improve the reliability of the code were made until reach the final version.

As it was commented in the previous section, in the final version of the assembly the flash memory of the microcontroller was used since it was not possible to control the converter with the laptop due to EMI problems. Hence, two switches were attached to the DSP experimental platform to perform the control of the converter. These components were in charge of:

- First switch: This component is the responsible to transmit the signal that is commanded to the converter to enable and disable the transmission of the pulses to the gate drivers of the GaN HEMTs. Therefore, two positions are required: with a 0 the PWM pulses are disable, so the transistors are turned-off continuously; with a 1 the PWM signals are enabled, so the pulses are transmitted to the gate drivers and hence to the GaN devices.

- Second switch: This element is used to modify the value of the duty-cycle in steps of 0.1. Two positions are needed for that purpose, in such a way that

every time the switch commands a high state (1) to the DSP, the value of the duty-cycle is increased.

Notice that, a high-state (1) is commanded to the DSP when the switch connects the corresponding GPIO with the $3.3\,V$ terminal, and a low-state (0) is transmitted when the switch connects the GPIO with the GND pin. For that, the used GPIOs must be configured in the DSP as "input", such that they are reading the values that are being commanded at the clock frequency. Another consideration that must be applied, is to disable the pull-up resistances that internally the microcontroller has enabled. In this way, the normal state of the GPIOs configured as inputs will be a low-state.

The program has been structured in such a way that, it has a main file and other functions created in other files that can be called and used in the main file. These functions are:

- Configure and initialize the GPIOs: inside this function, all the used GPIOs are configured as it is required and initialized. Particularly, they are configured as ePWM for the signals that will carry the pulses to drive the GaN HEMTs, inputs for the pins that are connected to the switches and outputs for the pins that commands control signals to the experimental kit (converter). The latest are required since, an enable/disable command is required for the gate drivers, and to command low-states to the pins not used of the experimental kit, commented in Section 3.1.3, just for reliability issues.

- Configuration and initialization of the ePWM: in this function, the pulses that need to be commanded to the buck converter to drive the GaN devices are programmed. Symmetrical triangular carriers have been used, and a continuous comparator to create the pulses, in such a way that when the constant comparator signal is greater than the triangular carrier a high-state is produced ($3.3\,V$), and when is smaller a low-state is generated ($0\,V$). Notice that two commands are needed (one for each switch), so another signals has been programmed in complementary mode. This means that this signal will generate the pulses in

the opposite way than in the first case. As commented in Section 3.2.5, dead-times are required to avoid short-circuit. For this reason, dead-times have been configured at the rising and falling edges of the pulses of both signals to achieve an equally share of the dead-times.

Notice that other functions already created by TexasInstruments are used, to initialize the system for example. In the following figure, a diagram of the program structure implemented to control the synchronous buck converter is included:

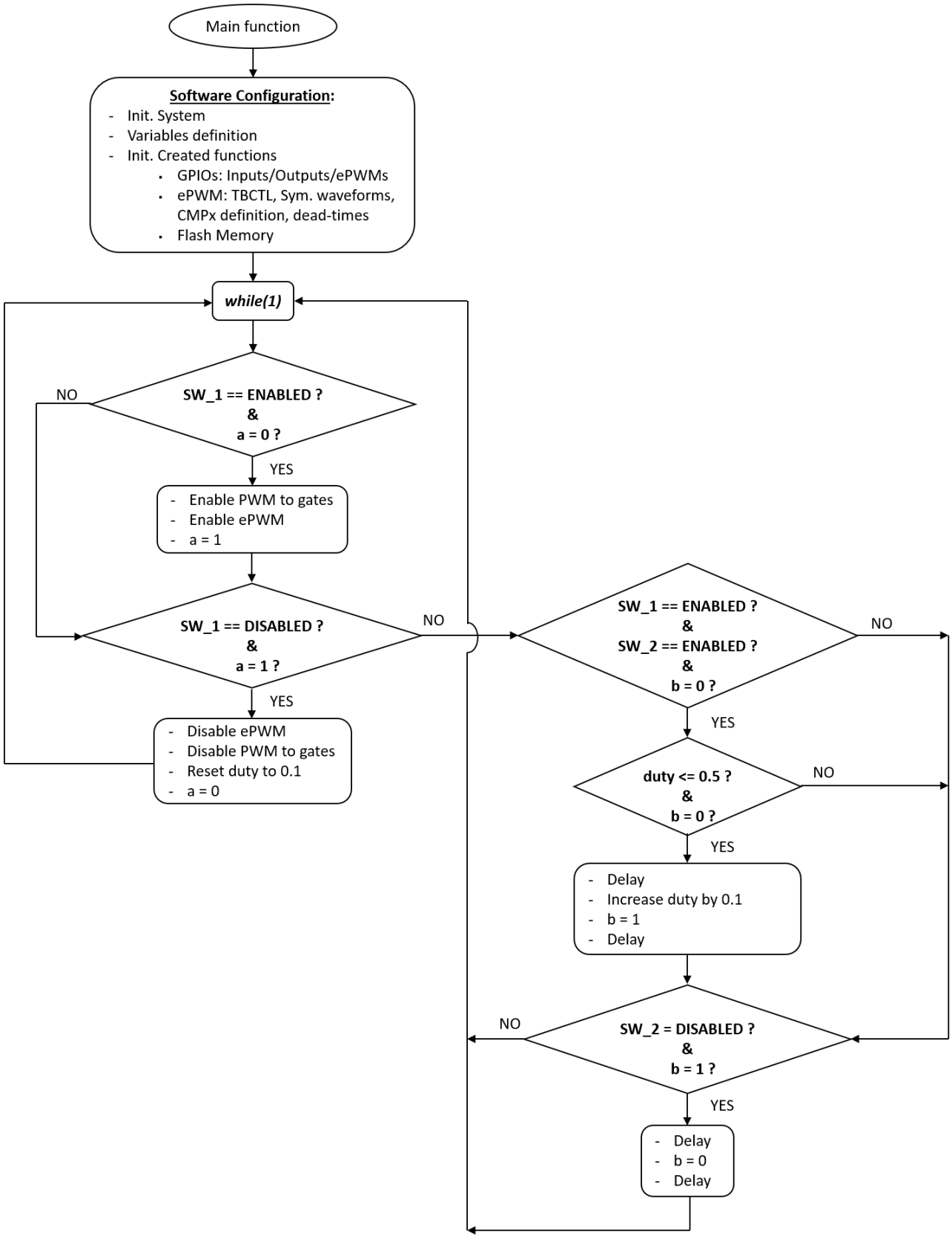


Figure 3-24: Flow chart of the program created to generate the pulses for the buck test.

Explanation of variables a and b:

- Variable a: this variable is used to avoid activating continuously the PWM signals. In this way, if the user changes the position of the switch to enable the PWM signals (first switch) and keep the switch in that position, the activation of the PWM signals is produced just once. Initially is set at 0.

- Variable b: this variable is used to increase the duty-cycle each time the second switch is commutated to the position that increases the duty-cycle by 0.1. In this way, if the switch is kept in the same position, the duty does not increase continuously.

Now that all the important features have been explained, the program structure can be explained. First of all is to initialize the system and to call the function which enables the flash memory programming. Then, the GPIOs are initialized, but not the ePWM function. If this function would initialize in this stage, it will directly activate the pulses. To avoid that, the ePWM function is called inside a condition included in an infinite loop. To enter in such condition, the user must activate first switch, that is, enable the PWM signals. Before, the ePWM pins were commanded at a low-state to avoid undesired switching. To increase the duty-cycle, another condition included inside the infinite loop was created, related with the second switch. In this way, if the user activates such switch, the condition was fulfilled and the duty cycle will be increased by 0.1. Notice that of course the duty-cycle needs to be limited to the maximum value.

If the user needs to turn-off the pulses rapidly, the first switch can be moved again to disable the PWM signals. In this way, the PWM pins are commanded to the power devices a low-state to turn them off.

Chapter 4

Experimental and Simulation Results

In this chapter, the obtained simulation and experimental results will be exposed, comparing the differences observed between both.

In the first section, the experimental and simulation results of the studies carried out for the double-pulse test will be shown, and in the second part, the experimental and simulation synchronous-buck converter tests results will be exposed.

The analyses performed for both tests are based in the observation of the drain-to-source voltage (V_{DS}), since it was not possible to measure the drain current (I_{DS}) in the experimental tests due to the fact that no drain current measure points were included in the finally used experimental kit board. However, with the drain-to-source voltage it is possible to obtain large information, such as: a comparison of the transient response between simulation and experiments, the overshoot peak voltage, the dV/dt, rise time, fall time, the oscillation frequencies, etc. This information will be analysed in the following sections, for the turn-on and turn-off events and for different voltage and current levels.

4.1 Double-Pulse Test

In this section, the double-pulse test analyses carried out experimentally and in simulations will be shown. The analysed voltages for these tests were: $V_{in} = 50V, 100V$, $150V$, $200V$, $250V, 250V$. The analysed currents for each voltage level were: $I = 5A, 10A, 15A, 20A, 25A, 30A$. As it can be observed, a wide variety of operating points of the GaN HEMTs will be studied.

In the following figure, a representation of the drain-to-source voltage and inductor current obtained for the DPTs performed experimentally and in simulation for $V_{in} = 50V$ and $I = 5A$ is shown:

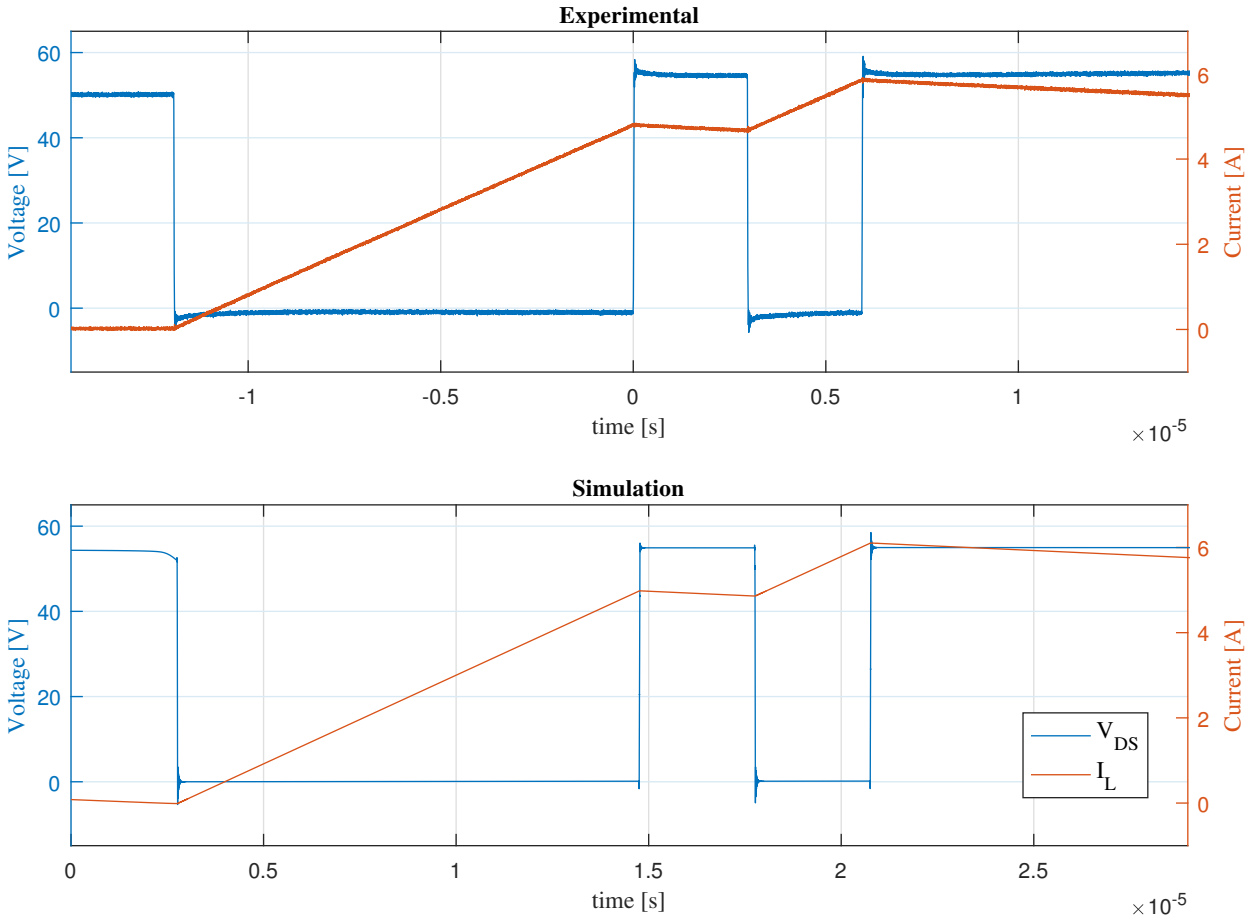


Figure 4-1: Drain-to-source voltage and inductor current observed in the DPT for $V_{in} = 50V$ and $I = 5A$.

In the figure below, an example of a DPT is exposed. As it can be observed, when the first pulse is produced (see Figure 3.2), the GaN transistor is closed, the V_{DS} drops to ~ 0 and the current through the inductor starts increasing. The turn-off event can be observed at the end of this interval. In the break, the voltage V_{DS} raises to $\sim 50V$ again and the current decreases slightly through the coil. The turn-on transient can be analysed at the end of this interval. Then, the second pulse is produced, followed by a break. Notice that the turn-off can be observed as well at the end of this interval if the current level reached is similar.

4.1.1 Transient Analyses for the DPTs

In this subsection, the transient response appearance of the DPTs will be analysed for the turn-on and turn-off events of the GaN transistor, making a comparison between experimental and simulation results. Notice that, in this studies, not all the voltage and current levels will be analysed, since too much figures will be necessary, and this analysis can be performed by choosing some voltage levels and intermediate current values, particularly $I = 5A, 15A, 30A$.

In Figure 4.2, the turn-off events at $V_{in} = 50V$ are shown. As it can be observed, for $I = 5A$, the transient overshoot is more significant in the case of the experimental test, practically not affecting the simulation response. In case of $I = 15A$, it can be seen that the overshoot behaviour is similar in terms of duration, observing some differences in the shape of the wave. For $I = 30A$ the differences between bot models are more pronounced, since the waveform is quite different. It can be appreciated how the ringing oscillations varies with the current level in both cases, increasing the wave amplitudes with higher current values.

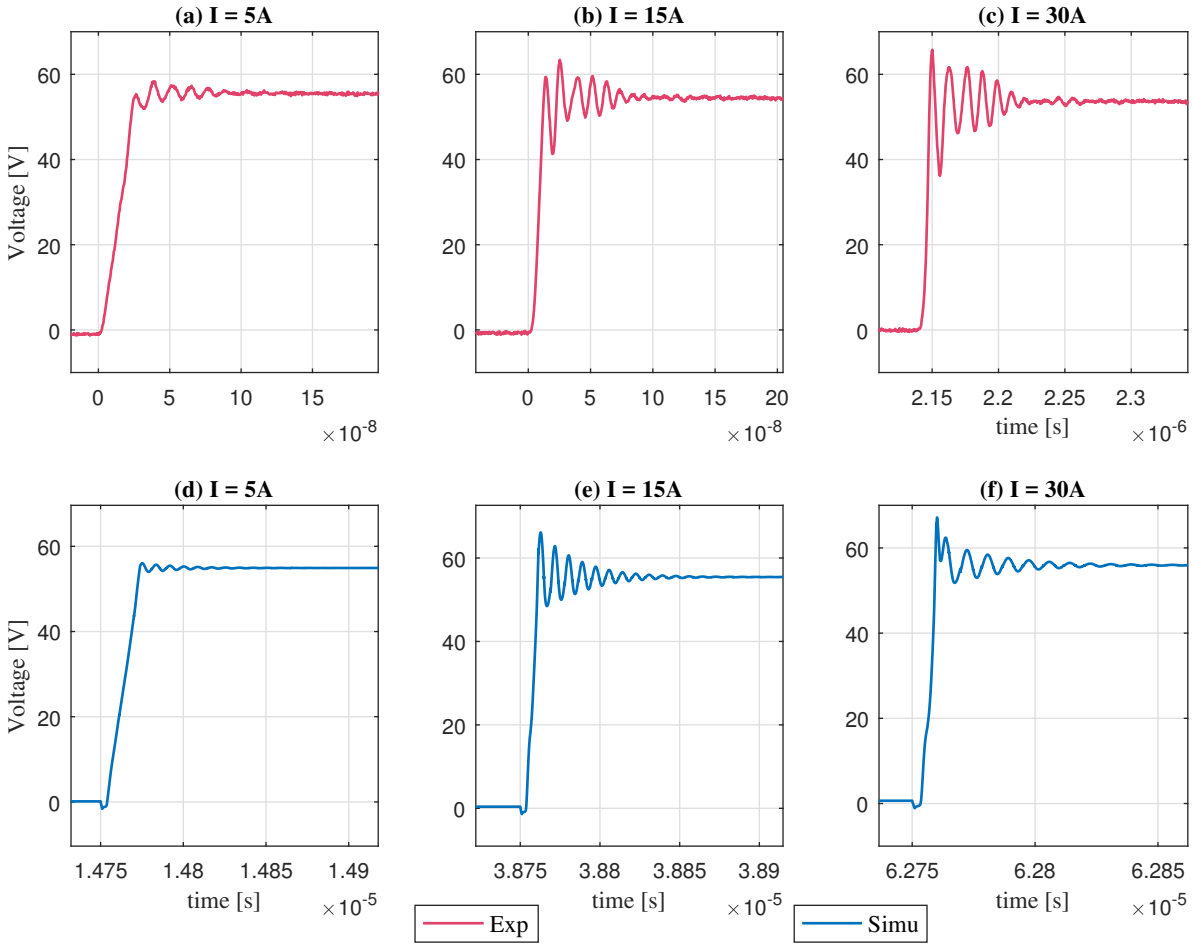


Figure 4-2: Drain-to-source (V_{DS}) voltage transients produced at the turn-off for different current levels at $V_{in} = 50V$: (a) Experimental at $5A$; (b) Experimental at $15A$;(c) Experimental at $30A$;(d) Simulation at $5A$;(e) Simulation at $15A$;(f) Simulation at $30A$.

In Figure 4.3, the turn-off events produced at $V_{in} = 200V$ are shown. In the first case ($I = 5A$), it can be determined that in the simulation response, practically no effect of overshoot is observed with respect to the experimental response. In the second and third cases ($15A$ and $30A$), the overshoots produced in the simulation test are closer to the reality produced in the experimental tests. However, there are some differences observed in the wave shapes. The ringing amplitude increases with the current as well.

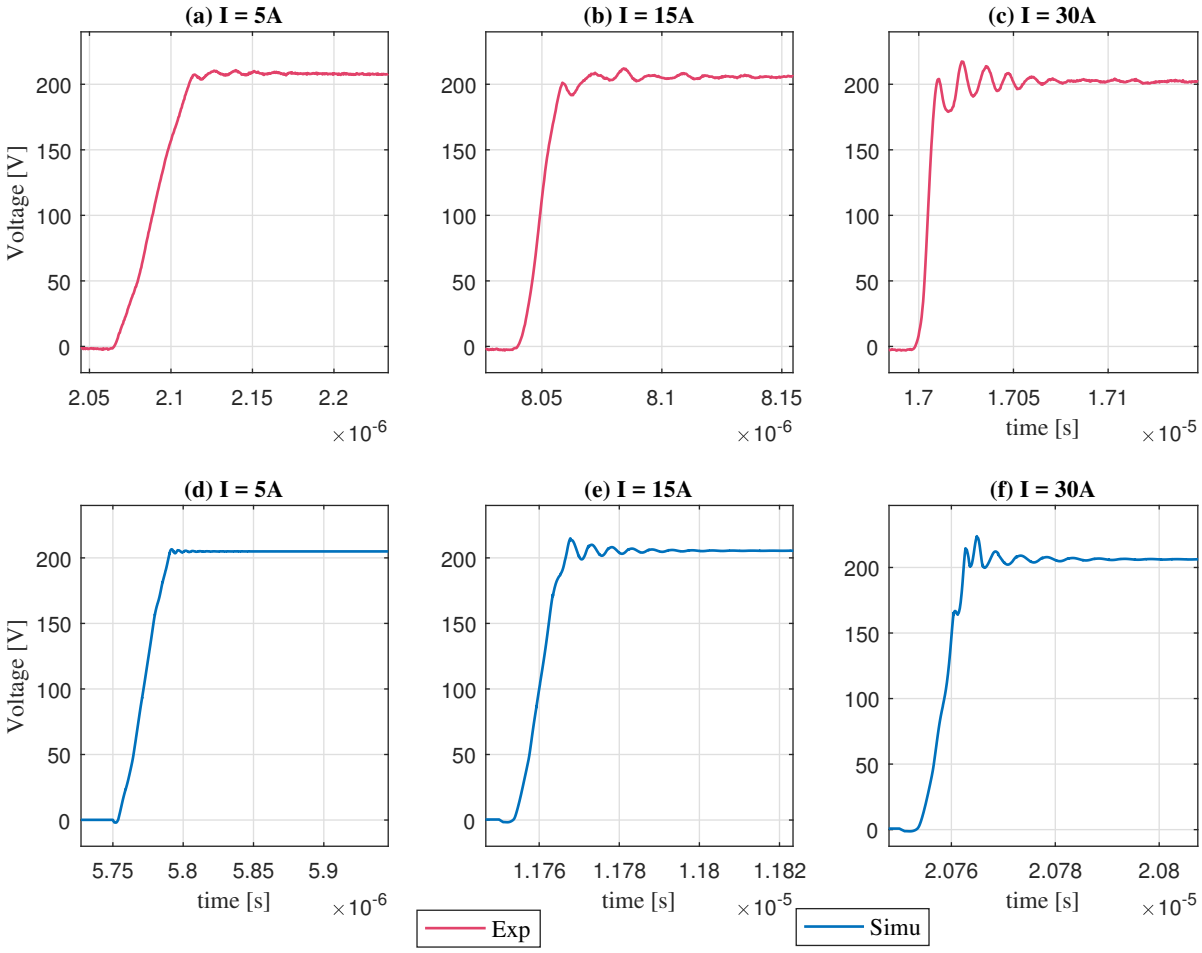


Figure 4-3: Drain-to-source (V_{DS}) voltage transients produced at the turn-off for different current levels at $V_{in} = 200V$: (a) Experimental at $5A$; (b) Experimental at $15A$;(c) Experimental at $30A$;(d) Simulation at $5A$;(e) Simulation at $15A$;(f) Simulation at $30A$.

The turn-off events in the DPTs are represented in Figure 4.4 for $V_{in} = 300V$. As it can be observed, for a current level of $5A$, the overshoot produced in both cases is reduced significantly with respect to previous voltage levels. A slight reduction of the overshoot is observed as well for $15A$ and $30A$, observing similar wave shapes than in the case of $V_{in} = 200V$, but with reduced voltage amplitude in percentage of the analysed voltage level. It can be concluded therefore, that the transient performance is better for larger voltage values. This will be studied later in the peak voltages produced.

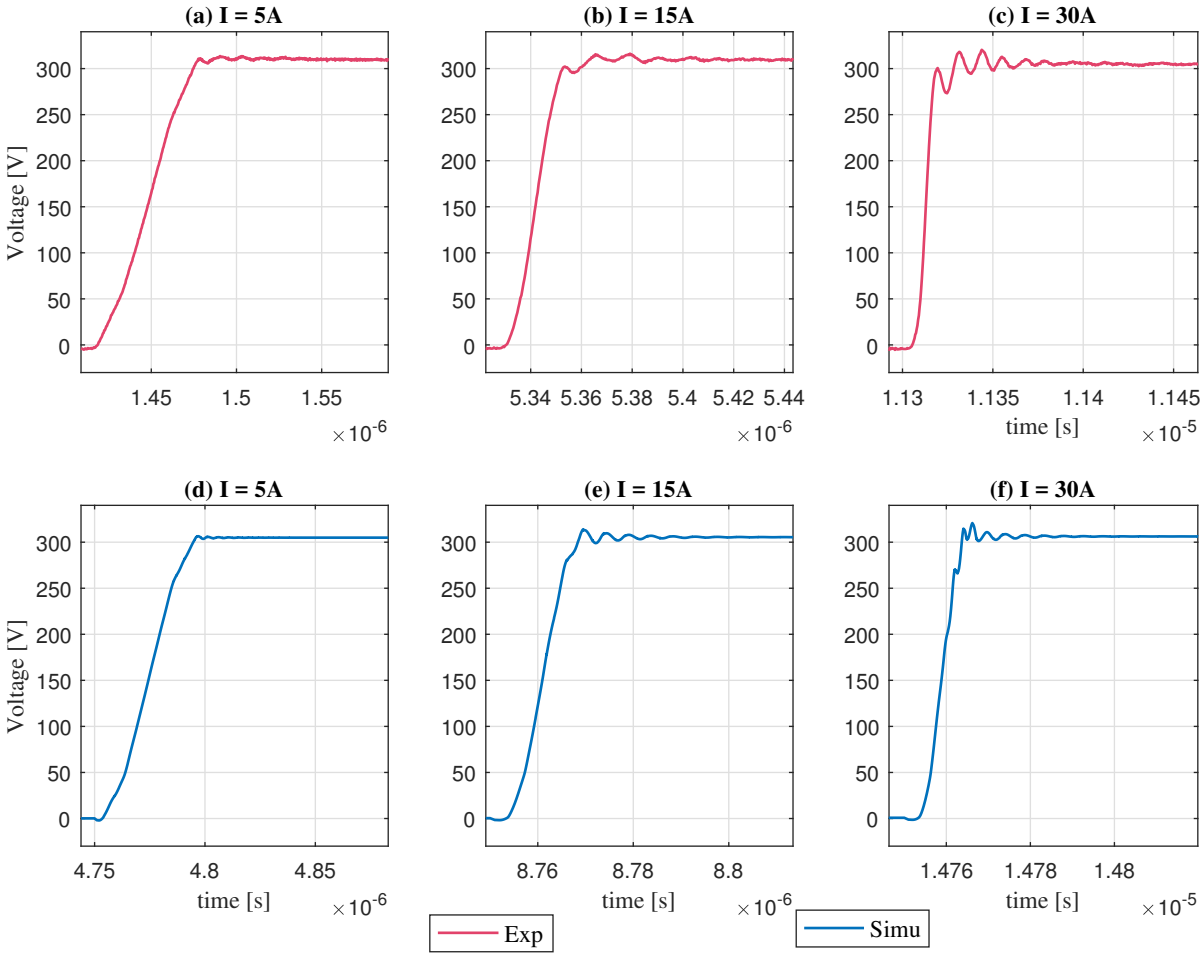


Figure 4-4: Drain-to-source (V_{DS}) voltage transients produced at the turn-off for different current levels at $V_{in} = 300V$: (a) Experimental at $5A$; (b) Experimental at $15A$;(c) Experimental at $30A$;(d) Simulation at $5A$;(e) Simulation at $15A$;(f) Simulation at $30A$.

In Figure 4.5, the turn-on transients for $V_{in} = 50V$ are represented. As it can be observed, the transient responses obtained in the simulations are closer to the expected waveforms obtained in the experimental results than in the turn-off events. However, it can be observed a V_{DS} dip in different locations when comparing the simulation and experimental results. That voltage dips are produced due to the loop inductance ($\Delta V = L_p \cdot di/dt$), so it can be determined that the simulated loop inductance can be better adjusted to the reality. It can also be commented that the overshoot duration is slightly larger in the experimental response than in the simulation analyses. However, if comparing these results on which SMD GaN HEMTs have been used, with "TO-X" packages, the overshoot is significantly reduced.

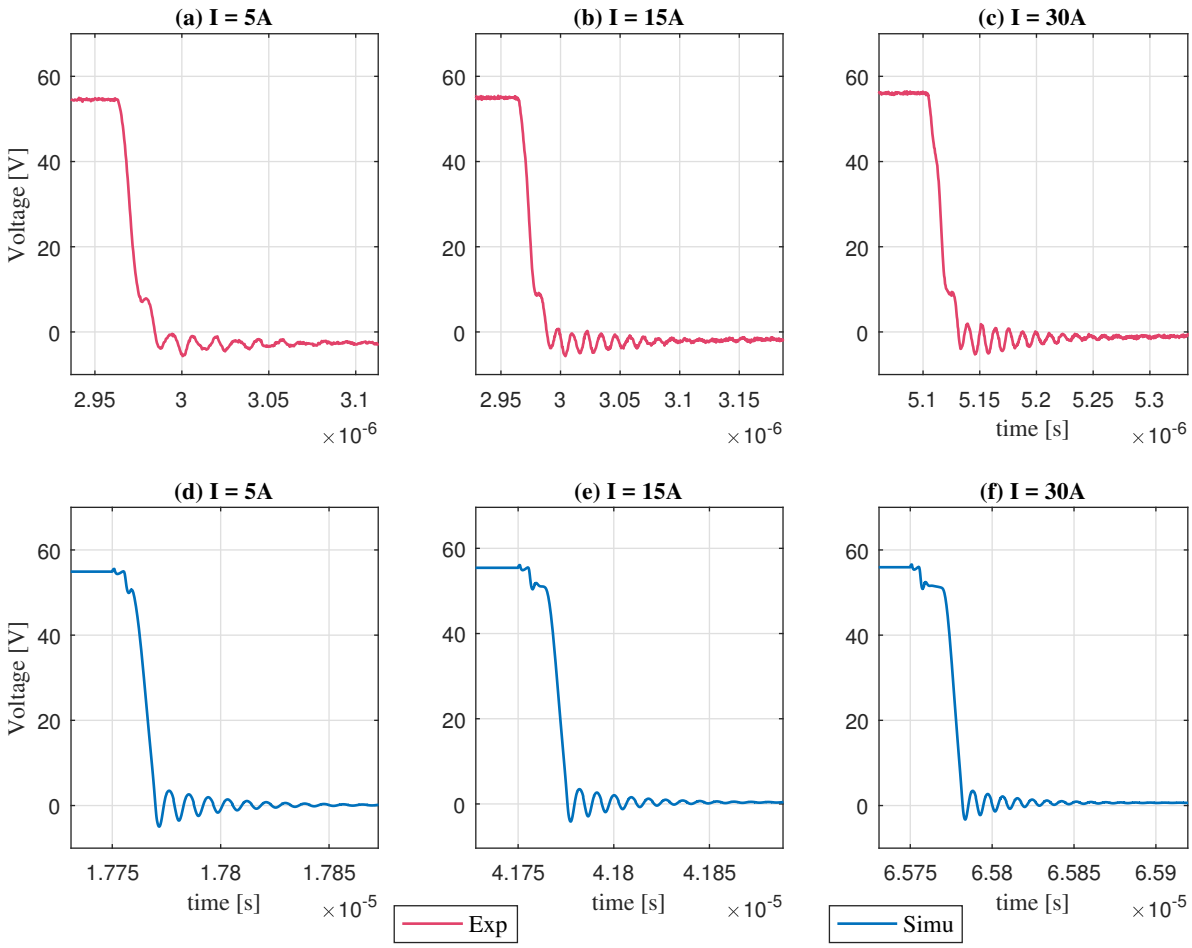


Figure 4-5: Drain-to-source (V_{DS}) voltage transients produced at the turn-on for different current levels at $V_{in} = 50V$: (a) Experimental at $5A$; (b) Experimental at $15A$;(c) Experimental at $30A$;(d) Simulation at $5A$;(e) Simulation at $15A$;(f) Simulation at $30A$.

In Figure 4.6, the same transient analysis is shown, but now for $V_{in} = 200V$. As it can be observed, a ringing oscillation occurs in the simulation results just before turning-on the GaN transistor. This phenomenon is not present in the case of the experimental results, and might be produced due to the effect of the loop inductance. The transient overshoot duration observed in the experimental results is reduced when compared with the previous case of $50V$. However, the match between simulation and experiments was better in the previous case, since practically no overshoot is produced in the simulation results in contrast with the experiments. It can be also appreciated that the overshoot produced in the experiments is not too much dependant on the current value.

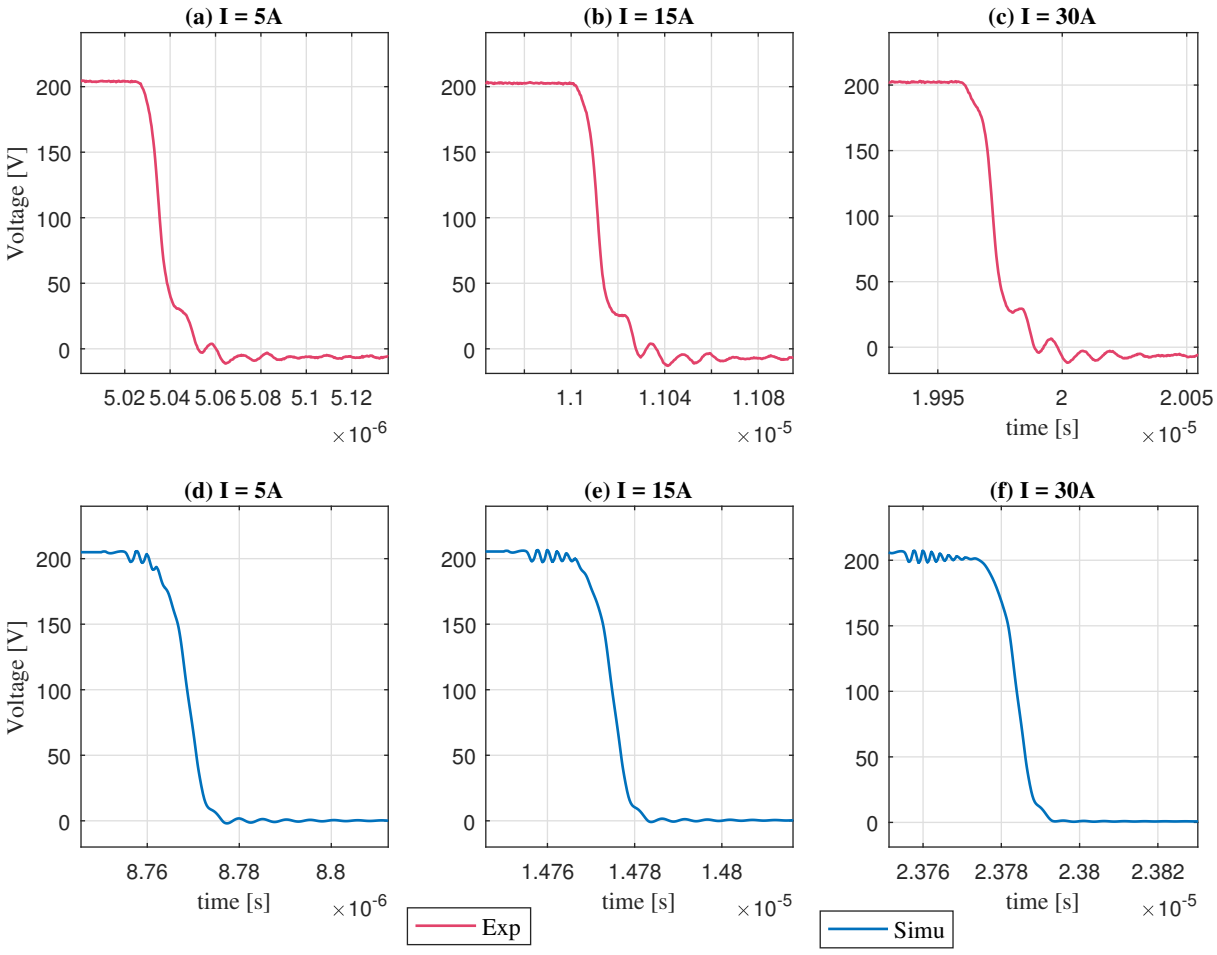


Figure 4-6: Drain-to-source (V_{DS}) voltage transients produced at the turn-on for different current levels at $V_{in} = 200V$: (a) Experimental at $5A$; (b) Experimental at $15A$;(c) Experimental at $30A$;(d) Simulation at $5A$;(e) Simulation at $15A$;(f) Simulation at $30A$.

Finally, the case of $V_{in} = 300V$ is exposed in Figure 4.7. As it can be seen, similar comments than in the previous case ($200V$) can be done: the ringing in the simulation response appears again, and the overshoot in the experiments is reduced again. With the information collected in these analyses, it can be concluded that the transient response varies considerably with the input voltage level. Similarly, the match between the simulation and experimental transients depends on the voltage level.

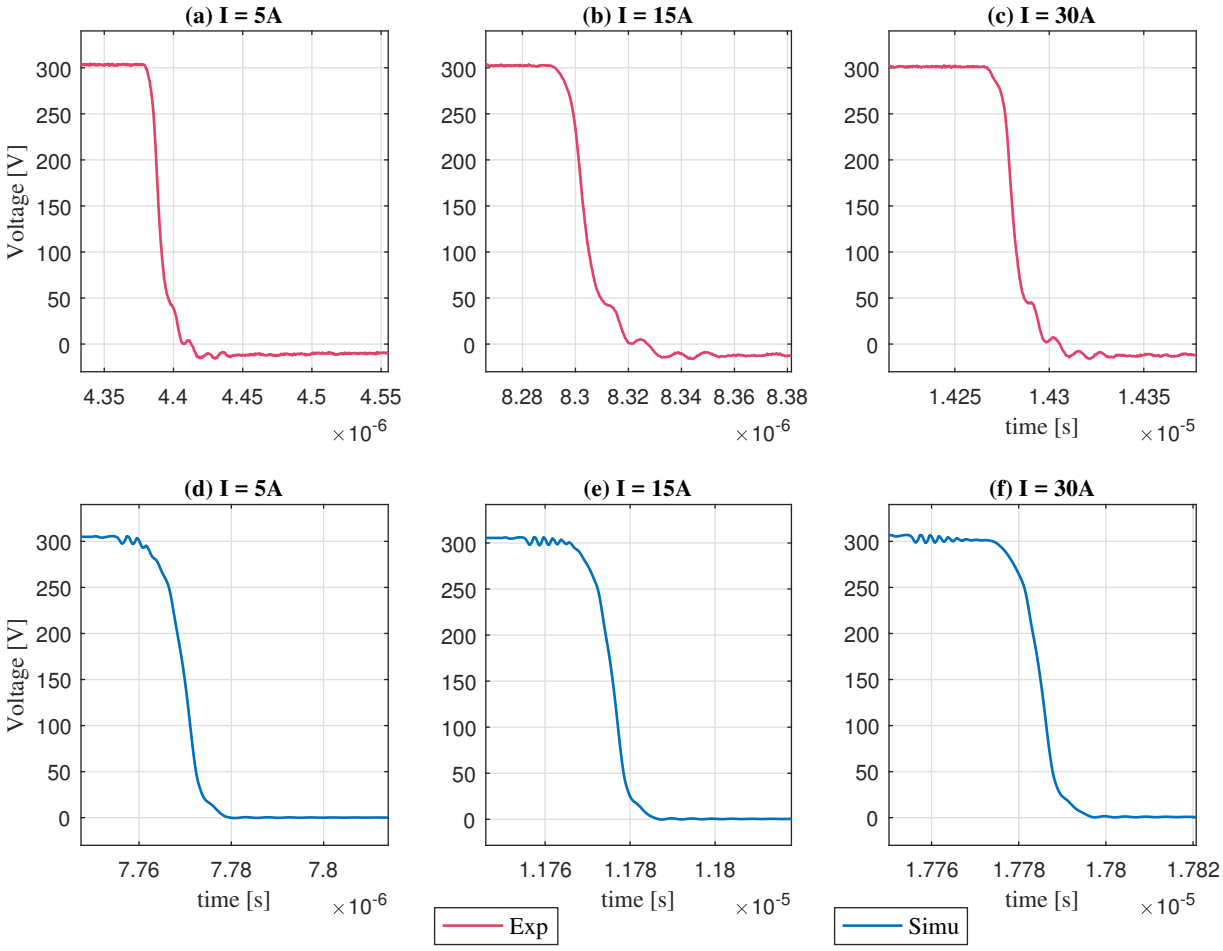


Figure 4-7: Drain-to-source (V_{DS}) voltage transients produced at the turn-on for different current levels at $V_{in} = 300V$: (a) Experimental at $5A$; (b) Experimental at $15A$;(c) Experimental at $30A$;(d) Simulation at $5A$;(e) Simulation at $15A$;(f) Simulation at $30A$.

4.1.2 Peak voltages produced at the turn-off and turn-on events

In this subsection, the peak voltages of V_{DS} reached in the transient response and produced in the turn-on and turn-off events will be evaluated for different voltages and current levels.

In Figure 4.8, the peak voltages produced at the turn-off transients are shown for different voltages and currents. Notice that the voltages have been exposed in percentage in the figure in order to be able to compare the results obtained when the DPT is performed with different voltages. As it can be observed, the larger peak voltages (in percentage of the applied test voltage) are produced for the lower voltage levels, as it is the case of (a) and (b). In the first case, the lager peak is produced in the simulation for a current level of $20A$, and almost reaches the 25% of the test voltage. However, in the experiments, the larger peak voltage is produced for a current level of $30A$ and its value is around 20% of the test voltage. As the figures show, the peak voltages are reduced while increasing the voltage level, and increase with the test current generally (at least in the experimental tests). It can be also checked that the peak voltage variations for the same test voltage and different current values are much more significant for lower test voltages. The lowest peak voltages variations for different currents and the same test voltage are produced for cases (e) and (f). Therefore, it can be concluded that the best performances are achieved for the larger test voltages, and for reduced currents, in accordance with the results previously seen in the transient response analyses (Section 4.1.1).

On the other hand, it can be appreciated that, in some cases, significant differences are produced between the simulation and experimental tests. However, it cannot be observed a relation with the test voltages and currents. For each case the coincidences are different.

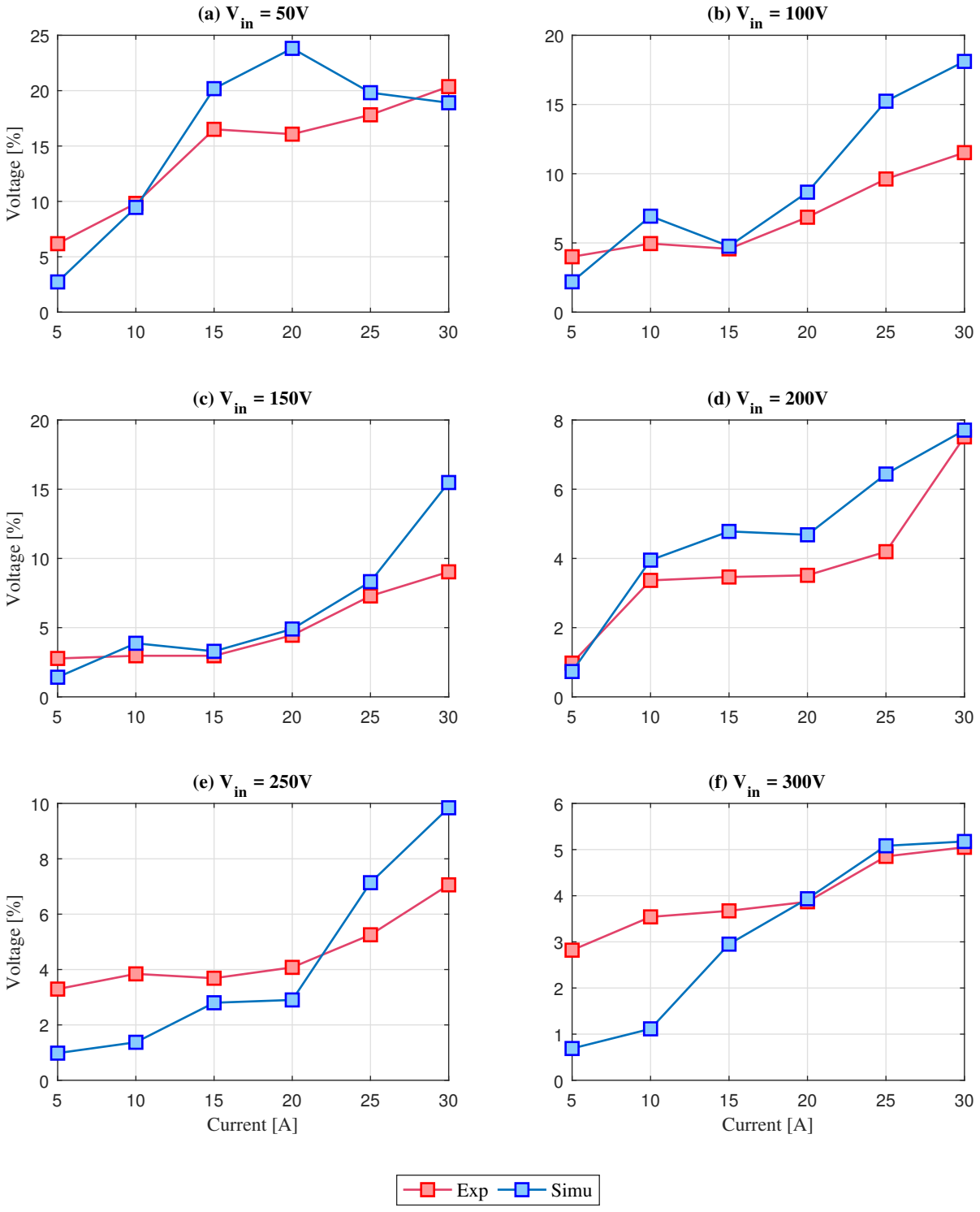


Figure 4-8: Drain-to-source (V_{DS}) peak voltages produced at the turn-off overshoot for different current levels and different test voltages: (a) $V_{in} = 50V$; (b) $V_{in} = 50V$;(c) $V_{in} = 50V$;(d) $V_{in} = 50V$;(e) $V_{in} = 50V$;(f) $V_{in} = 50V$.

In figure 4.9, the peak voltages produced at the turn-on events for different currents and voltages are shown. Notice that in this case, the voltages presented in percentages are expressed with negative values, since the overshoot produced here is below 0. As it can be observed, significant differences are produced between the simulation and experimental results. This can be also verified by observing Figures 4.5, 4.6 and 4.7, where practically no overshot is produced in the simulation turn-on events. However, in case (a), some overshoot is produced. Therefore, it can be concluded that the turn-on transients does not properly match the experimental results.

In the case of the experimental results, the peak voltages produced are reduced while increasing the voltage levels, as in the case of the turn-off. However, it can be appreciated that the peak voltage values are much lower in amplitude than in the case of the turn-off. This fact is produced due to the higher resistance value employed in the gate drive for the turn-on event, used to control the dV/dt slew rate (switching speed), to avoid large overshoots and reduced commutation losses (see Figure 3.20, where it can be seen how two different resistors are used for the turn-on and turn-off). In this tests, it can be observed how this design works properly. It can be also checked that, the current dependency of the peak voltages practically does not exist for the same test voltage, especially for the tests from $150V$.

The highest peak voltage (in percentage of the test voltage) is reached at $V_{in} = 50V$ and for a current level of $10A$. The lowest values are produced for $300V$. Therefore, it can be concluded that the bests performances are obtained are higher voltages, independently on the current in general.

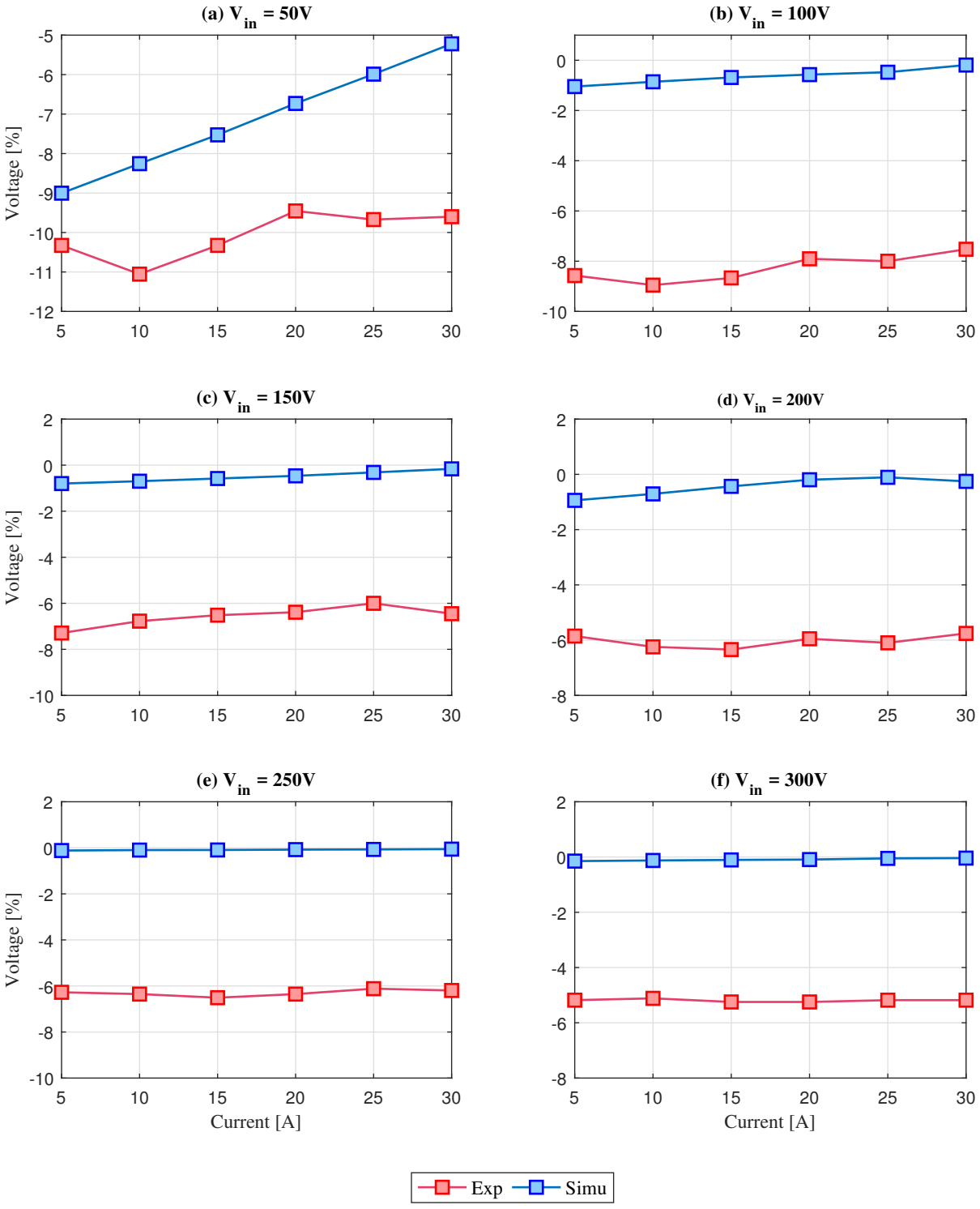


Figure 4-9: Drain-to-source (V_{DS}) peak voltages produced at the turn-on overshoot for different current levels and different test voltages: (a) $V_{in} = 50V$; (b) $V_{in} = 50V$;(c) $V_{in} = 50V$;(d) $V_{in} = 50V$;(e) $V_{in} = 50V$;(f) $V_{in} = 50V$.

4.1.3 dV/dt produced at the turn-off and turn-on events

In this subsection, the rate of variation of the voltage with respect to time (dV/dt) will be analysed at the turn-off and turn-on events for different voltage levels and currents.

In Figure 4.10, the results obtained for the turn-off events are exposed. As it can be observed, the simulation and experimental results show similar behaviours, since the values obtained in both cases are very similar. It can be also appreciated that the voltage derivative increases with the test voltage and also, for the same test voltage, the dV/dt increases with current. This is because the voltage rise time is reduced with current. In fact, the largest dV/dt are produced at large current levels for the highest test voltages, that is: at $30A$ for $250V$ and $300V$. It is observed that the dV/dt variations between $5A$ and $30A$ are more pronounced at large test voltages. In general, high dV/dt are produced, and the expected results match with the experimental analyses.

In Figure 4.11, the results of the turn-on events are exposed. As it can be observed, the rates of variation of the voltage with respect to time are larger in the case of the simulations for all the voltage and current levels. The closest relation is achieved for voltage levels of $100V$ and $150V$. However, such relation is quite large in other cases, such as case (f), where the reality is not well reflected in the simulations.

In all the cases, it can be observed that the dV/dt increases with the test voltage, and decreases with the test current. This phenomenon is observed in both, the experimental and simulation results, and is produced due to the increase of voltage fall time with drain current. Notice that the variations of the voltage derivative for the same voltage level and different currents are quite reduced in comparison with the previous case, similarly than in hte case of the peak voltages for the turn-on.

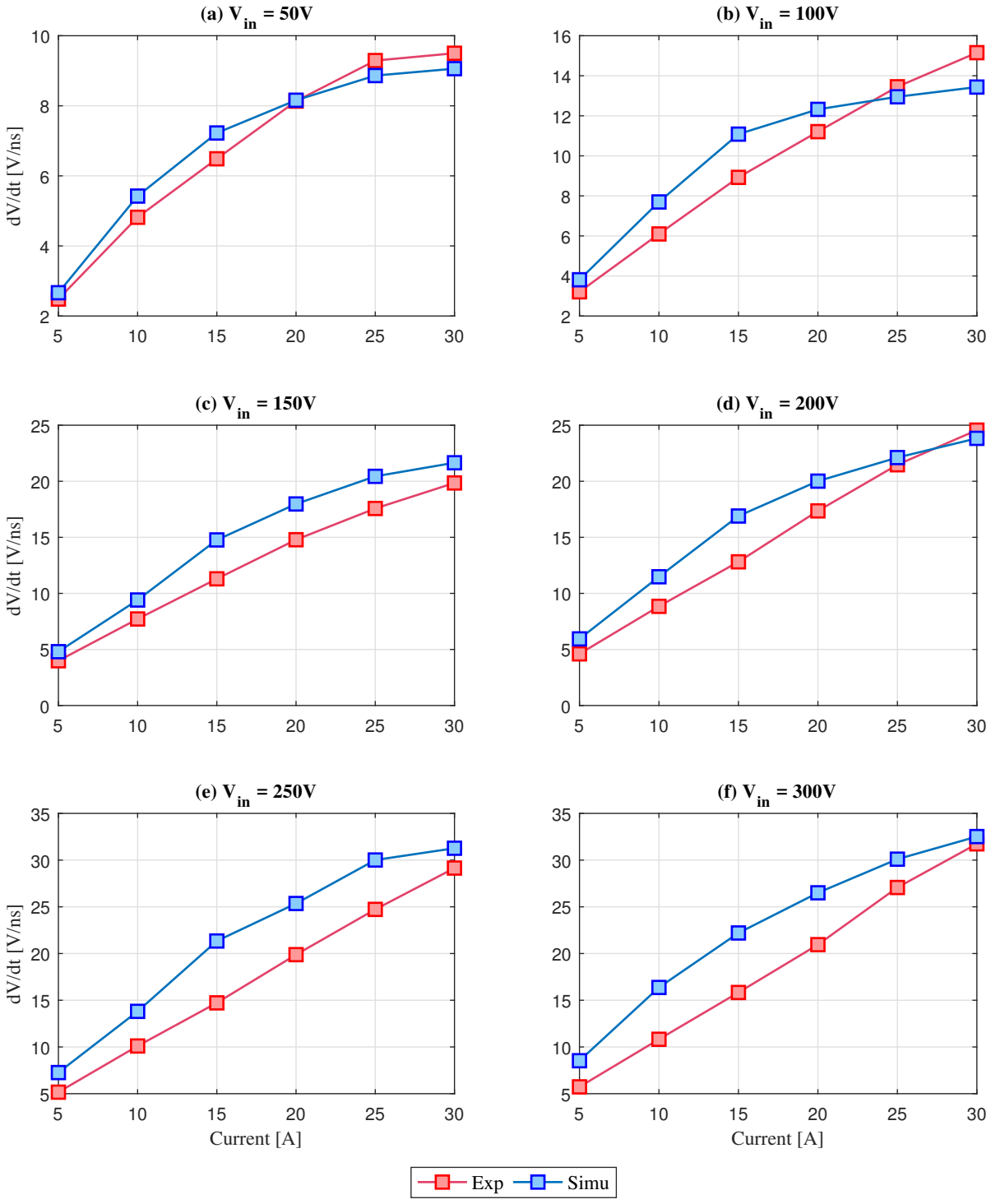


Figure 4-10: Drain-to-source (V_{DS}) dV/dt in $[V/ns]$ produced at the turn-off event for different current levels and different test voltages: (a) $V_{in} = 50V$; (b) $V_{in} = 50V$;(c) $V_{in} = 50V$;(d) $V_{in} = 50V$;(e) $V_{in} = 50V$;(f) $V_{in} = 50V$.

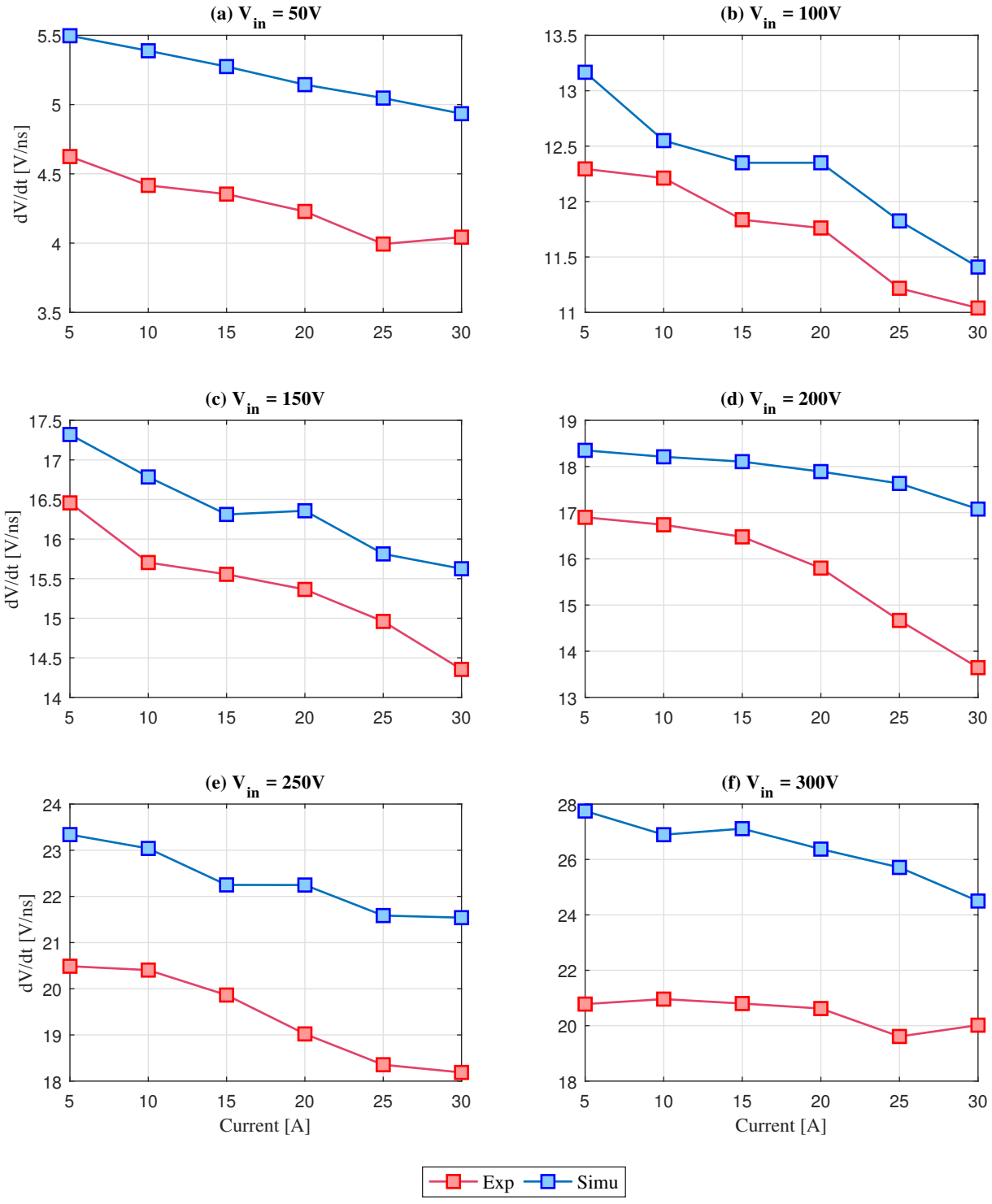


Figure 4-11: Drain-to-source (V_{DS}) dV/dt in $[V/ns]$ produced at the turn-on event for different current levels and different test voltages: (a) $V_{in} = 50V$; (b) $V_{in} = 50V$;(c) $V_{in} = 50V$;(d) $V_{in} = 50V$;(e) $V_{in} = 50V$;(f) $V_{in} = 50V$.

4.2 Synchronous Buck Converter Test

In this section, the synchronous buck converter tests will be analysed. As in the case of the DPTs, different voltage and current levels (different duty-cycles) have been tested. However, due to the problems that appeared during these tests (commented in Chapter 3), the synchronous buck converter was just analysed for $V_{in} = 50V$ and $V_{in} = 75V$.

In the following figure, an example of the data obtained in the experimental and simulation results for $V_{in} = 50V$ and duty $= 0.3$ is shown:

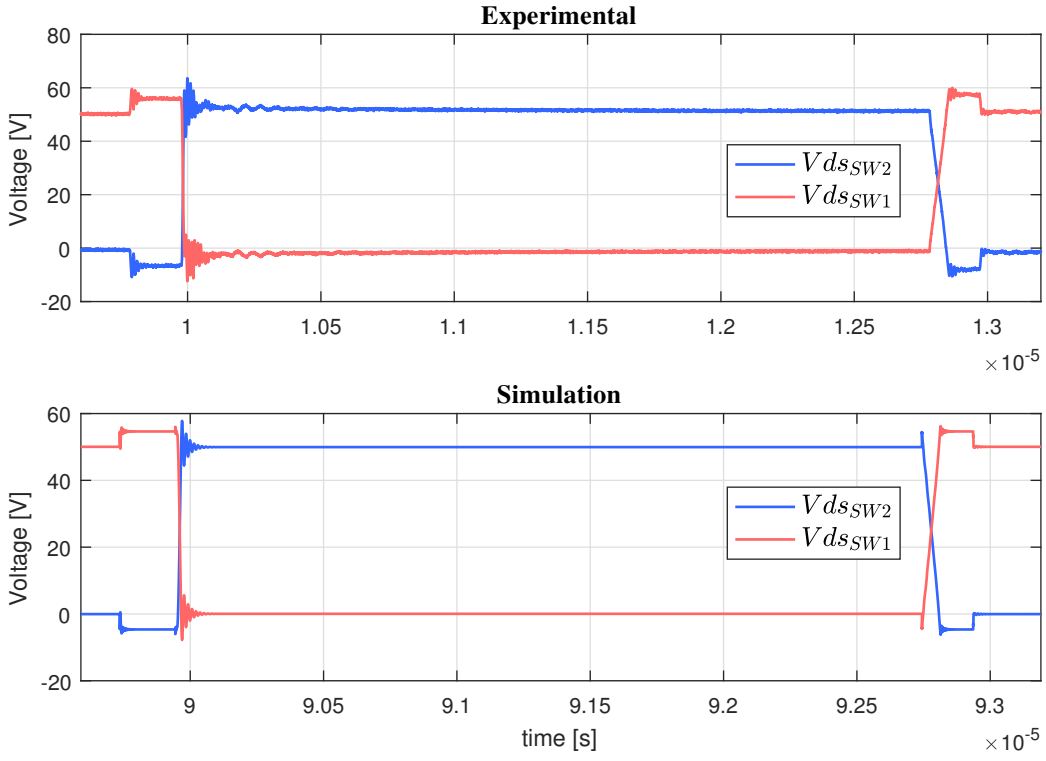


Figure 4-12: Drain-to-source (V_{DS}) voltage transients produced at the turn-on and turn-off events in the synchronous buck converter in the experimental and simulation results.

As it can be appreciated, both switches of the synchronous buck converter are

included in the experimental and simulation results. They are denoted with SW1 (first switch) and SW2 (second switch, substituting the diode of the original buck converter).

As it can be seen, just before the first commutation and just after the second commutation, the voltage value V_{DS} is modified. This phenomenon is produced due to the fact that, during the dead-times (necessary to avoid short-circuit), both power devices are turned-off simultaneously, but the energy stored in the inductor discharges through the 2DEG of the second switch until the corresponding gate-to-source signal becomes high ($V_{DS,ON} < V_{Reverse}$).

4.2.1 Transient analyses for the Synchronous Buck Converter

In this subsection, the drain-to-source voltage V_{DS} transient results obtained in the simulations and experiments will be analysed. As commented previously, two voltage levels were possible to analyse ($V_{in} = 50V$ and $V_{in} = 75V$). The duty-cycle was also varied in order to evaluate different points of operation. However, in this section just some cases will be studied to avoid redundancy.

In Figure 4.13, the turn-off transient voltages for switch 1 (SW1) are shown for an input voltage of $50V$ and different duty cycles. As it can be appreciated for duty = 0.1, the simulation does not represent properly the reality reflected in the experimental result, since practically no overshoot is produced in the simulation. In the next plots, some ringing appears. However, the oscillation frequency does not match correctly with that observed in the experiments. This phenomenon can be improved by adjusting and correcting the loop inductances used in the simulation model to match the performance observed with the used experimental kit board. In case of the experiments, it can be seen how the oscillations amplitude increases with the duty.

Another behaviour that can be observed in the simulation results is the undervoltage produced just before turning-off. This phenomenon takes place at the end of the dead-time and is caused as a consequence of the V_{GS} turn-off undershoot, which adds to the V_{SD} droop during the dead time. This is traduced into a higher dead time loss,

and can be avoided by adjusting and optimizing experimentally the turn-off resistance value (R_{off}). However, this effect is not present in the experimental results.

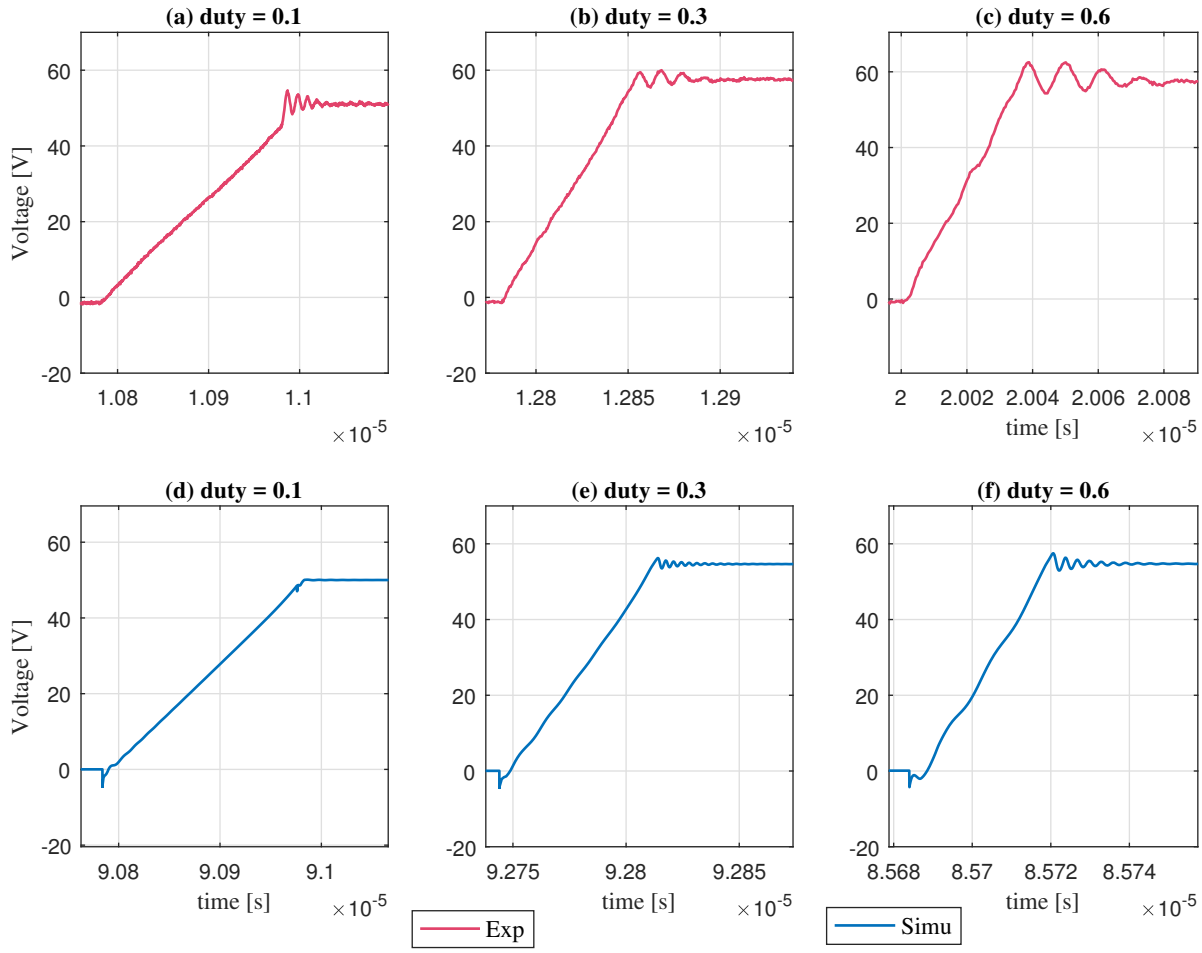


Figure 4-13: Drain-to-source (V_{DS}) voltage transients produced in SW1 at the turn-off for different duty-cycles at $V_{in} = 50V$: (a) Experimental at $duty = 0.1$; (b) Experimental at $duty = 0.3$;(c) Experimental at $duty = 0.6$;(d) Simulation at $duty = 0.1$;(e) Simulation at $duty = 0.3$;(f) Simulation at $duty = 0.6$.

In Figure 4.14, the performance of SW1 during the turn-on event for a voltage level of $50V$ and different duty-cycles have been analysed. As it can be observed, both for the simulation and experimental results, the overshoot produced does not vary significantly for the different operating points. Even so, a small increase in the overshoot can be appreciated between case (a) and cases (b) and (c). The most notable difference is produced between the wave shapes of the simulation and exper-

imental results, since the simulations does not match perfectly with the experiments. This could be improved by representing in a better way in the simulations the loop inductance circuit that has the used experimental kit.

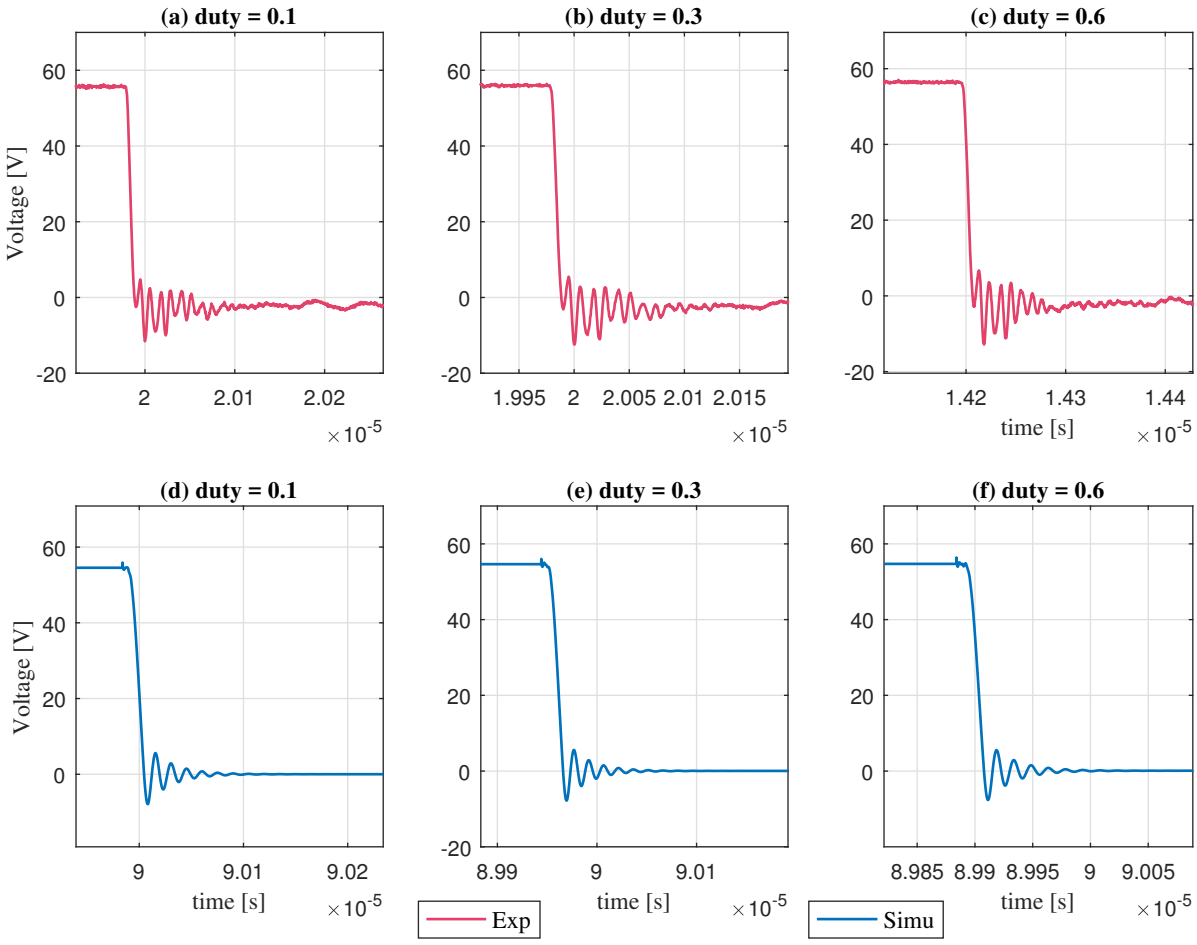


Figure 4-14: Drain-to-source (V_{DS}) voltage transients produced in SW1 at the turn-on for different duty-cycles at $V_{in} = 50V$: (a) Experimental at $duty = 0.1$; (b) Experimental at $duty = 0.3$;(c) Experimental at $duty = 0.6$;(d) Simulation at $duty = 0.1$;(e) Simulation at $duty = 0.3$;(f) Simulation at $duty = 0.6$.

Now, the same events analysed in the two previous figures will be studied but in this case for switch 2 (SW2). In Figure 4.15, the turn-off at $50V$ and different duty-cycles is shown. As it can be appreciated, the waveforms are very similar to those obtained in the turn-on event of SW1. This is because in the switches are operating in complementary mode (when one switch turns-on, the other turns-off),

so the behaviours are reflected on each other. The wave shapes of the experimental results for the different duties are similar, with some increase in the amplitudes achieved, and the simulation waves are quite invariant with each other. The simulation and experimental waveforms do not match perfectly, as commented in the previous paragraph.

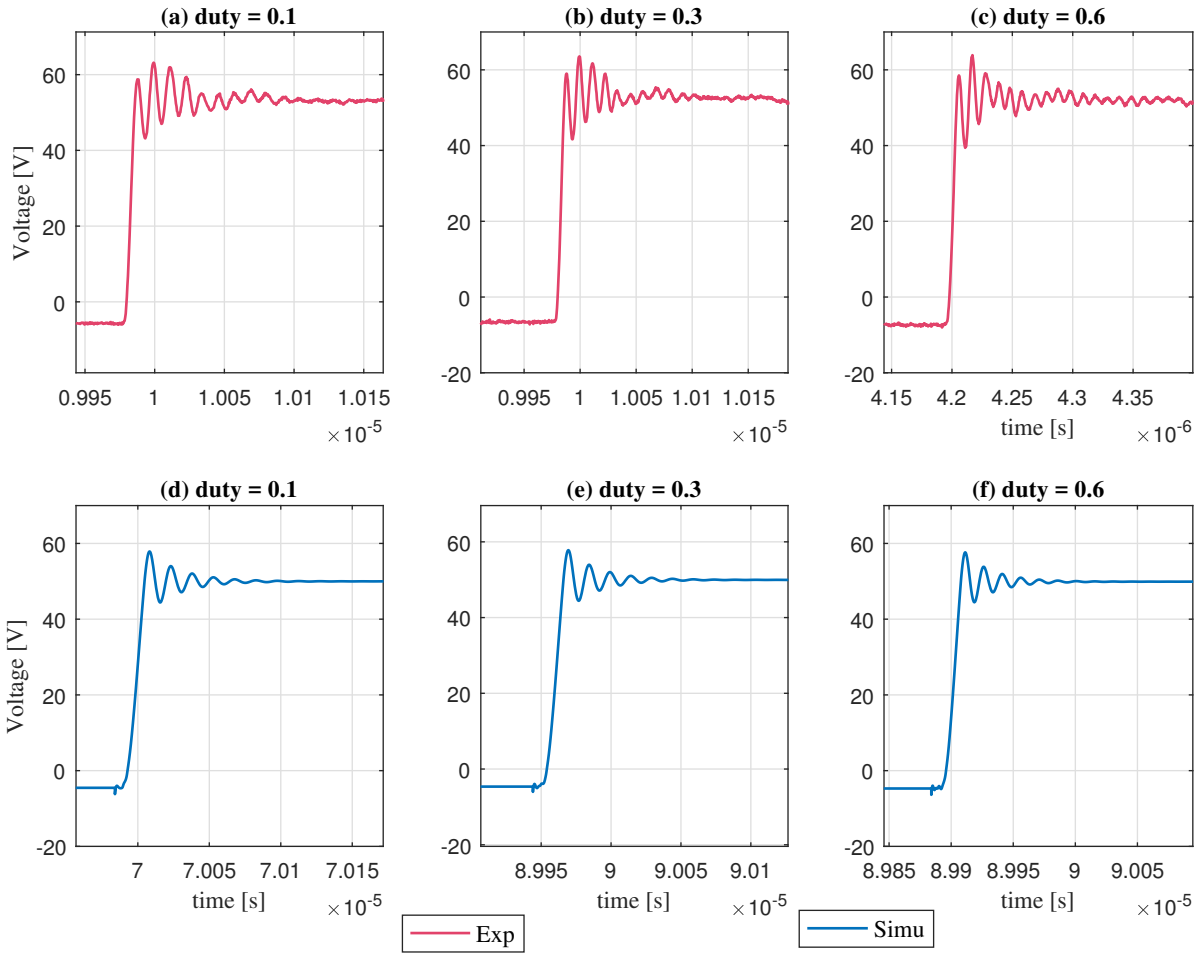


Figure 4-15: Drain-to-source (V_{DS}) voltage transients produced in SW2 at the turn-off for different duty-cycles at $V_{in} = 50V$: (a) Experimental at $duty = 0.1$; (b) Experimental at $duty = 0.3$;(c) Experimental at $duty = 0.6$;(d) Simulation at $duty = 0.1$;(e) Simulation at $duty = 0.3$;(f) Simulation at $duty = 0.6$.

In Figure 4.16, the turn-on event is exposed for the same conditions as previous analyses. As it can be appreciated, the responses are similar to those obtained in the turn-off event of SW1. It can be seen how in the simulated results the phenomenon

of the undervoltage commented is reflected, but in this case, causing a small overvoltage just after the commutation. This is to compensate such effect. Respect to the experimental waves, it can be concluded that a low overshoot is produced, much lower and shorter in duration than in the case of the turn-off. It can be also observed how the overshoot amplitude and duration increases with the duty-cycle (with the output voltage and current). The match between the simulation and experimental results must be improved to get closer to reality results.

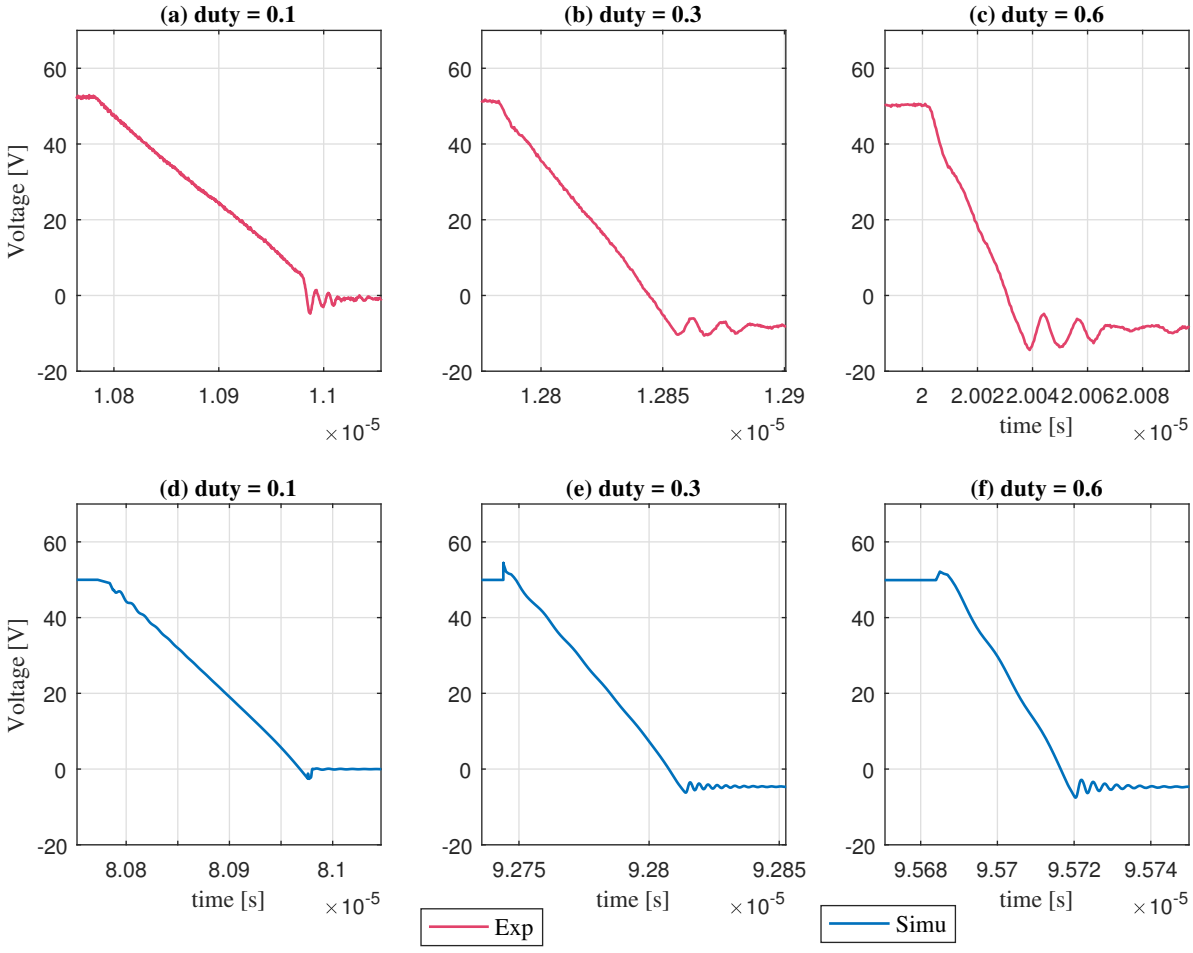


Figure 4-16: Drain-to-source (V_{DS}) voltage transients produced in SW2 at the turn-on for different duty-cycles at $V_{in} = 50V$: (a) Experimental at $duty = 0.1$; (b) Experimental at $duty = 0.3$;(c) Experimental at $duty = 0.6$;(d) Simulation at $duty = 0.1$;(e) Simulation at $duty = 0.3$;(f) Simulation at $duty = 0.6$.

4.2.2 Peak voltages produced at the turn-off and turn-on events

In this subsection, the peak voltages of the drain-to-source voltage V_{DS} produced during the synchronous buck converter tests will be commented. The turn-on and turn-off events will be evaluated in both switches (SW1 and SW2) for different voltage levels and different duty-cycle values.

As Figure 4.17 shows, in the case of the turn-on event of SW1 (both for $V_{in} = 50V$ and $Vin = 75V$) the difference produced between the simulation and experiment models is more pronounced than in the case of the turn-off event. This effect can be checked in the previously commented Figure 4.14 and 4.15. The voltage difference between both models is around $5V$ in the case of the turn-on. On the contrary, the simulation results for the turn-off events are much closer to the real obtained values in the experiments. In this case, the voltage difference between both models is around $2 - 3V$.

It can be seen how in the case of the experimental results the trend is to increase the peak voltage values when increasing the duty, while in the simulations the values are even decreasing in the case of $50V$. However, the peak voltage variation for the same test voltage and different duty is much more relevant in the case of the turn-off event than in the turn-on, where practically there is no duty dependency. The higher experimental peak voltage (in percentage of its nominal value) is reached at the turn-on at $50V$ and duty = 0.6, which does not match with the simulation results, where the highest voltage is reached at duty = 0.1 for $50V$.

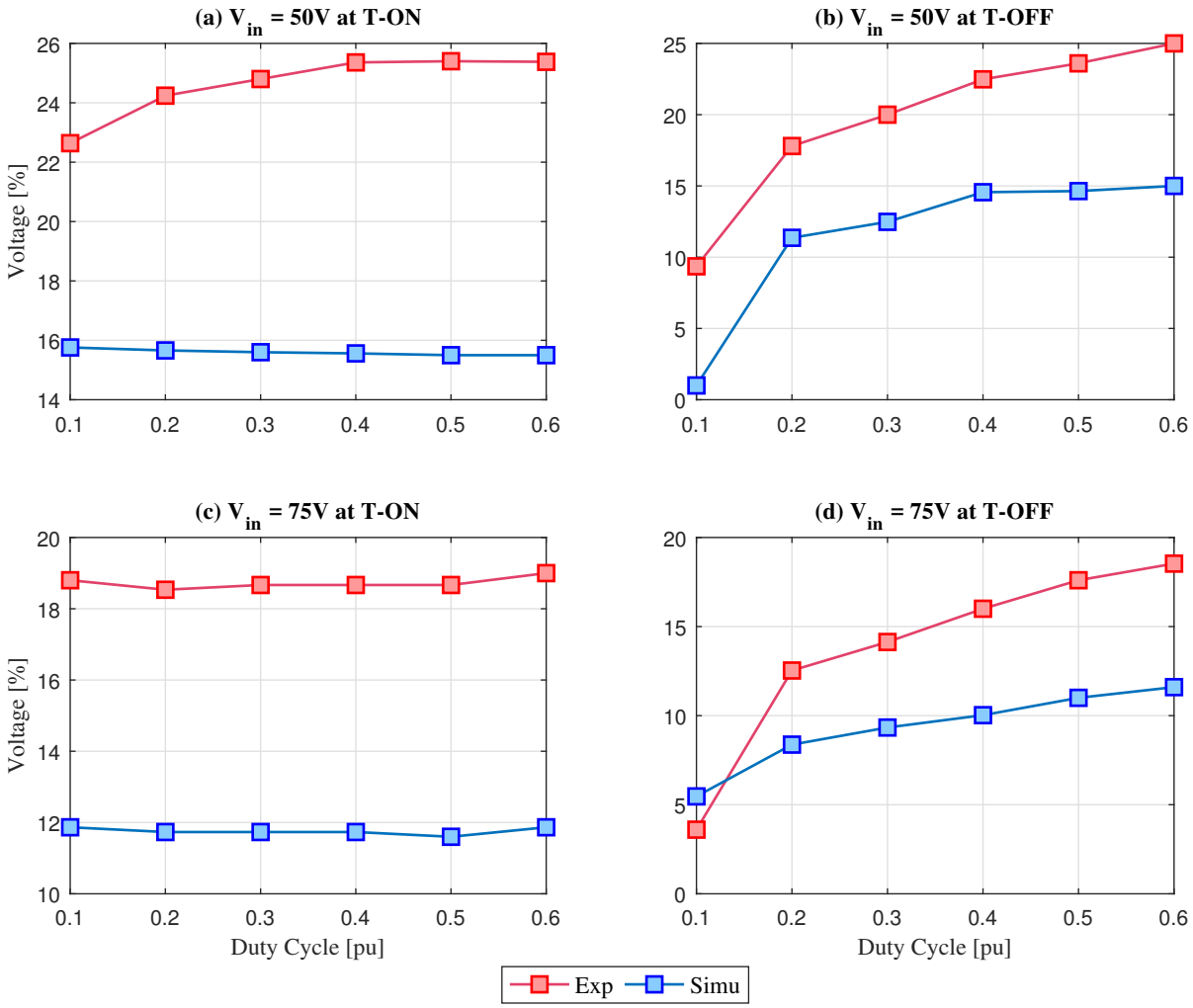


Figure 4-17: Drain-to-source (V_{DS}) peak voltages produced in switch 1 (SW1) at the turn-on and turon-off events for different duty-cycles and different test voltages: (a) turn-on at $V_{in} = 50V$; (b) turn-off at $V_{in} = 50V$;(c) turn-on at $V_{in} = 75V$;(d) turn-off at $V_{in} = 75V$.

In Figure 4.18, the same situation than in the previously commented figure is exposed for SW2. It can be seen how in this case, the better approximations are achieved in the case of the turn-on event, This fact is produced because SW1 is complementary to SW2. However, in the case of $V_{in} = 75V$, the voltage difference between the experiment and simulation results increases in a faster way than in case of Figure 4.17 (d). This is because the peak voltage values of the experimental test increase with a larger slope.

In the case of the turn-off, a similar behaviour than in the case of Figures 4.17 (a) and (c) is shown, with a larger difference voltage value reached between the simulation and the experiments. The largest peak voltage value obtained is produced at the turn-on for $50V$ and duty $= 0.6$ for both, the experimental and simulation results, which matches with the previous case of SW1. Has it can be observed, the peak voltage values reached in SW2 are larger than in SW1.

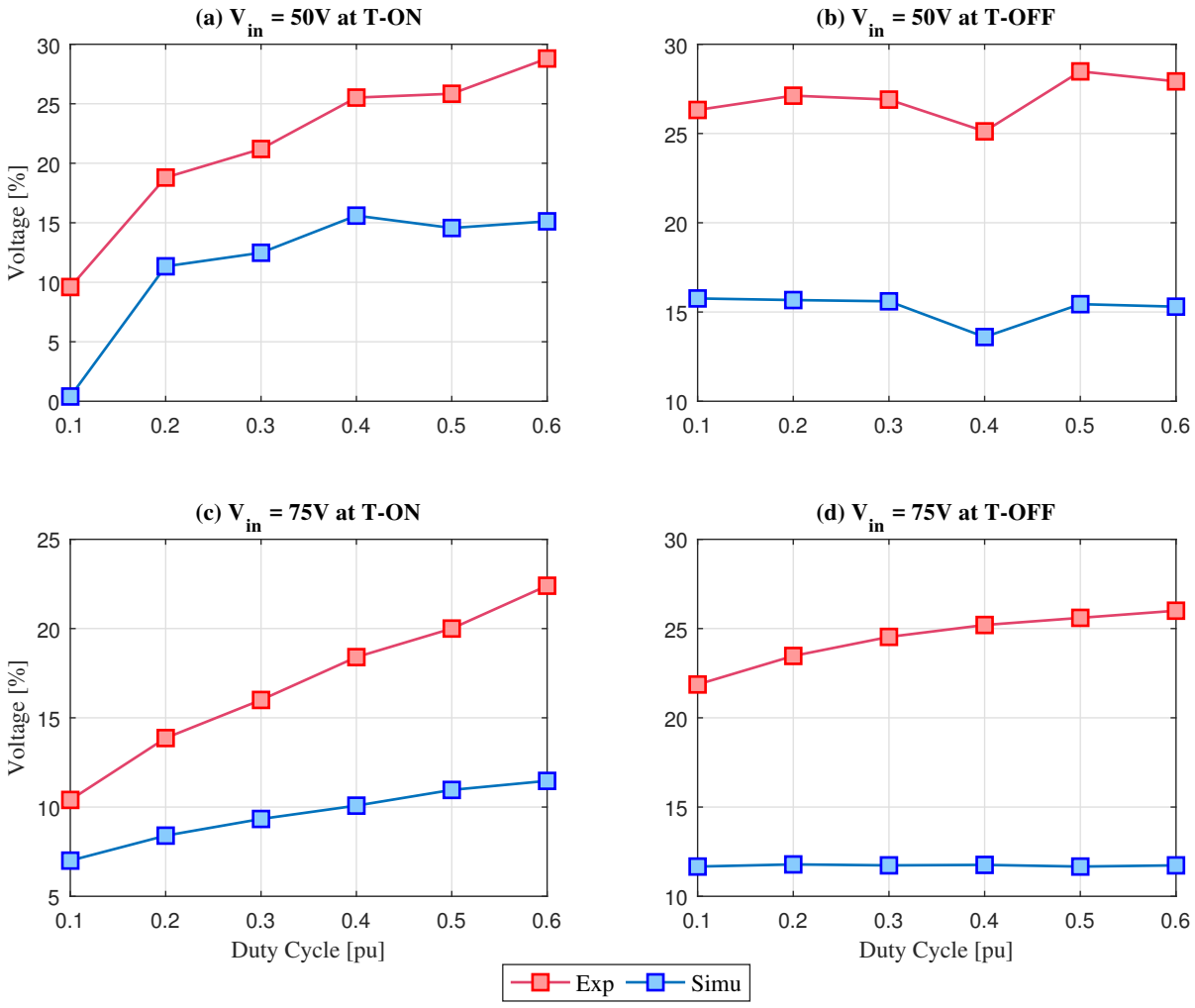


Figure 4-18: Drain-to-source (V_{DS}) peak voltages produced in switch 2 (SW2) at the turn-on and turon-off events for different duty-cycles and different test voltages: (a) turn-on at $V_{in} = 50V$; (b) turn-off at $V_{in} = 50V$;(c) turn-on at $V_{in} = 75V$;(d) turn-off at $V_{in} = 75V$.

4.2.3 dV/dt produced at the turn-on and turn-off events

The voltage derivative (dV/dt) at the turn-on and turn-off events in the synchronous buck converter for switches 1 and 2 (SW1 and SW2 respectively) will be analysed in this section. As in the other cases, different voltage levels and different duty-cycles will be studied.

In Figure 4.19, the dV/dt produced in SW1 and SW2 at the turn-on and turn-off events for $V_{in} = 50V$ at different duty-cycles is shown. It can be observed that in cases (b) and (c) (which corresponds to SW1 and SW2 operating in complementary mode), a very good match between the experimental and simulation results is obtained. However, in cases (a) and (d) the simulation does not coincide with the experimental results. It can be also checked how the dV/dt increases with the duty for cases (b) and (c), and decreases for cases (a) and (b). However, the duty dependency of the voltage derivative is much higher for cases (b) and (c). The highest dV/dt is obtained experimentally in (d) for a duty = 0.2.

It is also remarkable the difference produced between dV/dt values for the turn-on and turn-off (in both switches). This phenomenon can be explained by looking at Figure 4.12: it can be seen how in the second switching event the dV/dt is much slower. This phenomenon is produced due to the fact that in the second switching, SW2 is blocking the current and SW1 is conducting, but during the dead-time, SW2 is forced to conduct due to the charge accumulated in the inductor. For this reason, the voltage in SW2 needs to drop to 0, and V_{GS} in SW1 increases, and the transition is produced slowly since SW1 has to stop conducting.

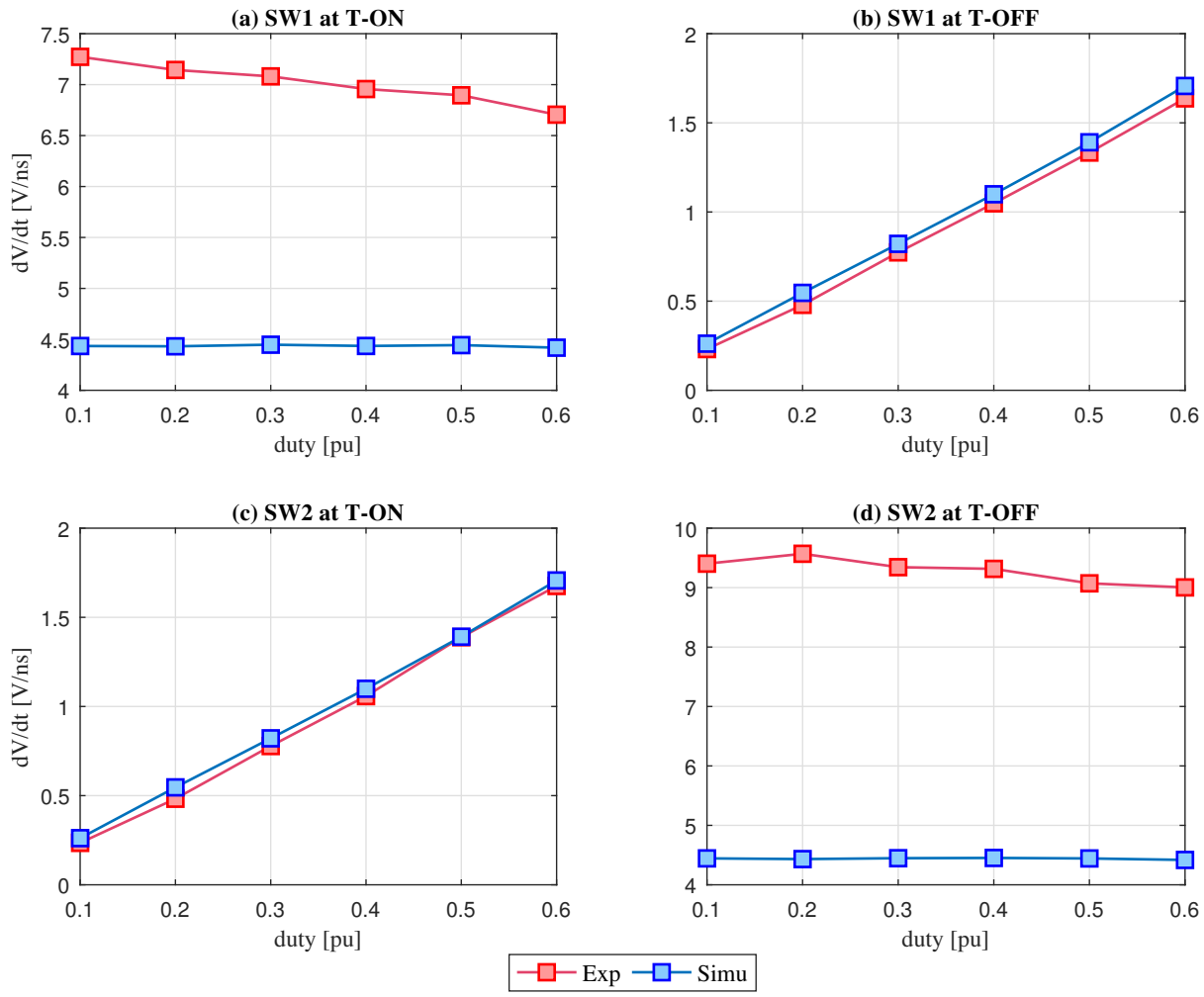


Figure 4-19: Drain-to-source (V_{DS}) dV/dt in $[V/ns]$ produced in switch 1 (SW1) and switch 2 (SW2), at turn-on and turn-off events for $V_{in} = 50V$ at different duty-cles: (a) SW1 and turn-on; (b) SW1 and turn-off;(c) SW2 and turn-on;(d) SW2 and turn-off.

In Figure 4.20, the same test performed in the previous figure is exposed but now for $V_{in} = 75V$. As it can be clearly appreciated, the best match between the simulation and experimental results is produced at the turn-off for SW1 and turn-on for SW2 (which occurs simultaneously, as seen previously). The simulation model in this case is really accurate. However, in cases (a) and (d), the simulation does not represent properly the expected performance of the GaN device in terms of the voltage derivative.

With respect to the experimental results, the largest dV/dt is produced in the turn-off of SW2 (case (c)). In this case, the voltage derivative practically does not depends on the duty-cycle, as well as in case (a) for SW1. On the contrary, in cases (b) and (c), the voltage derivative varies considerably with the duty, particularly the rate of variation increases with the duty (with the output voltage and current).

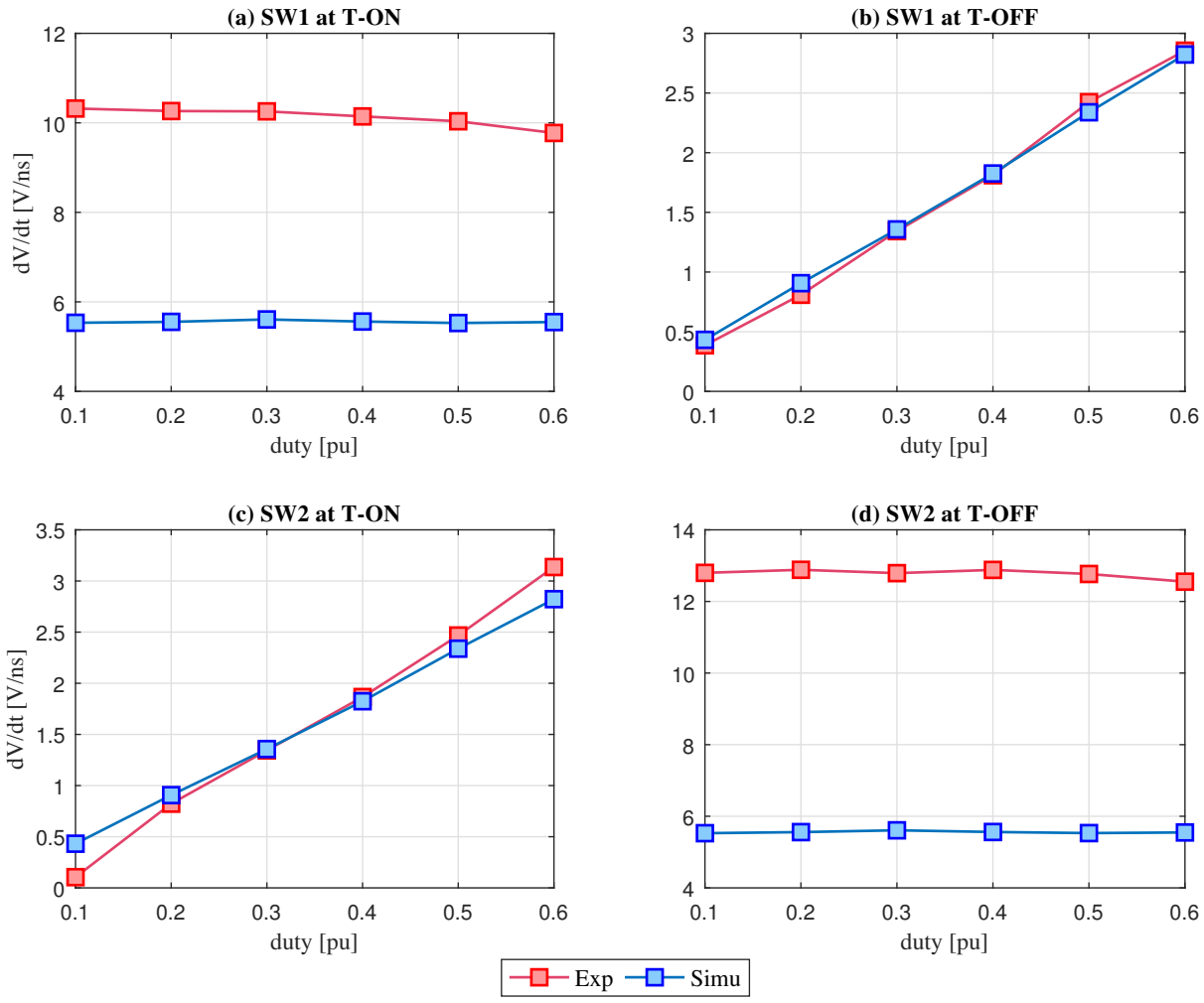


Figure 4-20: Drain-to-source (V_{DS}) dV/dt in $[V/ns]$ produced in switch 1 (SW1) and switch 2 (SW2), at turn-on and turn-off events for $V_{in} = 75V$ at different duty-cles: (a) SW1 and turn-on; (b) SW1 and turn-off;(c) SW2 and turn-on;(d) SW2 and turn-off.

4.2.4 Analysis of the Synchronous-Buck Efficiency

In this subsection, an analysis of the synchronous buck converter efficiency carried out in the simulations will be commented. The converter has been analysed as in previous cases for $V_{in} = 50V$ and $V_{in} = 75V$ at different duty-cycles.

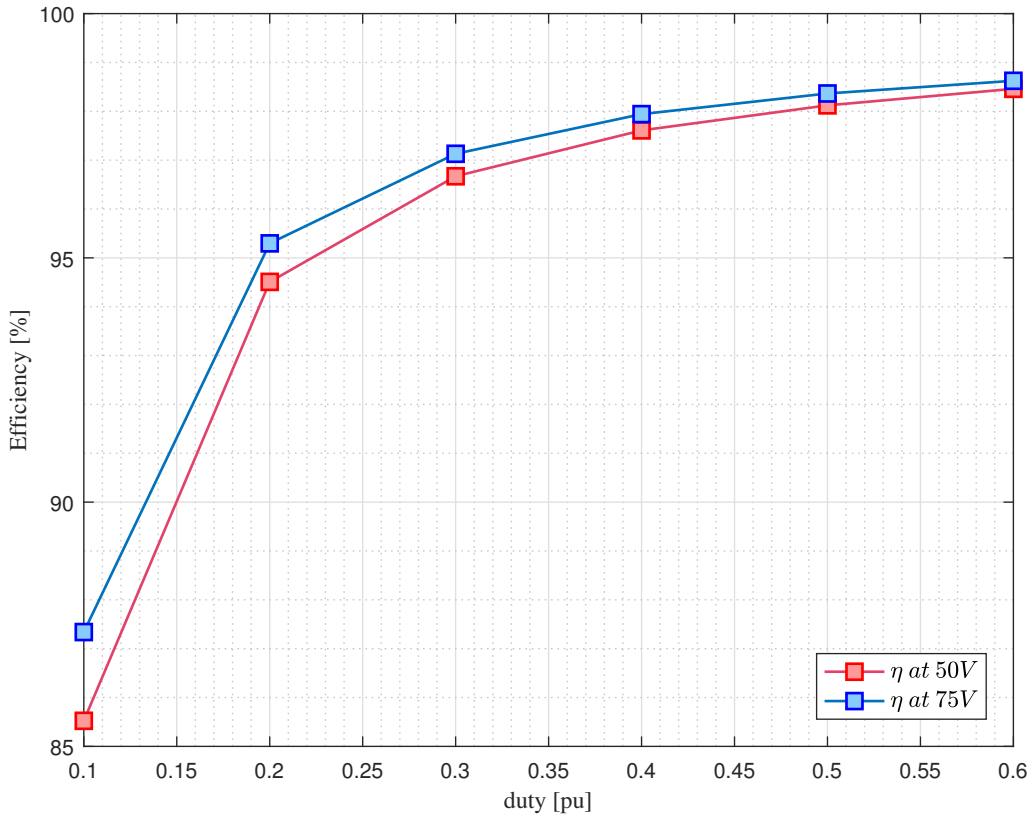


Figure 4-21: Efficiency of the synchornous buck converter obtained in the simulations for different input voltage levels at different duty cycles.

As Figure 4.21 shows, the efficiency of the synchronous buck converter is directly related with the duty-cycle. It can be observed that for both voltage levels, the converter efficiency increases with the duty-cycle, obtaining the lowest performances for duty = 0.1 and increasing significantly the efficiency from duty = 0.2. This phenomenon is produced because in switch 2 the conduction losses are more significant than the switching losses, and while increasing the duty of SW1, the duty of SW2 is reduced. The voltage across the drain-to-source of the low-side GaN HEMT is

much lower during turn-on and turn-off transitions due to the conduction of the 2DEG during the dead time. As a result, switching losses in the low side are often negligible. Therefore, the converter efficiency increases when reducing the dead time for SW2 (reduce conduction of the device). In case of SW1, the switching losses are more relevant at lower duty-cycles and at high duties, conduction losses become dominant.

It can be also checked that the the best performance is achieved for an input voltage of $75V$ for all the evaluated operating points. The highest efficiency value is produced at duty = 0.6 and is: $\eta = 98.5\%$.

Notice that it would be required to consider the necessary power that the gate drivers consume. Therefore, the converter efficiencies shown in Figure 4.21 would be lower in reality.

4.2.5 Comparison of the Synchronous Buck-Converter Efficiency: GaN vs Si

In order to have a simple comparison of the GaN efficiency with another common technology, the buck converter simulation was adapted in order to use Si power MOSFETs. Particularly, the power device *CoolMOS 650V G7* model, which presents similarly ratings than the used GaN device, was employed in the simulation for comparing the buck converter efficiency.

In Figure 4.22, the efficiencies obtained in the simulations for the synchronous buck converter are presented. The tests were performed for $V_{in} = 50V$ and $V_{in} = 75V$, at different duty-cycles. As it can be seen, for both voltage levels, the tests performed with the GaN devices show a higher efficiency for all the evaluated operating points. It can be clearly appreciated how the difference between both devices efficiencies is larger at low duty-cycle values, and such difference is quite reduced for larger duty values. In order to improve the converter efficiency, it can be studied the possibility of adding a Schottky diode in parallel with the second power device in order to minimise the losses produced during reverse conduction.

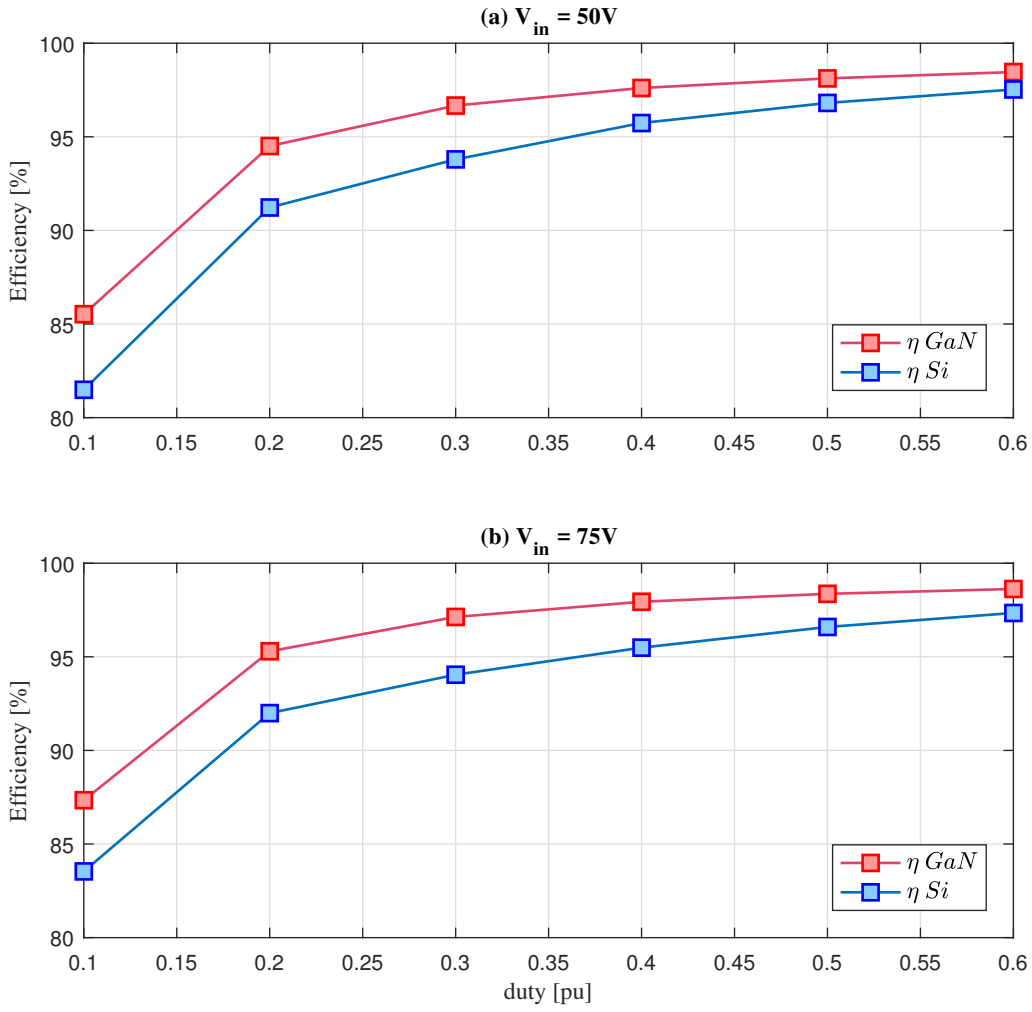


Figure 4-22: Comparison of the synchornous buck converter efficiency obtained in the simulations when using GaN and Si technology for different input voltage levels at different duty cycles.

Chapter 5

Conclusions and Future Work

5.1 Conclusions

In this project, an analysis of the switching characteristics and transient response of the GaN HEMTs has been performed. During the experiments, several setbacks arose which slowed down significantly the advances in the tests. However, considerably information could be extracted from the finally preformed experiments, mainly focused on the drain-to-source voltage transient response. Hence, the switching characteristics of this electrical parameter were studied in double-pulse tests and in a synchronous-buck converter for different points of operation.

5.1.1 Double-Pulse Tests

As it could be seen in the transient response analyses, the match between the simulation and experimental results was better in the case of the turn-off events. In the case of the simulation turn-on results, the oscillations produced were too low in comparison with those produced in the real experiments. In case of the experiments, the overshoot produced in both, turn-off and turn-on events, was reduced (in percentage of the test voltage) while increasing the voltage. For the turn-off events, the transient response observed was quite dependant on the test current, while in the turn-on events the current dependency was much lower for all the evaluated voltages.

It is also remarkable the oscillations produced in the simulations in the turn-on just before switching, that was not present in the experiments.

In case of the peak voltages produced in the turn-off event for the DPTs, it was seen that the largest peaks reached (in percentage of the applied test voltage) were observed for the lowest test voltage, and decrease with the voltage, for both, the simulation and experiment results. It was also checked that the peaks produced increase with the current, and for the same test voltage and different currents, the peak voltages vary much more for lower test voltages. For the turn-on events, it could be observed how the peak voltages reached were much lower than in the previous case. Therefore, the effect of having a greater resistor for controlling the dV/dt slew rate to avoid large overshoot and reduce power losses due to commutations was checked. It was also observed that, for the turn-on, the peak voltages did not depend on the test currents practically.

For the voltage derivative, it was observed that in the turn-off event, the dV/dt increases with the test voltages and currents, while in the turn-on analyses the voltage derivative was reduced with the test current due to the increase of the voltage fall time. In general, higher dV/dts were observed for the turn-off. A good match between the experiments and the simulation was achieved for the turn-off, while in the turn-on, the simulation values did not adapt perfectly to the obtained experimental values. With respect to the dV/dt results obtained for the same test voltage and different current values, the variations were larger in the case of the turn-off, for high test voltages. In the case of the turn-on, the dV/dt variations for the same test voltage did not depend too much in the current.

5.1.2 Synchronous Buck Converter Tests

In the transient analyses of the synchronous buck converter tests it could be checked that for switch 1 and turn-off, the simulation response did not match the oscillations produced in the experiments, while in the turn-on this response was improved. However, the loop inductance circuit used in the simulations to represent the behaviour of the experimental kit loop inductance has to be improved. On the other hand, it

could be appreciated that the overshoot produced in the turn-off events was quite dependant on the duty-cycle value, while the turn-on response did not depend too much. In the case of switch 2, it could be checked that the oscillations produced were similar than those obtained for the switch 1 but coinciding with the opposite switch events, since the devices operate in complementary mode. In general, the simulation model can be improved to match the experimental results.

During the analyses of the peak voltages for the turn-off and turn-on events, it was observed that the best match between simulation and experiment was produced in the case of the turn-off event for SW1 and turn-on for SW2, since both switches are complementary. It was also checked that for the turn-off event in SW1 and turn-on in SW2 the peak voltages vary much more with the duty than in the other cases. Generally, higher peak voltages were observed in SW2 than in SW1.

In case of the voltage derivative for the synchronous buck converter, it was observed that very good matches between the experiments and simulations were achieved for cases (b) and (c) for both evaluated voltage levels. In these cases, the dV/dt duty dependency was also higher than in cases (a) and (d). The highest dV/dt was produced experimentally in SW2 at the turn-off for $75V$ (Figure 4.20 (d)).

5.2 Future Work

Due to the setbacks produced during the experimental tests, as well as the impossibility of measuring the drain current of the devices with the finally used experimental kit, there is a lot of future work that can be implemented:

- To go on with the experiments carried out, it will be necessary to solve the problem caused by the EMI between the converter and the computer. This can be addressed by using some type of filter between these elements, or by using optical fibre cables to transmit the control signals form the laptop to the experimental kit.

- Secondly, it would be necessary to perform a study of the analyses carried out

but now observing the drain current transient response. With this information, it will be possible to extend the knowledge of the switching characteristics as well as to get the power losses produced in the transistors

- Then, it would be possible to analyse the behaviour of the switches in other converter topologies (half-bridge, full-bridge, other DC-DC converters, etc.) for high-power fast-switching applications.

- An optimization of the simulations performed can be done, improving the loop inductances with respect to the experimental kit used. With this, several analyses could be performed, such as optimization of the gate resistance values, snubber circuits, optimization of dead-times, etc.

- A thermal analysis can be also performed to observe the heat distribution in the SMD package and improve the thermal management of this design.

- It would be also interesting to analyse the behaviours produced when adding an antiparallel diode for improving reverse conduction.

- An experimental and simulation comparison with similar ranging SiC transistors to analyse the advantages and disadvantages (overshoots, peak voltages, dV/dt, power losses, thermal resistance, efficiency, etc.) of both power devices in DPTs and other converter topologies.

- A study of the packaging impact on the switching losses, the reduction of the loop inductance and the thermal management drawbacks. Remember that the employed transistors used SMD packages.

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