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An ac-dc PFC single-stage Dual Inductor Current-Fed Push-Pull for HB-LED lighting applications

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Abstract— An ac-dc single-stage driver for High Brightness Light-Emitting Diodes with galvanic isolation is presented in this paper. The driver is based on a Dual Inductor Current-Fed Push-Pull converter with each inductor operating in Boundary Conduction Mode. The interleaving between the two inductors enables the converter to reduce the high input current ripple inherent to a BCM. Moreover, it is fully compliant with IEC 1000-3-2 Class C and it is able to achieve a high Power Factor. Its low component count, simplicity and overall outstanding characteristics make this current-fed topology suitable for medium power range HB-LED drivers in low cost applications. The proposed topology has been tested on a 100W prototype for the full range of the US single-phase line voltage, feeding several HB-LED strings, with an output voltage equivalent to 48V at full load. The prototype achieves a maximum efficiency of 92% with a 0.99 power factor, 8% THD at full load while guaranteeing good quality light.

Keywords— Single phase, ac-dc power conversion, Power Factor Correction, HB-LED driver

I. INTRODUCTION

High-Brightness Light-Emitting Diodes (HB-LEDs) are increasingly becoming the main source of artificial light in homes, offices and streets due to their reliability, long life, energy efficiency and low maintenance requirements. However, the driving of HB-LEDs with primary access to single-phase AC requires the use of a converter that is able to achieve high efficiency, a long lifespan comparable to that of the HB-LEDs and Power Factor Correction (PFC) in order to comply with the regulation for both residential and commercial lighting. A high Power Factor (PF) is required to maximize the power transferred from the grid. This is the reason why, Energy Star® [1] requires an 0.7 PF for residential lighting and an 0.9 PF for commercial lighting. Furthermore, the low-frequency harmonic content of the line current must comply with IEC 1000-3-2 Class C [2]-[4], which establishes a very strict harmonic content for the line current in lighting equipment of more than 25 W. Therefore, the line current needs to have a sinusoidal shape following that of the input voltage.

Traditionally, HB-LED drivers are based on a high-performance ac-dc PFC converter, followed by a dc-dc converter, which in most situations has galvanic isolation and provides a constant current to the HB-LEDs in order to comply with the aforementioned regulations. In most scenarios, however, the cost of the HB-LED driver is the main concern and a single-stage needs to be used to reduce the amount of components and complexity of the HB-LED driver. This is particularly important in low to medium power range HB-LED drivers, where galvanic isolation is recommended for safety requirements. Accordingly, isolated buck-boost topologies like the flyback working in Discontinuous Conduction Mode (DCM), which achieves unity PF naturally, are widely used in this application [5]-[10]. Although these topologies have a low component count, they suffer from low efficiencies (<90%) and the inability to remove the bulk capacitor required in PFC. However, the removal of the bulk capacitor is not always possible in a single-stage without including more active components [10]-[14] or distorting the input current [15] [16]. This occurs due to the pulsating input power of the grid, which must be decoupled from the HB-LEDs in order to avoid the well-known flicker phenomenon.

Another topology that is able to achieve unity PF naturally, by means of its control, is the boost converter. The boost converter is normally used as a front-end, ac-dc, PFC, converter operating either in Boundary Conduction Mode (BCM) or employing a Multiplier-Based Control (MBC) [17] [18] with a cascaded step-down converter. Hence, the isolated variations of the boost converter family are suitable to be used as a single-stage PFC, (i.e. current-fed based isolated converters). However, current-fed based isolated converters are rarely used in PFC due to the drawbacks they present. For instance, they have a complex transformer design, which may hinder the efficiency of the single stage, and require a demagnetizing path for the main inductance, as reported in previous literature [19]. Nevertheless, previous literature does include some papers on single-stage, ac-dc, PFC, current-fed based, isolated, converters, such as the push-pull [20] or the full-bridge [21]

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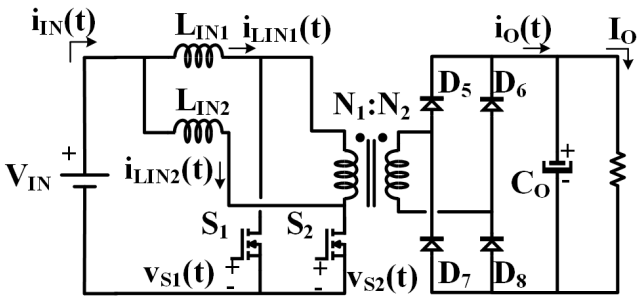

Fig. 1. A dc-dc Dual Inductor Current-fed Push-Pull [22] [23].

both working in CCM with a MBC. Among the current-fed push-pull topologies, the Dual Inductor Current-fed Push-Pull (DICPP), see Fig. 1, proposed in [22], [23] as a dc-dc converter can deal with the efficiency issues intrinsic to current-fed topologies due to complex transformer design, thanks to its simpler transformer (i.e. two windings one for the primary side and the other for the secondary side), while employing two MOSFET referenced to the same ground. In fact, the DICPP uses the same amount of switches as the classic Current-Fed Push-Pull (CPP) [23] whole only adding one more magnetic component. Furthermore, the switches used in the DICPP (S_1, S_2) withstand half the voltage when compared to those in the CPP, therefore the switches can be downsized in terms of voltage and the transformer requires less isolation, so its complexity is decreased even further. These facts are particularly important to reduce the parasitic components that may cause the topology to behave inappropriately due to resonances that will impact both the output current or the losses in the passive snubbers, which will decrease the efficiency of the single-stage.

The proposal of this work is to revise the DICPP topology, which has been widely used in dc-dc, high power, low input voltage, high input current, step-up applications (i.e. fuel cells, battery storage and photovoltaic applications) [24]-[26] and has never been proposed as an ac-dc PFC [27]. Hence, the aim is to study its feasibility as an ac-dc, single-stage, converter with PF close to unity to be used in HB-LED lighting applications. The working principle of the DICPP Adapted for PFC (DICPP-APFC) carried out in Section II, shows that each switch controls the magnetization of the inductor in its branch. This feature makes suitable the operation of each inductor in BCM while demanding a sinusoidal current at each branch. In fact, this behaviour leads to a reduced ripple at the input current due to the sum of the input currents of each branch, which are phase shifted 180º in terms of switching frequency. Furthermore, Section III shows the proposed control based on only sensing the information of the output current before being filtered by the bulk capacitor ($i_o(t)$) in order to maintain the simplicity of the solution. Finally, Section IV will show the experimental results, making the DICPP-APFC a plausible solution for single-stage PFC in HB-LED drivers since the DICPP- APFC is able to achieve higher efficiency and lower input current ripple than traditional AC-DC single-stage converters.

II. Working Principle

A. Static Analysis

The concept of the HB-LED driver presented in this paper (i.e., the DICPP) is based on [22], where it was proposed as a dc-dc converter working in CCM. Moreover, current-fed push-pull topologies are normally used with low input voltages (i.e. 0-50V) and high currents in power conversion for fuel cells [24], battery storage [25], photovoltaic [26] and electric vehicle applications [28], due to their transformer limitations and voltage stress on the main switches. The present paper proposes to increase the scope of the topology to work as an ac-dc PFC by operating in BCM in the range of hundreds of watts to increase the efficiency by applying well-known control methods used in interleaved PFC boost rectifiers. Hence, increasing the input voltage range of the topology.

In order to achieve good quality rectification at the input current, a Loss Free Resistor (LFR) [30] behavior is required. It is well known that a boost converter operating in BCM (i.e. constant on-time and variable frequency) can achieve an LFR behavior naturally. Therefore, the DICPP should also be able to work as a PFC by operating in BCM since it is a converter from the boost family. In order to verify its operation as an ac-dc PFC, the converter behaviour is going to be analyzed in terms of switching and line frequency.

The operation of the HB-LED driver in BCM is summarized in Figs. 2 and 3. Fig. 2, shows the three different stages that the topology undergoes in a switching period (T_s), while Fig. 3 shows the most important waveforms to understand its operation. Furthermore, the stages shown in Fig. 2 correspond with the waveforms and interval times depicted in Fig. 3 (b). In order to correctly exemplify the operation of the HB-LED driver in a switching period the elements that are not being used in each stage are shaded. In that regard, Fig. 2 (a) depicts the conduction from [t_0, t_1] and [t_2, t_3] when the two main switches (i.e., S_1 and S_2) are closed and the primary side of the transformer is short-circuited. Hence, both inductors are being magnetized by the input voltage ($v_{IN}(t)$), as shown in Fig. 3 (b). The next interval [t_1, t_2], shown in Fig. 2 (b), represents the stage when S_1 is closed and S_2 is open. During this time, L_{IN1} keeps being magnetized, whereas L_{IN2} is being demagnetized. At this time, power is flowing through the transformer, D_6 and D_7 supplying the load. As was previously stated, the next time interval from t_2 to t_3 is the same as the one represented by Fig. 2 (a). Finally, the last stage [t_3, t_4] shown in Fig. 2 (c) represents the stage when S_1 is open and S_2 is closed, thereby magnetizing L_{IN2} and demagnetizing L_{IN1} while giving power to the load through the transformer, D_5 and D_8, as it can be seen in Fig. 3 (b).

Fig. 3 (a) shows in red the input and output currents averaged at switching frequency during a half line period, while Fig. 3 (b) shows the time domain waveforms to analyze the topology in detail (i.e. at switching frequency). In Fig. 3 (b), it can be seen at a glance that, the time L_{IN1} is being magnetized is equal to the on-time of switch S_1 and the magnetizing time for L_{IN2} is equal to the on-time of switch S_2. It should be noted that L_{IN1} magnetizes regardless of the on-time of S_2 and L_{IN2} magnetizes regardless of the on-time of S_1. Therefore, the

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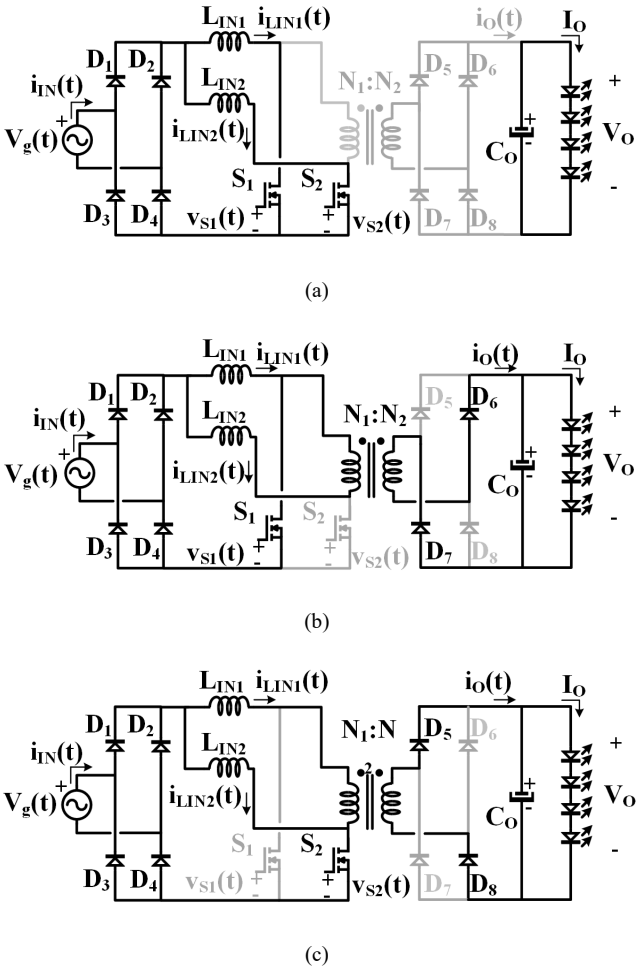

Fig. 2. Stages of the DICPP-APFC. (a) [t_0, t_1] [t_2, t_3] Both S_1 and S_2 are closed. (b) [t_1, t_2] S_1 is closed and S_2 is open. (c) [t_1, t_2] S_2 is closed and S_1 is open.

topology can be modelled as two independent boost converters interleaved with a 180º phase-shift and galvanic isolation. This fact will reduce the input current ripple at switching frequency, as reported in [33] for interleaved boost converters. Hence, improving the behaviour of the converter since the EMI filter is not as penalized in size as in other ac-dc, single stage, converters working either in DCM or BCM [34].

The control of the main switches (i.e. S_1 and S_2) is based on generating the control signal for v_{S1} and phase shifting this same signal 180º to control $v_{S2}(t)$ by means of a Phased Locked Loop (PLL). Note that the duty cycle (d(t)) at each switch of this converter should always be higher than 50% due to the fact that, when both switches S_1 and S_2 are open, there is no demagnetizing path for L_{IN1} or L_{IN2}, which could lead to their destruction due to overvoltage. This is an intrinsic characteristic of current-fed converters, hence the need for a stage that overlaps both control signals, see Fig. 2 (a). As regards the stages in Figs. 2 and 3, the converter relationship between output voltage and input voltage in BCM can be obtained by studying the volt-second balance on one of the inductors. The converter gain can thus be defined by,

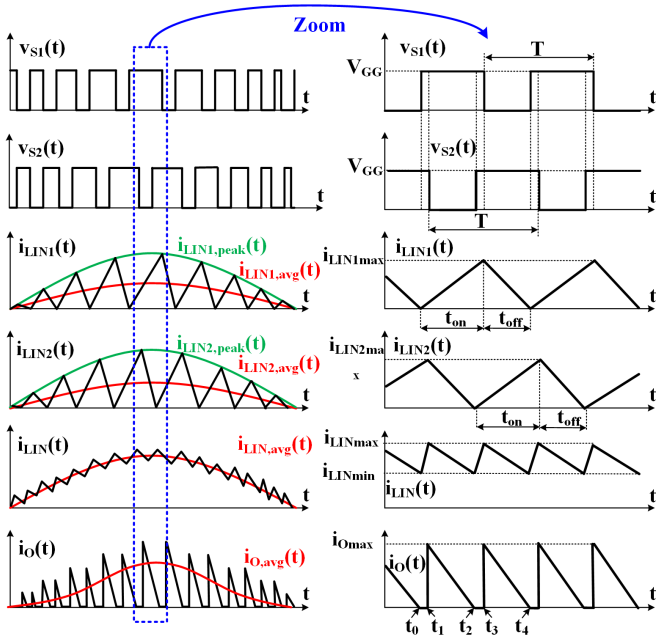

Fig. 3. Most characteristic waveforms of the topology. (a) Line frequency. (b) Time domain.

$$m = \frac{v_o}{v_g(t)} = \frac{N_2}{N_1(1-d(t))}\,, \tag{1}$$

where v_o is the output voltage, $v_g(t)$ is the input voltage, and N_2 and N_1 are the number of turns of the secondary and primary windings, respectively.

From the previous analysis, it can be seen that each inductor of the DICPP-APFC works independently. S_1 controls the magnetizing of L_{IN1} and S_2 controls the magnetizing of L_{IN2}. Therefore, it can be assumed that if both L_{IN1} and L_{IN2} are equal (i.e., $L_{IN1} = L_{IN2} = L$), by studying the voltage balance in the inductors during stage [t_1,t_2] for L_{IN1} and [t_3,t_4] for L_{IN2}, the inductor peak current (i.e. $i_{LIN1,peak}$ and $i_{LIN2,peak}$) can be defined as,

$$i_{L_{IN1},peak}(t) = \frac{v_{gp}}{L}\sin(\omega t)t_{on}, \tag{2}$$

$$i_{L_{IN2},peak}(t) = \frac{v_{gp}}{L}\sin\left(\omega\left(t-\frac{T_s}{2}\right)\right)t_{on}, \tag{3}$$

where v_{gp} is the peak value of the input voltage, t_{on} is the on-time of each driving signal, which coincides with the magnetizing time of each inductor and ω is the angular frequency of the line voltage. If (2) and (3) are averaged in a switching period, the average current through the inductors can be expressed as,

$$i_{L_{IN1},avg}(t) = \frac{v_{gp}}{2L}\sin(\omega t)t_{on}, \tag{4}$$

$$i_{L_{IN2},avg}(t) = \frac{v_{gp}}{2L}\sin\left(\omega\left(t-\frac{T_s}{2}\right)\right)t_{on}. \tag{5}$$

Therefore, the current in both branches (i.e. $i_{LIN1,avg}$ and $i_{LIN2,avg}$) will be sinusoidal; in this case, phase shifted 180º from the point of view of the switching period (T_s). Hence, the input

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current demanded by the HB-LED driver will be sinusoidal, as it is the sum of the two sinusoidal waveforms, given that the delay between them (i.e., $T_S/2$) is negligible from the point of view of the line period, as can be seen in Fig. 3 (a). Therefore, the average input current at switching frequency ($i_{IN,avg}$) can be expressed as

$$i_{IN,avg}(t) = i_{L_{IN1,avg}}(t) + i_{L_{IN2,avg}}(t) =$$
$$= \frac{v_{gp}}{2L} t_{on} sin(\omega t) + \frac{v_{gp}}{2L} t_{on} sin\left(\omega\left(t - \frac{T_s}{2}\right)\right) \cong \quad (6)$$
$$\cong \frac{v_{gp}}{L} t_{on} sin(\omega t)\,.$$

For a correct operation in BCM, t_{on} needs to be kept constant at a certain value guaranteeing that the converter will demand a certain amount of power and that the off-time of the driving signal (t_{off}) will vary depending on the demagnetizing time of each of the inductors until reaching the zero current value. The zero current value must be detected by a Zero Current Detection (ZCD) circuit based on a comparator.

Given that the average input current will be a sine wave, as stated in (6), by multiplying it by the input voltage, the instantaneous input power can thus be defined by,

$$p_g(t) = \frac{v_{gp}^2}{L} t_{on} sin^2(\omega t)\,. \quad (7)$$

By averaging (7) at line frequency, the following relationship between t_{on} and several well-known design parameters can be formulated as,

$$t_{on} = \frac{2P_G L}{v_{gp}^2}\,, \quad (8)$$

where P_G is the averaged input power processed by the HB-LED driver in a line period. From (8), the LFR behaviour and value can be obtained by considering the input power as a relation between v_{gp} and a resistor that models the input impedance of the converter (R_{LFR}),

$$R_{LFR} = \frac{L}{t_{on}}\,, \quad (9)$$

Eq. (9) shows that by applying the correct control method to operate in BCM the converter is going to behave as resistor. Therefore, the input current will follow the input voltage which will result in achieving almost unity PF. Moreover, by applying voltage balance to one of the inductors, (10) can be obtained as,

$$\frac{v_{gp}}{L} t_{on} = \frac{\frac{N_1}{N_2} v_o - v_g(t)}{L} t_{off}(t), \quad (10)$$

where t_{off} is the off-time of the control signal of the switches.

From this equation, the variation in the switching period over time and the switching frequency can be obtained as,

$$T_s(t) = t_{on} + t_{off}(t) =$$
$$= \frac{\frac{N_1}{N_2} v_O}{\frac{N_1}{N_2} v_O - v_{gp}|sin(\omega t)|} t_{on}\,, \quad (11)$$

From (11), the maximum and minimum frequency values can be obtained. These frequency values are of importance for the correct design of the topology: selection of the main switches, magnetics and t_{on}. Hence, yielding,

$$f_s(t) = \frac{\frac{N_1}{N_2} v_O - v_{gp}|sin(\omega t)|}{\frac{N_1}{N_2} v_O} \frac{1}{t_{on}}\,. \quad (12)$$

B. Design criteria of the HB-LED driver

In order to correctly design for the HB-LED driver, some steps need to be followed, and are summarized below.

First of all, the transformer relationship needs to be obtained from (1), considering v_{gp} as the maximum value of the input voltage (i.e., V_{gpmax}), v_o as the output voltage at the full dimming point, and d_{min} as the minimum duty cycle acceptable, which should be around 55% to avoid periods where the control signals do not overlap.

After obtaining the transformer relationship, the duty cycle needs to be calculated under nominal conditions. The duty cycle and the desired switching frequency can then be used to obtain the required inductance from (8). If the calculated inductance has an acceptable value, (12) should be used to check whether the frequency range is as well. If not, then the inductance value needs to be adjusted to suit design specifications. Guaranteeing that the lowest frequency value is higher than 20 kHz constitutes a good practice to avoid any audible noise in the converter. Having calculated all the above parameters, the next step will be to select the main switches. It is hence necessary to know the maximum current and voltage that they will have to withstand. From (1) and (7),

$$V_{Smax} = \frac{V_{gpmax}}{1 - d_{min}}\,, \quad (13)$$

$$I_{Smax} = \frac{P_g}{V_{gpmin}}, \quad (14)$$

where V_{gpmin} is the voltage peak of the minimum voltage in the range. As can be seen, the maximum voltage withstood by the switches relies entirely on the maximum input voltage and the minimum duty cycle. Considering that the minimum duty cycle is not allowed to go lower than 55%, the maximum voltage withstood by the switches will increase linearly with the input voltage. Therefore, the European/Universal input voltage range would require the use of switches with a higher breakdown voltage (i.e. 900/1200 V), which would mean the use of Silicon Carbide (SiC). In the present work, a prototype will be constructed for US range in order to validate the idea. Although it is not shown in Fig. 2, the HB-LED driver also includes a clamping snubber to protect both switches from overvoltage. A passive snubber is added to the circuit to protect the switches from voltage spikes that can occur due to the leakage inductance of the transformer. An active clamp can also be used for this matter [24] to further improve the efficiency of the HB-LED driver.

To select the high frequency diodes (D_5-D_8), the maximum values that need to be taken into account are:

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$$V_{Dmax} = V_o - \frac{N_2}{N_1} V_{gpmin}, \quad (15)$$

$$I_{Dmax} = \frac{N_1}{N_2} I_{L_{IN1},peak,max}, \quad (16)$$

where $I_{LIN1,peak,max}$ is the maximum input current of the HB-LED driver. As can be seen, the breakdown voltage of the high frequency diode bridge can be low enough to guarantee the use of a very low forward voltage diode to improve the efficiency of the driver.

Finally, in order to be able to demagnetize both inductors, in a case were the HB-LED driver needs to be shut down, another winding is added to provide a path for the demagnetization to occur, as has been previously reported in [18][19]. This demagnetization path, will work also as a protection in case of failure of the driving of the active switches.

C. Transformer design

In push-pull converters, where the current through the primary transformer winding is abruptly changed whenever a transistor switches, the leakage inductance of the transformer should be as low as possible. Otherwise, each switching instant will produce a significant voltage spike, making the use of higher voltage rated transistors or protective devices such as snubbers necessary.

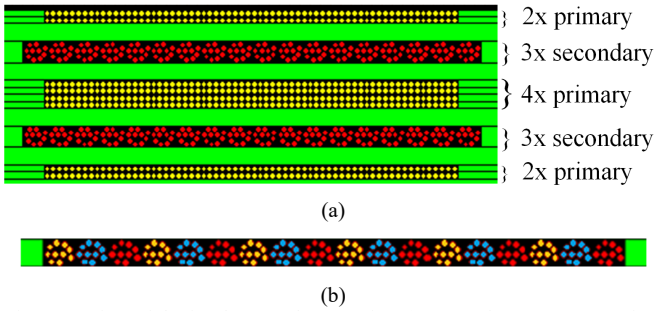
Winding interleaving is a well-known procedure for reducing leakage inductance. However, as a side effect of adding a high number of thinner sub-windings, a really low leakage inductance can only be obtained at the cost of a higher parasitic capacitance. This has proved to be troublesome when voltage spikes due to leakage inductances are close to non-existent, but the transformer resonates due to its stray capacitances similarly to those of the transistor, C_{oss}. These recirculating currents not only hinder the efficiency of the converter, but they also make it more difficult to implement the control to detect certain events needed to properly operate in BCM, requiring complex filters to be introduced in the topology.

The transformer resonance in a CPP has been studied in [35], where it is shown that both leakage inductance and stray capacitance play an important role in improving the efficiency of the converter. An empiric rule developed for a well-designed transformer is a leakage inductance at least thousand times lower than the transformer magnetizing inductance. It needs to be taken into account that lowering the parasitic capacitor is in no way as critical as a low leakage inductance. Nevertheless, it should be studied when designing the transformer.

Using planar magnetic technologies is a feasible option, the main advantages of which are the ease of implementation of interleaved windings and the predictability and repeatability of the process [36]. However, in order to attain a low leakage inductance, a large amount of PCB layers is required, rapidly increasing both the complexity and the winding capacitance. Although some techniques to reduce parasitic capacitances in planar transformers have been presented [36] [37], some traditional transformer options will be studied in order to simplify its design.

TABLE I
TRANSFORMER PARASITIC COMPONENTS FOR DIFFERENT IMPLEMENTATIONS

	STRAY CAPACITANCE	LEAKAGE INDUCTANCE
Maximum	100 pF	21 µH
No interleaving	10.99 pF	47.589 µH
Interleaving	20.73 pF	5.498 µH
Foil-based	58.36 pF	0.606 µH
Actual prototype	45.80 pF	3.020 µH



(a)

(b)

Fig. 4. Design of the implemented magnetics. (a) Transformer cross section. (b) Detail of the transformer secondary sub-windings, each color represents a different sub-winding in the same layer.

Based on the previously presented design equations, an 11:1 transformer has been designed aiming for low losses in a relatively wide frequency range around 150 kHz. Its magnetizing inductance is not critical as long as it is much higher than L_{IN1} and L_{IN2}. An EPCOS RM12 – N49 core was chosen, as it is compact and meets design requirements. Several designs were simulated using ANSYS® Maxwell and PExprt. The most noteworthy results are summarized in Table I, where there are shown the maximum parasitic values for the desired transformer design based on the aforementioned empirical rule, the values obtained for three different implementations (i.e., no interleaving, interleaving and foil-based) using Finite Element Analysis (FEA) simulations, and the actual measurements from the constructed interleaved transformer obtained by means of an impedance analyzer. It can be seen that the non-interleaved design does not comply with the desired specifications and the foil-based transformer provides a much lower leakage inductance at the cost of greatly increasing the complexity of assembly. The interleaved transformer can be easily manufactured and meets the desired specifications.

As can be seen in Fig. 4 (a), the winding arrangement is kept rather simple in order to be able to easily assemble and replicate the transformer with regular manufacturing techniques and machinery. The primary winding consists of 8 different sub-windings, each of 66 turns, of AWG 35 copper wire, all connected in parallel.

The secondary winding consists of 6 different sub-windings, each of 6 turns. These are arranged in only two layers, interleaved with the primary, each with three windings. Note that each winding is built from Litz wire comprising 10 AWG 35 wires. Thus, the total thickness is small enough to distribute the windings evenly along the window height, thus reducing the leakage inductance even further. If a single, thicker winding were used on each layer, it would not fit inside the available winding area.

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Different implementation options were also considered for the secondary winding, see Table I. The use of copper foil is an interesting alternative, although the benefit does not justify the increase in manufacturing difficulty, requiring custom foil thicknesses or even laser cutting machinery for fitting the required turns in just one layer. Simulations did not show significant advantages over the preferred simple designs, so this approach was discarded.

As the copper windings do not fill the winding area completely, PET insulating tape layers are added between them. This serves a dual purpose: fixing and insulating the primary and secondary layers, and creating wider spaces between them, thus lowering the stray capacitance.

The design of the input inductors is not as critical as that of the transformer, but a custom design was also used for this prototype. Even though, there is a wide range of commercial inductors that meet the inductance value and frequency requirements with small form factors, they have higher losses. An EPCOS RM8 – N97 core was chosen, with two AWG 29 22-turn windings connected in parallel. The design thus obtained is only slightly bigger than equivalent commercial inductances, but reduces conduction losses by more than half.

III. Control Strategies

Fig. 5, shows a diagram of the control loop of the HB-LED driver in red and the extra winding for the demagnetization path in blue. The current is sensed at the output of the high frequency diode bridge (D_5-D_8) ($i_O(t)$) with the aid of a simple current transformer. The main reason for sensing $i_O(t)$ is that it contains information from both inductor currents reaching the zero value, as well as information on the average output current value by applying a low pass filter to $i_O(t)$ to obtain its average. This means that all the required information for the control is obtained from the same isolated measurement.

By sensing $i_O(t)$ instead of the current in each inductor, as many interleaved boost PFC do, the control needs to be able to discern which switch to trigger. Fig. 6, summarizes the ZCD methodology used to achieve the variable switching frequency control in open loop. Hence, not taking into account the t_{on} variation that would occur due to the closed loop operation that controls the average value of $i_o(t)$. For that reason, the proposed control considers one zero and discards the other. That is, it generates the signal for S_1 and generates the signal to control the other switch (i.e. S_2), see Fig. 6 (b), from the former signal by phase shifting it 180º, taking into consideration the variable T_s, see Fig. 6 (a). This open loop interleaving method is similar to those proposed in the literature based on master-slave techniques [38] [39]. The master is selected at the converter start-up and may be either S_1 or S_2. This switch will not abandon its master status during the entire operation of the HB-LED driver. It is important to note that, once a master is selected, the next zero detection will be discarded, as seen in Fig. 6 (b).

The output of the low pass filter will be the average output current (I_O) scaled by a constant value, α, which will be compared with a reference within the digital control in order to regulate the output current of the driver. Moreover, there needs to be a variable to regulate, which in this case is t_{on}, as well as a

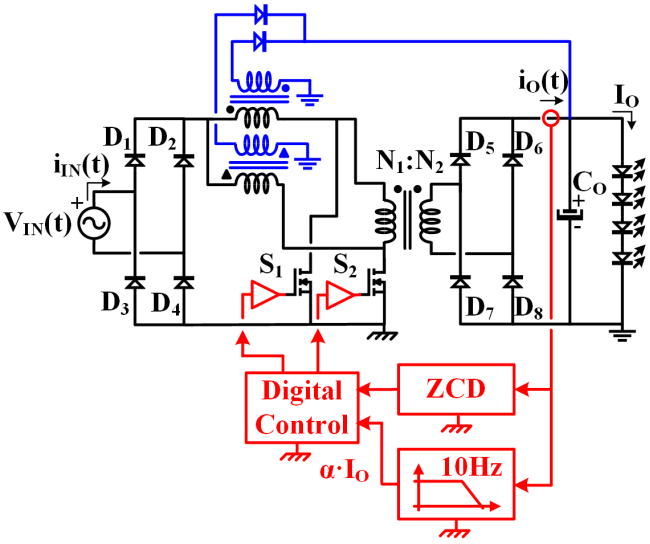
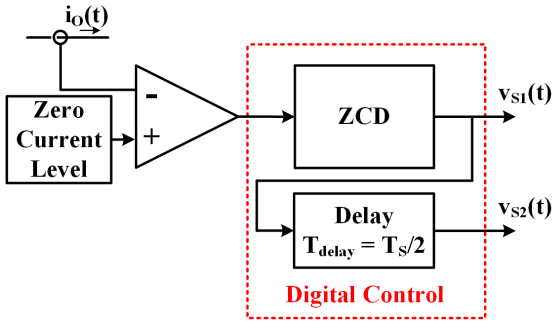
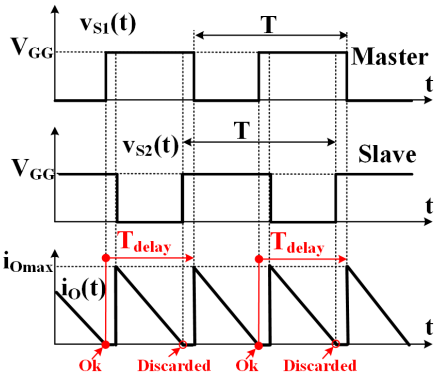


Fig. 5. Scheme of output current closed loop for the DICPP-APFC.



(a)



(b)

Fig. 6. Zero current detection methodology. (a) Basic control circuit. (b) Waveforms used in zero current detection.

transfer function that models the converter in order to design the regulator. In this case, t_{on} will regulate the amount of power the driver demands. The small-signal analysis to obtain the transfer function of the converter is carried out in a similar way to that of an interleaved boost [40], modeling the HB-LEDs as a dynamic resistance (r_{LED}) in series with a voltage source (V_F). Hence, (7) is averaged in a half-line period in order to obtain the average input power:

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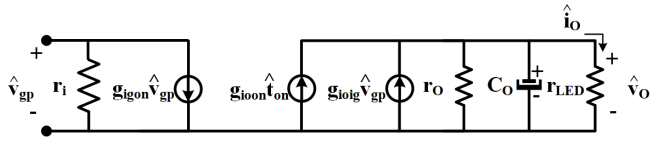

Fig. 7. Equivalent small-signal circuit model of the DICPP, as a PFC.

$$P_g = \frac{v_{gp}^2}{2L} t_{on}, \tag{17}$$

Relating (17) with the average output power, we can thus obtain (18)

$$i_o = \frac{v_{gp}^2}{2Lv_o} t_{on}\,. \tag{18}$$

(18) can be linearized and particularized at a point in order to obtain the small-signal model:

$$\left.\frac{\partial i_o}{\partial t_{on}}\right|_P = \frac{V_{gp}^2}{2LV_o} = g_{ioon}, \tag{19}$$

$$\left.\frac{\partial i_o}{\partial v_{gp}}\right|_P = \frac{V_{gp}}{2LV_o} T_{on} = g_{iogp}, \tag{20}$$

$$\left.\frac{\partial i_o}{\partial v_o}\right|_P = -\frac{V_{gp}^2}{2LV_o^2} T_{on} = -\frac{I_o}{V_o} = \frac{1}{r_o}, \tag{21}$$

where g_{ioon}, g_{iogp} and r_o are depicted in Fig. 7.

In order to complete the small-signal analysis, the input current in a half-line period must be averaged. Thus, from (6) we obtain

$$i_{IN} = \frac{2v_{gp}}{\pi L} t_{on}. \tag{22}$$

After linearizing and particularizing as done previously for the input current, the following relationships are obtained:

$$\left.\frac{\partial i_{IN}}{\partial v_{gp}}\right|_P = \frac{2T_{on}}{\pi L} = \frac{1}{r_i}, \tag{23}$$

$$\left.\frac{\partial i_o}{\partial t_{on}}\right|_P = \frac{2V_{gp}}{\pi L} = g_{igon}. \tag{24}$$

Fig. 7 shows the equivalent small-signal whose transfer function relating i_o and t_{on} can be obtained:

$$\left.\frac{\hat{\imath}_O}{\hat{t}_{on}}\right|_{\hat{v}_{gp}=0} = \frac{\frac{g_{ioon} r_o}{r_{LED}+r_o}}{1+\frac{sC_O r_{LED} r_o}{r_{LED}+r_o}}. \tag{25}$$

After obtaining (25), the compensator can be designed. For this particular case, which is a PFC, the bandwidth of the compensator needs to be sufficiently low to filter the low frequency component of twice the line frequency, that appears at the output due to the pulsating power as has been mentioned before.

IV. Experimental Results

The HB-LED driver introduced in the previous sections has been designed for a maximum power of 100W, the full range of US single-phase line voltage and to feed five strings of 12 HB-LED (W42180T2-SW) with their respective equalizing resistors, which are equivalent to 1.8A/48V at full load. The switching frequency of the HB-LED driver varies from 55 kHz at the lowest line voltage peak to 225 kHz at the zeroes of the maximum line voltage. These frequencies have been selected following the criteria of having a balance between a low frequency that is not audible and a high frequency that does not cause an increase in terms of switching losses. All the selected components for the HB-LED driver are summarized in Table II. Note that the selected MOSFET for the test prototype is a 650V superjunction MOSFET, as it needs to withstand around 450V in the full US range. As for the high frequency diode bridge, it is comprised of 60V/10A fast-recovery Schottky silicon diodes with ultra-low forward voltage. In addition, the digital control of the entire ac-dc HB-LED driver has been implemented in an FPGA due to the simplicity and versatility this platform offers. Nonetheless, an analog control could be also implemented. Fig. 8 shows a picture of the prototype that has been built to validate the analysis carried out in the previous sections. Fig. 9 (a) shows a snapshot of the oscilloscope for an input voltage of 110Vrms/60Hz, measured with no EMI filter to exemplify the low high frequency ripple of the input current operating in BCM. As can be seen, the current follows the input voltage, demonstrating the LFR behavior from the input, which was theoretically obtained, and almost unity PF. Moreover, the input current presents a low switching frequency ripple in spite of having its two inductors operating in BCM. Therefore, the benefit of interleaving the two inductors can be deduced. Fig. 9 (b) shows a zoom of Fig. 9 (a) at the peak of the input voltage. As can be seen, $v_{S1}(t)$

TABLE II
Components of the Experimental Prototype

Fig. 1 reference	Value
D_1-D_4	1N4007
D_5-D_8	FSV1060V
S_1-S_2	IPP65R225C7
FPGA	XC7A100T-1CSG324C
C_O	60V, 2.2mF Electrolytic Capacitor

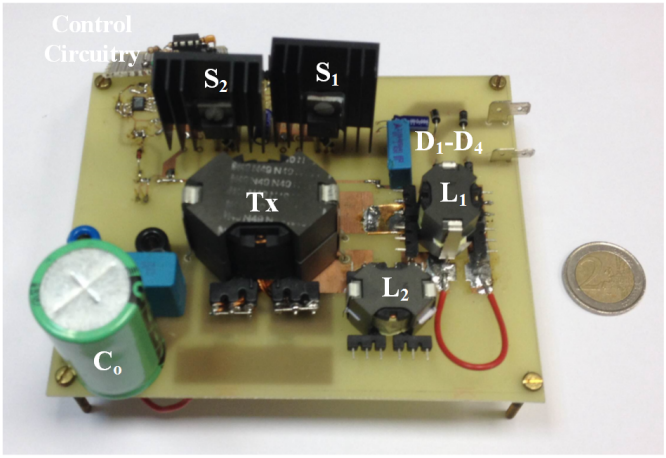

Fig. 8. Experimental prototype of the DICPP-APFC.

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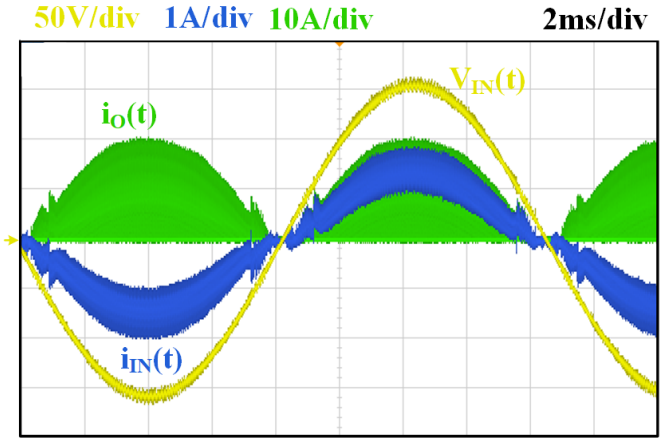
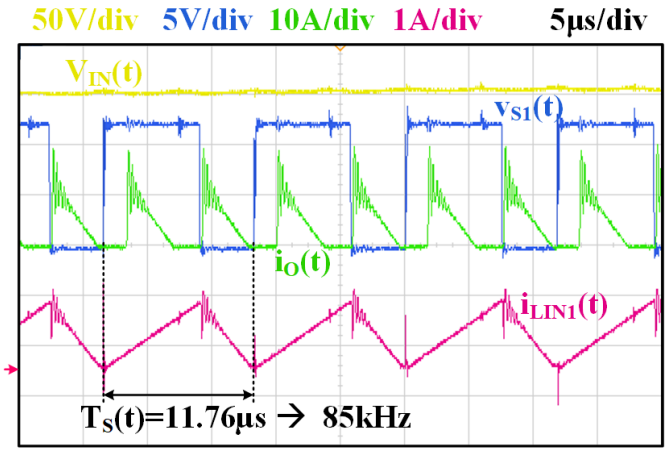
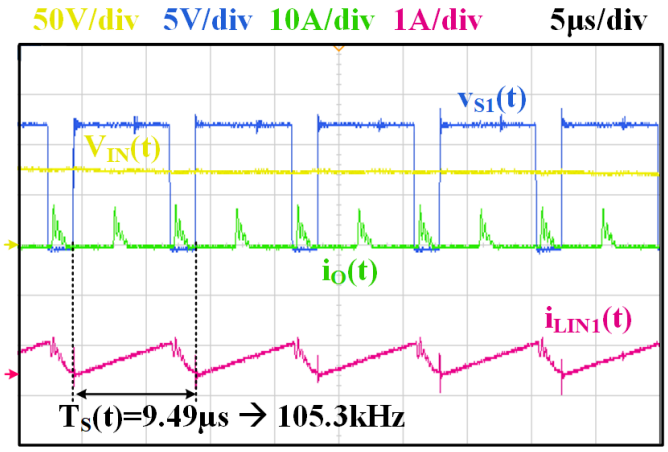


(a)



(b)



(c)

Fig. 9. Experimental input waveforms. (a) Input current and voltage, $i_O(t)$ at 110Vrms. (b) Zoom at the peak of the sine wave. (c) Zoom at a lower input voltage point of the sinusoid.

triggers every two zero crossings of $i_O(t)$ and that they are coincidental to the zeroes of i_{LIN1}. Same can be said for Figure 9 (c) with a higher switching frequency of the control signal, $v_{S1}(t)$, increases by moving to a lower voltage point in the input voltage sine curve. The same is true for $v_{S2}(t)$, demonstrating

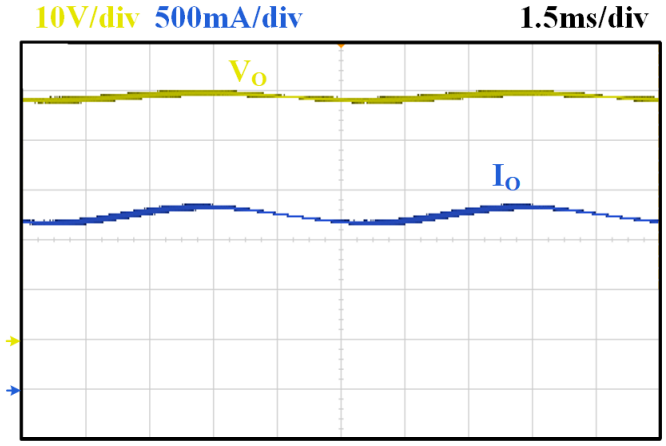


Fig. 10. Output voltage and current at full load.

TABLE III
THD, PF AND EFFICIENCY VS. INPUT VOLTAGE

V_{IN} [V_{RMS}]	THD [%]	PF	EFFICIENCY [%]
80	8.5	0.99	90.6
110	8	0.99	91.9
140	7.5	0.99	93.4

the correct operation of the proposed control. $i_{LIN1}(t)$ can also be seen in these graphs, illustrating that one of the inductors is operating in BCM, as intended. The other inductor is also working in BCM, although it is not shown in the graphs, but can be deduced to be working in BCM by observing $i_o(t)$.

Fig. 10 shows a snapshot of both the output voltage and current with the required electrolytic capacitor to reduce the output current ripple due to the well-known effect of pulsating power in PFC.

In order to validate the correct operation of the HB-LED driver, several waveforms were obtained, under different conditions, from the oscilloscope as data and processed with MATLAB® to properly analyze them. The parameters obtained from said waveforms were: efficiency, THD, PF, and compliance with Class C IEC 1000-3-2 [2]-[4].

The efficiency, THD and PF of the HB-LED driver are shown in Table III as a variation of the line voltage. For the nominal conditions presented in Figure 9 (a), the efficiency is around 92%, the THD is about 8% and the PF is 0.99, all of which comply with the Energy Star® regulation [1]. Note that the efficiency at full load does not fall below 90% even for the worst case scenario.

Fig. 11 shows the efficiency in dimming conditions for the nominal input voltage (110 V_{rms}). As can be seen, the efficiency of the HB-LED driver stays above 90% from full load to half load. At low output current, however, the converter suffers a drop in efficiency.

Fig. 12, shows a prediction of the losses distributed in the components of the experimental prototype studied in this section. The magnetic components present more than 50% of the losses of the converter and have been estimated using Finite Element Analysis (FEA) via ANSYS® Electromagnetics Suite. The losses in the MOSFETs present a 16% of the total losses

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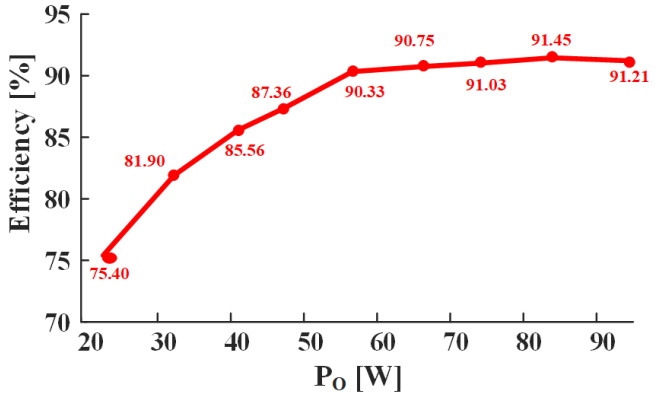

Fig. 11. Efficiency at 110 Vrms versus output power.

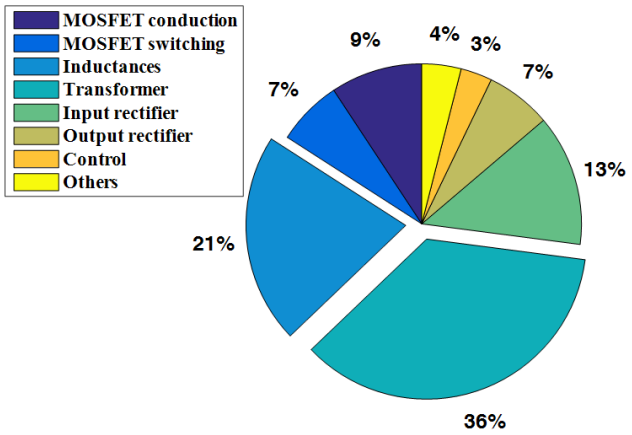

Fig. 12. Distribution of losses in the experimental prototype of the DICPP-APFC under nominal conditions.

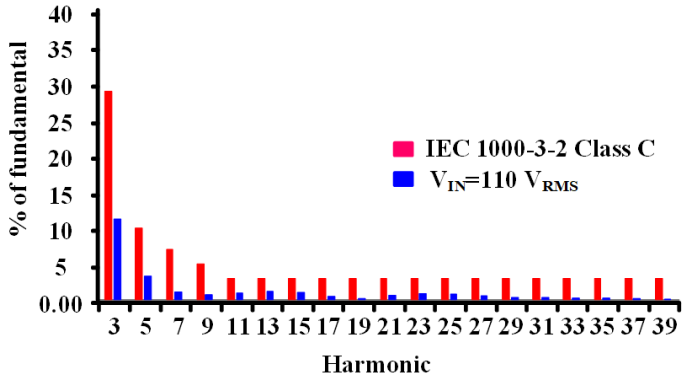

Fig. 13. Harmonic content of the input current for the topology under study and compliance with Class C.

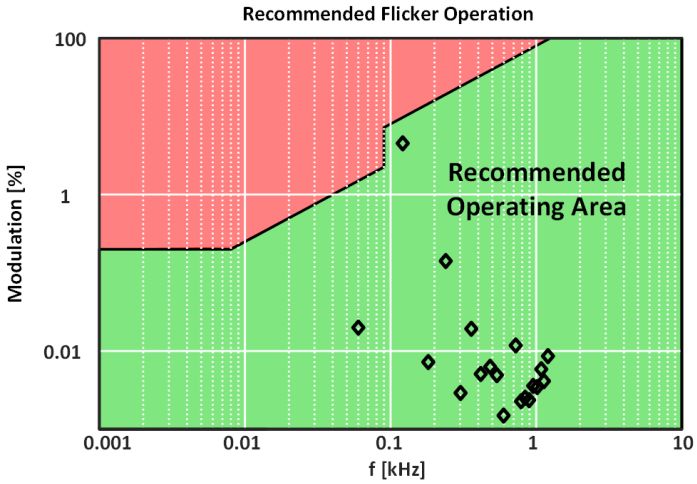

Fig. 14. Recommended flicker operation at full load for both drivers, P1789 [31].

and have been estimated using an analytical model for superjunction MOSFETs [41].

The input waveforms were also used to extract the harmonics using the Fourier series. These measurements were then compared with Class C IEC 1000-3-2 harmonic limits. As can be seen in Fig. 13, the HB-LED driver complies with the regulation.

To limit the biological effects and detection of flicker in general illumination, the Modulation (%) should be kept within the shaded region defined in [31], [32], where the Modulation (%) calculation can be defined as follows:

$$Modulation\ (\%) = 100 \cdot \frac{(L_{max} - L_{min})}{(L_{max} + L_{min} + L_{DC})}, \quad (26)$$

where L_{max} and L_{min} correspond to the maximum and minimum luminance of each harmonic of the ac component of the light output respectively, and L_{DC} corresponds to the average of the light output.

The luminance of the HB-LEDs was measured for the driver under study by using a transimpedance amplifier (TSL-257) with a bandwidth of 10 kHz to measure the light output waveform. After obtaining the luminance waveform, all the harmonics were obtained from 60Hz (the frequency of the fundamental harmonic) to 3 kHz and compared with the standard, see Fig. 14, by means of applying the Fourier series to luminance waveform. As can be seen, all the harmonic content falls within the shaded region, even in those frequencies below 90Hz, which are the ones humans are more sensitive to. Therefore, good light quality and non-harmful effects can be assumed from the proposed HB-LED driver topology.

Table IV, shows a brief comparison of the experimental prototype studied in this work with state of the art, single-stage, ac-dc, LED drivers, in which several important parameters are compared, such as, output power, efficiency, THD, etc. As can be seen, the DICPP-APFC shows an outstanding performance with its biggest disavantage being the size of the output capacitor. This is the price to pay to achieve good light quality in this AC-DC single stage. In this respect, an active filter [7] [8] or a high efficiency post-regulator stage [43]- [45], to diminish the low frequency component and thus can be used to remove the bulk capacitor and control each HB-LED string individually. However, this is at the cost of adding more components and increasing the complexity of the DICPP-APFC.

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TABLE IV
COMPARISON OF STATE OF THE ART SINGLE-STAGE AC-DC LED DRIVERS

		REFERENCES				
	DICPP-APFC	[7]	[13]	[46]	[47]	[48]
Output Power [W]	100	35	35	81	100	12
Efficiency [%]	91.5	87	90.5	90.69	91.7	86.1
THD [%]	8	-	-	3.32	5.7	-
Switching frequency [kHz]	55-225	-	140	67	90	100
Output capacitor [μF]	2200	470	4.7	-	220	2
Output current ripple [%]	10	10	20	20	10	17.85
Output capacitor reduction	No	Yes	Yes	No	Yes	Yes
Reduced input cur. ripple	Yes	No	No	Yes	No	No
Number of MOSFETs	2	3	3	2	2	1
Number of transformers	1	1	1	2	1	1
Number of inductances	2	1	2	0	3	1

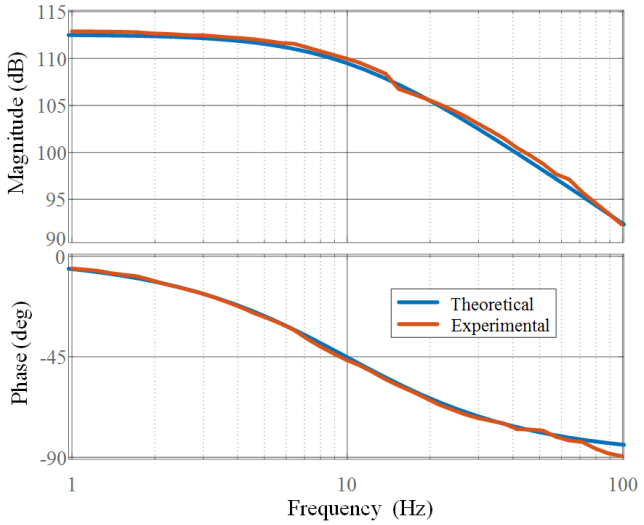

Fig. 15. Comparison of the theoretical and experimental measurements of the t_{on} to i_o transfer function (25).

TABLE V
VALUES USED TO OBTAIN THE THEORETICAL WAVEFORM OF (25)

	VALUE
V_{gp}	110 Vrms
L	860 μH
T_{on}	7.1 μs
C_o	2.2 mF
r_{LED}	5.5 Ω
V_o	48 V

All the results that have been shown in this section, have been measured in closed loop by controlling the output current of the HB-LED driver and allowing t_{on} to vary. In order to design the compensator, the open loop response of the converter relating the output current of the DICPP- APFC to variations of t_{on} has been measured by using a Venable® 6320. This response is represented in Fig. 15 and compared with its theoretical counterpart (25), showing that the theoretical analysis matches the experimental results. The values used to obtain the theoretical curve of (25) are calculated by using the design criteria introduced in Section II and are summarized in Table V. Considering the results shown in Fig. 15, the compensator design is straightforward and is extremely similar to any other PFC output loop, which can be accomplished with a simple PI [17].

IV. CONCLUSIONS

A simple, current-fed, ac-dc, single-stage, single-phase, isolated, high PF, HB-LED driver with two switches referenced to the same ground has been reported and experimentally tested in this paper. The DICPP-APFC is able to deal with most of the issues that made current-fed AC-DC converters not suitable for power factor correction: switches withstanding high voltage, complex transformer design and low performance at low power. Moreover, the advantages of using the DICPP-APFC against some of the conventional single-stage topologies, from Table IV, are that is able to achieve high efficiency and reduce the traditional switching frequency ripple of BCM operation with a single transformer, by using the inbuilt interleaving method between the two branches that comprise the push-pull topology, at the price of including one more magnetic component and one more active switch. It should be noted that, the adding of more branches is not scalable, hence it is not a possibility to reduce even more the input ripple with a single converter. However, the DICPP-APFC does come with some drawbacks: the first drawback comes from the need to use a demagnetization circuit to prevent the switches from destruction in case of a control failure, which is intrinsic to current-fed topologies, the second one comes from the inability to dispose of the bulk capacitor present in single-stage ac-dc converters which require a high PF and the third drawback is related to the voltages stress that the switches are withstanding, which at this point makes this topology not suitable to achieve universal input voltage range with silicon technology. In fact, not being able to dispose of the electrolytic capacitor may be troublesome for some LED drivers that require long lifespans. However, this is the price to pay for a simple, cost efficient, ac-dc single-stage solution at these power levels.

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