Distributed Control Alternatives of Modular Power Converters for Hybrid DC/AC Microgrids

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***Abstract*—This paper proposes a distributed control alternative for modular power converters. The focus is on the use of single-phase power units with embedded control capabilities, namely intelligent Power Electronics Building Block (iPEBB) for power conversion in hybrid DC/AC microgrids. The distributed control is achieved by the use of a versatile controller inside each iPEBB, so that they can operate independently by controlling their own voltage(s)/current(s). For the management of the entire system, a central controller is integrated into the control scheme. The central controller is in charge of the application-level control of the modular power converter, so that it determines the role of each iPEBB and commands the references to achieve the control goals. As a demonstration of the proposed approach, the control of a 4-wire 4-leg STATCOM using 4 independent power units is shown in this paper. For the implementation of the iPEBB control system, two different approaches are evaluated: Proportional-Resonant (PR) and Repetitive Control (RC) alternatives. Analysis is done using direct discrete design. Different simulations as well as experimental results are performed in order to validate the proposed system. The study considers communication delays between the central controller and the iPEBB as well as internal reconstruction of the reference from the central controller command.**

I. Introduction

Nowadays, the penetration of renewable energy generation is encouraging an evolution towards distributed generation systems, with the appearance of local small-scale power systems known as microgrids [1]. Microgrids opt for implementing hybrid generation using batteries, supercapacitors and flywheels [2], [3] to have a flexible and reliable operation. The increasing requirements regarding the number of switches, the switching frequency and the communication needs are driving the change of the control systems, moving from the central DSP/DSC based architecture to decentralized architectures [4]. The benefits of this approach can be summarized as: 1) scalability in terms of the needed inputs (A/D) and outputs (PWM), 2) flexibility and 3) reliability. However, there are some drawbacks that make the implementation more difficult than the one based on a central controller. In particular, the need of synchronization and communications as well as a change in the control design.

In order to accomplish a modular power converter, different proposals can be found in the literature using basic power cells [4], [5] to interface with the power system. This power cell is known as Power Electronics Building Block (PEBB) [5] and has to be controlled according to the desired power converter topology. Therefore, a distributed control system has to be developed in order to achieve a proper behavior of the modular power converter. This control consists of an individual autonomous control for each of the power blocks (inner current and voltage control loops), and a central controller to coordinate all the power blocks and provide a specific function to the whole power converter (application-level control loops).

In a generic application-agnostic approach, the inner control loop of each power cell has to be capable of tracking references and rejecting disturbances of different polynomial order. In this paper, the analysis is restricted to AC/DC and DC/AC power conversion, in which references and disturbances are expected at the fundamental harmonic frequency and its multiples. Based on the internal mode principle [6], the controllers need an internal harmonic generator model to properly manage harmonic references/disturbances. In this way, a theoretical zero steady-state error is achieved at the harmonic frequencies. Control techniques which meet this requirement are Proportional-Resonant (PR) controllers [7]–[9] and Repetitive Controllers (RC) [10]–[12].

The outer control loop of the central controller shall provide the control goals, i.e. references to the PEBB and receive the feedback signals for the control of the complete power converter through a communication channel, which implies the appearance of pure delays. The impact on the performance of these intrinsic pure delays have to be considered during the control system design.

The objective of this paper is to tackle the control issues for the system explained above. The studied case will be a 4-wire 4-leg grid-tied inverter. Particular emphasis will be placed in the reference tracking and disturbance rejection of fundamental and non-fundamental harmonics. The behavior under changes in the fundamental frequency will be analyzed. Communication delays will also be taken into account.

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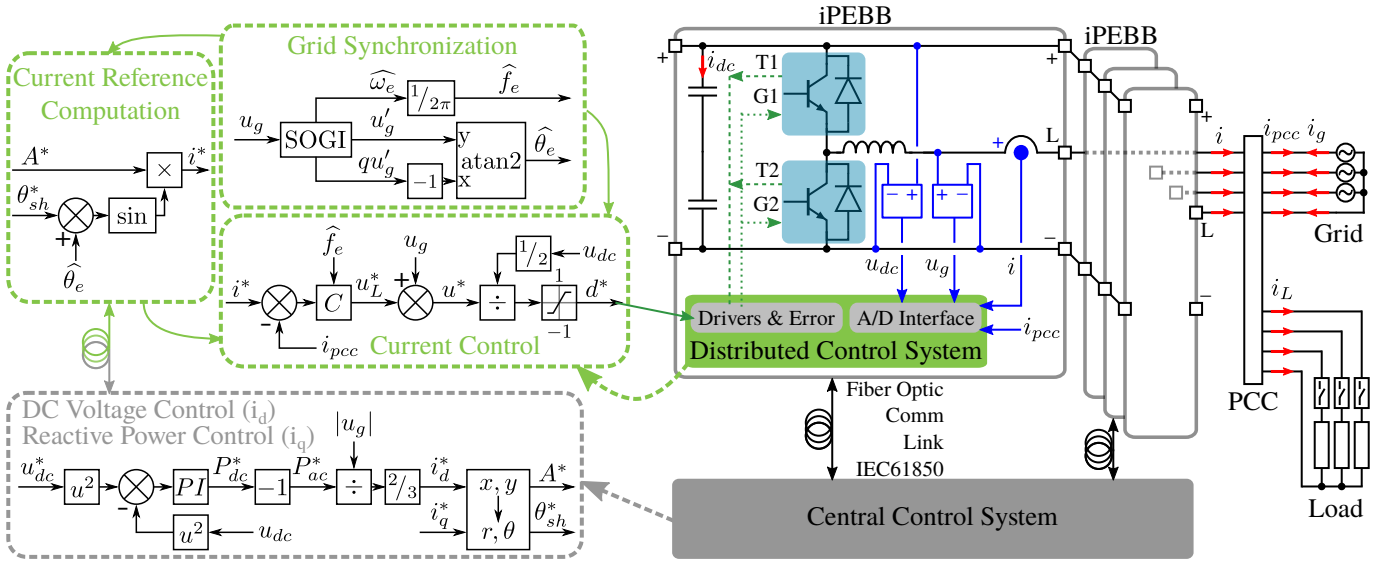

Fig. 1. Proposed architecture for a modular power converter based on iPEBB. The application is for a 4-wire 4-leg STATCOM connected to the grid.

This paper is organized as follows. In Section II, an explanation of the proposed system architecture is addressed. In Section III, an analysis of the different control alternatives suited for managing periodic signals is discussed. In Section IV, several control issues related to the studied case are analyzed. In Section V and Section VI, simulation and experimental results are obtained in order to validate the proposed system. Finally, in Section VII, conclusions about the accomplished work are discussed.

II. System Architecture

The proposed solution consists of several single-phase power cells (upper and lower power switches, parallel capacitor, and series inductor in mid-point) with built-in voltage and current sensors, and a digital control system which manages the power cell; thus creating an intelligent PEBB (iPEBB). On top of them, a central controller, based on a generic microprocessor with real-time capabilities and a fast communication channel, coordinates all the system.

The iPEBBs provide the interface with the global power system and hence their objective is to measure the electric variables (voltages and currents) and give the switching command to the drivers turning on/off the switches according to the desired control action. The central controller determines the application of the whole system by sending messages to the power cells with information about the operating point. An schematic of the proposed architecture for the power converter is shown in Fig. 1. Integration with the system operator, even if not analyzed in the present paper, is proposed to be implemented using the IEC61850 standard.

In order to validate the proposed architecture, the modular converter will behave as a 4-wire 4-leg STATCOM connected to the grid. Therefore, the main objective of the test application is to compensate reactive power and mitigate unbalances and harmonics produced by the connection of local loads, so that the current at the PCC is balanced and does not contain any non-fundamental harmonics. Four iPEBBs are used to carry out the current control of the three active phases and the neutral phase (homopolar injection), whereas the central controller is in charge of the DC link voltage control (i_d^*) and the reactive power compensation (i_q^*). The DC link voltage control uses a quadratic implementation to obtain directly the required power as control action.

The central controller sends messages with references of current magnitude (A^*) and phase shift (θ_{sh}^*) to the iPEBBs in charge of the active phases. Note that the homopolar current controller (neutral phase) does not receive any references from the central controller since its reference is zero (local control).

Since the system is connected to the grid and is working with resonant single-phase controllers, a SOGI is implemented for each iPEBB to carry out the grid synchronization. This way, each iPEBB is capable of estimating the grid frequency ($\widehat{f}_e$) and the grid voltage phase ($\widehat{\theta}_e$), and thus it can tune properly its resonant controller (C) and compute the current reference (i^*).

Note that the current control has to manage currents at the fundamental grid frequency and corresponding harmonics, so the selection of the single-phase controller (C) topology is not straightforward. An analysis of the different control alternatives is going to be done in the next section.

III. Analysis of Control Alternatives

The control of single-phase signals at a nominal frequency and multiples is analyzed in this section. The analysis is focused on the study of resonant controllers, particularly the proportional-resonant (PR) controller and the repetitive controller (RC).

A. Proportional-resonant controller

1) Continuous domain: The PR controller is a generalization of a proportional-integral (PI) controller centered at an

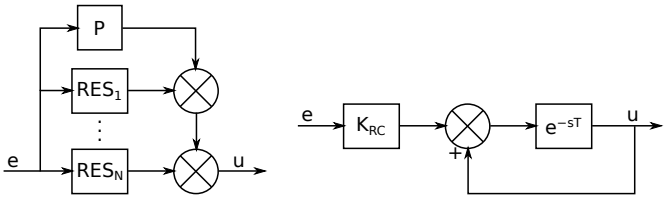

Fig. 2. Proportional-resonant (a) and repetitive (b) controller.

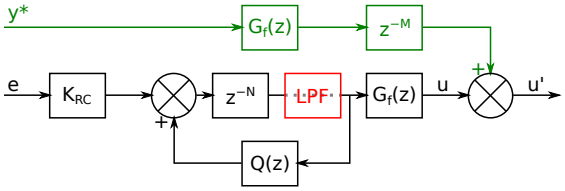

Fig. 3. Direct repetitive controller with feed-forward term (green path) and optional low-pass filter in direct path (red block).

arbitrary frequency. The PI controller is capable of achieve zero steady-state error for DC references (0Hz) whereas the PR controller has to be capable of achieve zero steady-state error at the central frequency. The continuous transfer function of the PR controller is given by [7].

The implementation of a PR controller in discrete domain can be achieved both by discretization methods (often Tustin with pre-warping is used) or by direct-discrete design techniques. The first approach is easier to implement, but tracking of higher harmonics becomes difficult if the sample-time delay is not considered. In this paper, direct-discrete design is used in order to extend the controller capabilities.

2) Discrete domain: The derivation of the PR controller in discrete domain is obtained from the discrete PI expression shown at (1).

$$C_{PI}(z) = C_P(z) + C_I(z) = K_p + \frac{K_i T_s}{z-1} \tag{1}$$

Applying the same derivation as in [7] to (1) as shown in (2), the discrete PR controller is obtained. This PR controller has infinite gain at the resonance frequency (ω), and thus zero steady-state error at that frequency. When considering multiple harmonics, the expressions in (3) and (4) are obtained, which is related to the block diagram shown in Fig. 2a.

$$C_{RES}(z) = C_{PI}(ze^{+j\omega T_s}) + C_{PI}(ze^{-j\omega T_s}) \tag{2}$$

$$C_{PR}(z) = C_P(z) + \sum C_{RES}(z) \tag{3}$$

$$C_{PR}(z) = K_p + \sum_{h\in\mathbb{Z}^*} \frac{2K_{ih}T_s\left[\cos(h\omega T_s)z - 1\right]}{z^2 - 2\cos(h\omega T_s)z + 1} \tag{4}$$

As it can be observed, the coefficients of the PR controller have to be calculated using the fundamental frequency of the system, and the number of resonant controllers in parallel depends on the number of harmonics which is going to be taken into account. This makes this multiple-parallel-connected PR approach tedious to implement [9].

B. Repetitive controller

1) Continuous domain: The RC is mainly based on the concept that it is possible to generate a periodic signal with a fixed period by means of a system with a pure time delay equal to the signal period (T) and a unitary positive feedback around this delay [10]. Applying the internal model principle [6], it is possible to design a controller capable of tracking a periodic variable by including the model inside its scheme. The resultant controller is shown in (5) and Fig. 2b.

$$C_{RC}(s) = K_{RC}\frac{e^{-sT}}{1-e^{-sT}} \tag{5}$$

The implementation of the RC into a digital control system is straightforward since the pure time delay is transformed into a number of control periods delay depending on the sampling frequency.

2) Discrete domain: As stated before, the RC digital implementation offers simplicity as a main advantage. Nevertheless, the stability of this controller is compromised since the RC introduces a unitary positive feedback. Therefore, the final scheme of the RC has to be tweaked a little bit. The presented discrete RC is known as direct repetitive controller (DRC) [11], [12]. The delay is now determined by an integer number of samples (N) and its expression is shown at (6) and Fig. 3.

$$C_{DRC}(s) = K_{RC}\frac{z^{-N}}{1-Q(z)z^{-N}}G_f(z) \tag{6}$$

Compared to Fig. 2b, in Fig. 3 there are two additional blocks, the robustness filter $Q(z)$ and the stability filter $G_f(z)$. The robustness filter is used to avoid a perfect positive feedback which could lead to an unstable system. There are several options for the robustness filter: constant value slightly lower than one, low-pass filter, moving average filter, etc. The stability filter is computed in order to achieve a zero-phase-shift (ZPS) compensator [12], so that the dynamics of the power converter filter are compensated and its influence is attenuated: $G_f(z) = \hat{G}_{OL}^{-1}(z)$.

Compared to the multiple-parallel-connected PR, the DRC is easier to implement since it provides an infinite number of resonances at multiples of the fundamental frequency without need of parallelization. However, this behavior implies that the repetitive controller reacts to high-frequency harmonics, which can lead to an unstable behavior due to high-frequency noise. In order to avoid this behavior, two different topologies are accounted: 1) Robustness filter $Q(z)$ with constant value slightly lower than one and without low-pass-filter (LPF) $\Rightarrow$ DRC; 2) $Q(z) = 1$ and low-pass filter (LPF) after the pure delay z^{-N} (Fig. 3 with red block) $\Rightarrow$ DRC_LPF.

Additionally, the RC has a drawback in the form of one fundamental period delay in order to track references (learning period). In order to reduce this effect, a feed-forward component of the reference through the block $G_f(z)$ is added to the action control of the controller as shown in Fig. 3 [13]. Note

that $G_f(z)$ is not a proper system in this case, so an additional pure delay (z^{-M}) is included in the feed-forward path to make the resultant system biproper.

The iPEBBs of the modular converter are not computationally very powerful, so that the control topology is focused on the use of repetitive controllers to reduce the complexity of the computations as stated in Subsection III-A. In particular, the DRC with LPF will be used to limit the bandwidth of the system.

IV. Control issues

The modular implementation approach used in this paper, together with the use of resonant controllers for the current control loop, implies the appeareance of some control issues, which are discussed hereunder: frequency shifts, communication channel and reference reconstruction.

A. Frequency shifts

The main problem of resonant controllers appears when the fundamental frequency is shifted with regard to the nominal frequency. In order to solve this problem, an adaptive frequency-dependent version of the resonant controllers has to be implemented.

Similarly, operation under variable frequency for the DRC case requires to adapt the delay value, as it depends on the ratio between the sampling frequency and the fundamental frequency. However, an integer relationship has to be kept according to the controller expression. Therefore, variations of the fundamental frequency cannot be fully compensated in a first approach (non-integer ratio). There are two options to solve this problem: 1) modifying the sampling frequency to achieve an integer delay or 2) implementing a fractional delay (z^{-F}) computation. The chosen option is the second one since the first would increase the complexity and the cost of the system. It is possible to halve the minimum delay of the controller as stated in [14] ($\omega_1 = 2$ and $\omega_2 = -1$ for even and odd harmonic compensation) but a better solution is addressed in [15], which is capable of compensating any kind of fractional delay by using a Lagrange-interpolating-polynomial-based fractional delay filter. A cubic interpolating polynomial is used: $z^{-F} \approx H_0 + H_1 z^{-1} + H_2 z^{-2} + H_3 z^{-3}$. The z^{-F} estimation block is placed just after the integer delay block (z^{-N}).

In this way, under frequency shifts, the integer part of the new ratio between sampling frequency and fundamental frequency will be considered by shifting the coefficients of the DRC (pure delay variation) whereas the non-integer part will be considered by changing the coefficients of the fractional delay filter.

B. Communication channel

A communication channel is required in order to connect the central controller and the power cells. This implies an additional problem in comparison to conventional control schemes, which is the appearance of stochastic pure delays between the outer and the inner control loop. In the analyzed case, the central controller sends references to the power cells (current magnitude and phase shift) and receives measurements from them (DC link voltage). In order to reduce the cost and the complexity of the system, a common communication channel is used for the entire system. Two operation modes are considered in relation to the communication channel:

- Asynchronous mode. Each power cell updates the reference value and the central controller updates the corresponding measurement asynchronously once the communication is carried out. Accumulative delays take place between power cell variables, so that virtual unbalances appear.
- Synchronous mode. A synchronization message is added to the communication protocol in order to synchronize the different elements of the system. In this case, the synchronization message is sent after all the references/measurements sequence. Only after this message, the elements of the system update their references/measurements, so that the accumulative delay effect disappears.

In this paper, the asynchronous mode is considered in order to avoid the need of synchronization among the different cells. This operation mode will be analyzed, and its effect over the error of the generated current will be considered as the figure of merit.

C. Reference reconstruction

The central controller is in charge of sending references to the individual iPEBBs. Since the control loop frequency of the power cells is higher than the control loop frequency of the central controller (a ratio of 10 for this research), the iPEBBs have a constant value for the reference between external loop iterations, thus leading to step-wise reference changes that cause additional distortion in the system, as shown in Fig. 4 (Initial Case).

To mitigate this problem, a linear extrapolation process at the iPEBB is proposed in this research in order to obtain a reference with a smoother shape for the intermediate iterations of the distributed current control with regard to the centralized voltage control, as shown in Fig. 5. The numerical expression is shown in (7).

$$x_k = \frac{x_{k'} - x_{(k-1)'}}{k_0 - k_{-1}} (k - k_0) + x_{k'} \tag{7}$$

After applying the linear extrapolation to the received reference, the results shown in Fig.4 (Reconstructed Ref. Case) are obtained. As can be seen, the spikes in the converter voltage because of sharp reference changes are mitigated, and thus the converter current is smoother. Note that, the extrapolation used in this case is linear but higher order extrapolation algorithms can be used in order to improve slightly the performance.

This algorithm is applied in the iPEBB to the magnitude reference (A^*) but not to the phase shift (θ^*_{sh}) in order to avoid an overcorrection of the whole reference.

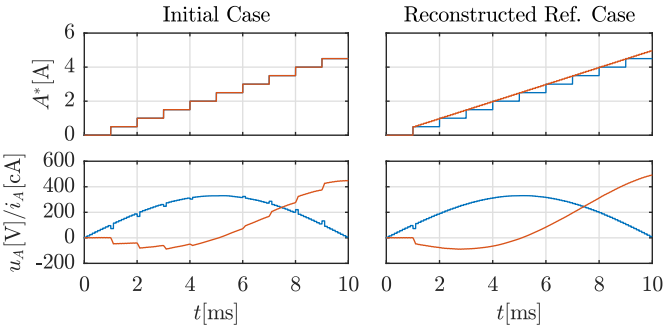

Fig. 4. Comparison between the initial case (left figures) and the reconstructed reference case (right figures) for one phase of the converter. Top figures: blue, reference sent by the central controller; orange, reference built by the single-phase controller via extrapolation. Bottom figures: blue, converter voltage; orange, converter current.

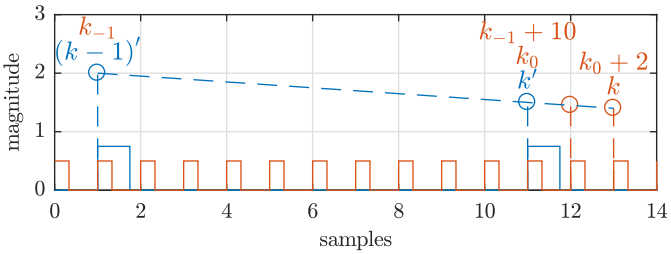

Fig. 5. Graphical representation of the linear extrapolation process used to generate a smooth reference for the intermediate iterations of the distributed current control. Circular marks represent the samples of the control loops and square signals represent the control loop periods. Blue variables are related to the centralized voltage control whereas orange variables are related to the distributed current control.

TABLE I
SYSTEM PARAMETERS.

Parameter	Value
Active phase filter inductance (L)	7 mH
Active phase filter resistance (R)	0.3 Ω
Neutral phase filter inductance (L_n)	3 mH
Neutral phase filter resistance (R_n)	0.06 Ω
DC link total capacitance (C_{dc})	5.04 mF
Nominal DC link voltage (U_{dc})	750 V
Sampling/PWM frequency	10 kHz
Current (iPEBB) control loop frequency	10 kHz
DC link voltage (central) control loop frequency	1 kHz
Nominal grid line RMS voltage	400 V
Nominal grid frequency	50 Hz

V. SIMULATION RESULTS

The simulation results are based on the system architecture shown in Fig. 1. The parameters are detailed in Table I.

In order to determine the system performance, four different tests will be conducted: 1) Reactive power management and frequency shifts, 2) Connection of local linear loads, 3) Connection of local non-linear loads, and 4) Error from communication delays. The complete simulation profile is shown in Fig. 6. For the subsequent analysis, the three-phase variables will be shown in a theoretical synchronous reference frame (dq0) in order to ease the understanding of the results.

As shown in Fig. 6, different operating conditions are

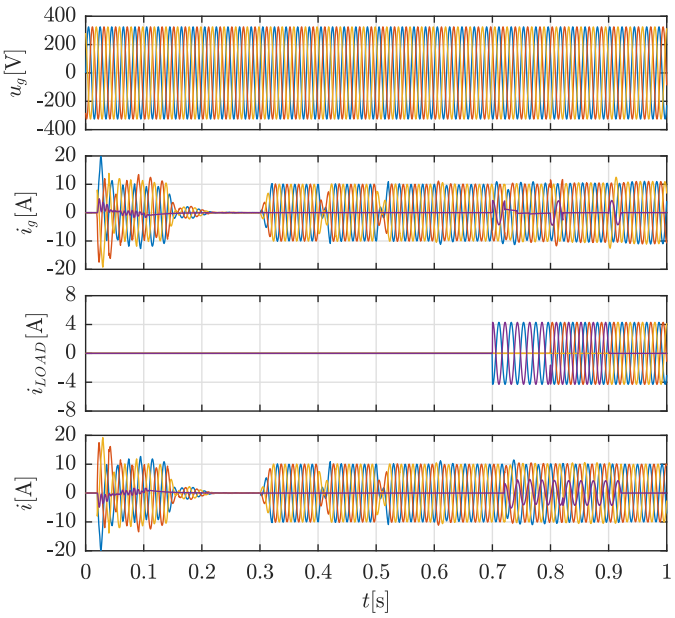

Fig. 6. Global simulation results. Variables are shown in phase coordinates (abcn): blue, phase A; red, phase B; orange, phase C; purple, phase N. 1) Grid voltage, 2) Grid current, 3) Load current, 4) Converter current.

evaluated: 1) At 0.02 s, the control is enabled; 2) From 0.3 s to 0.32 s, the reactive current reference (i_q^*) is changed from 0 A to −10 A by using a ramp; 3) From 0.4 s to 0.42 s, the reference is changed from −10 A to +10 A by using a ramp; 4) From 0.5 s to 0.52 s, the reference is changed from +10 A to −10 A by using a ramp; 5) At 0.6 s, the grid frequency is changed from 50 Hz to 47.2 Hz; 6) At 0.7 s, a resistive load of 700 W is connected between phase A and neutral phase; 7) At 0.8 s, a resistive load of 700 W is connected between phase B and neutral phase; 8) At 0.9 s, a resistive load of 700 W is connected between phase C and neutral phase.

A. Reactive power management and frequency shifts

The initial test consists in managing the reactive power which is injected/consumed into/from the grid by following the reference profile which was previously defined.

The results are shown in Fig. 7, Fig. 8 and Fig. 9. As can be seen, the DC link voltage reaches its nominal value at 0.3 s, which is maintained almost constant under changes in the reactive current. In addition, the reactive current management is properly done since the actual current follows the reference quickly and without steady-state error.

In addition, the grid frequency change is properly compensated in about 2 fundamental periods (40 ms). Note that, a huge step change in the grid frequency is tested (50 Hz to 47.2 Hz) whereas the grid frequency variations are much slower in a real application. The selection of the simulation final frequency value is not arbitrary, since it gives (10000/47.2) an integer delay of 211 samples and a fractional delay of 0.8644. This way, the fractional delay is quite high and its compensation is also tested.

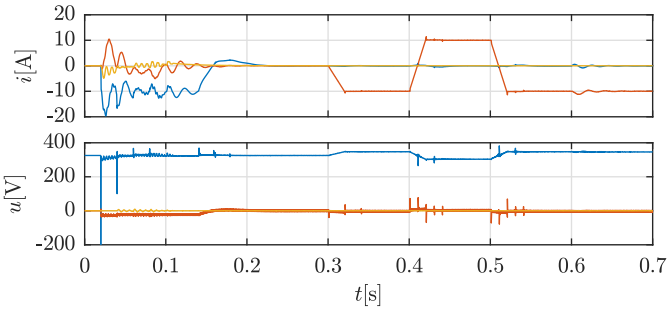

Fig. 7. Simulation results for reactive power management. Variables are shown in a theoretical synchronous reference frame (dq0): blue, d-axis; red, q-axis; orange, 0-axis. Top, converter current in synchronous reference frame. Bottom, current controller control action in synchronous reference frame.

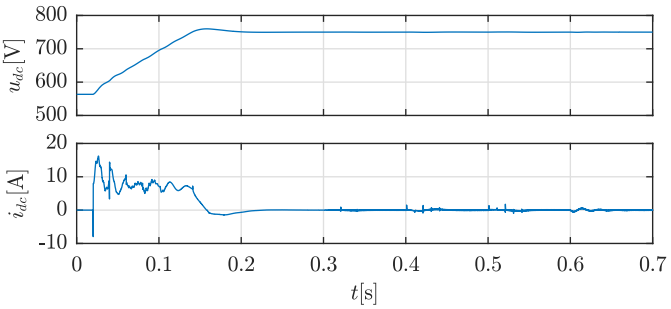

Fig. 8. Simulation results for reactive power management. Top, converter DC link voltage. Bottom, converter total DC link current.

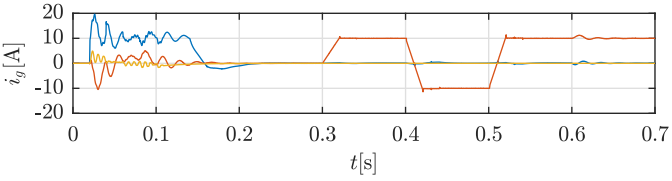

Fig. 9. Simulation results for reactive power management. Grid current in a theoretical synchronous reference frame (dq0): blue, d-axis; red, q-axis; orange, 0-axis.

B. Connection of local linear loads

Disturbance rejection capabilities are demonstrated with a set of single-phase linear loads which are connected to the grid at different times. With the proposed control scheme, both negative sequence and homopolar currents are supplied by the converter, making the grid isolated from the disturbances in steady state, only supplying balanced currents.

The results of this test are shown in Fig. 10 and Fig. 11. As can be seen, the converter reacts to the local load connection after one fundamental period (20 ms) due to the inherent learning period of the repetitive controller. Note that the feed-forward term is only applied to the current reference and a disturbance is introduced into the system in this case. Nevertheless, the unbalances are compensated in steady state by the converter by injecting negative sequence and homopolar current into the local grid. The main grid only supplies the needed balanced power.

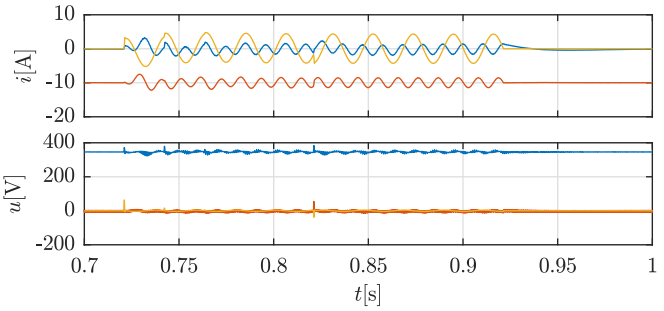

Fig. 10. Simulation results for local linear load connection. Variables are shown in a theoretical synchronous reference frame (dq0): blue, d-axis; red, q-axis; orange, 0-axis. Top, converter current in synchronous reference frame. Bottom, current controller control action in synchronous reference frame.

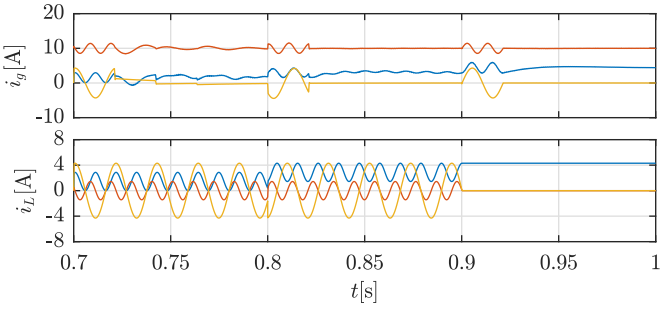

Fig. 11. Simulation results for local linear load connection. Variables are shown in a theoretical synchronous reference frame (dq0): blue, d-axis; red, q-axis; orange, 0-axis. Top, grid current in synchronous reference frame. Bottom, load current in synchronous reference frame.

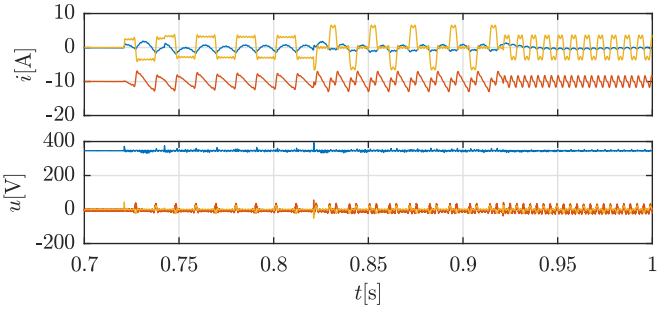

Fig. 12. Simulation results for local non-linear load connection. Variables are shown in a theoretical synchronous reference frame (dq0): blue, d-axis; red, q-axis; orange, 0-axis. Top, converter current in synchronous reference frame. Bottom, current controller control action in synchronous reference frame.

C. Connection of local non-linear loads

In order to see the disturbance rejection against non-fundamental harmonics, a set of non-linear loads is now connected instead of the linear loads of Subsection V-B. The non-linear loads absorb a power equivalent to the linear loads (same RMS current) but the current shape is now almost square (full-wave rectifier connected to an inductive load).

The results of this test are shown in Fig. 12 and Fig. 13. Similar performance when compared to the linear load case is obtained. The harmonics are absorbed by the power converter in steady state with a transient response lasting 20 ms.

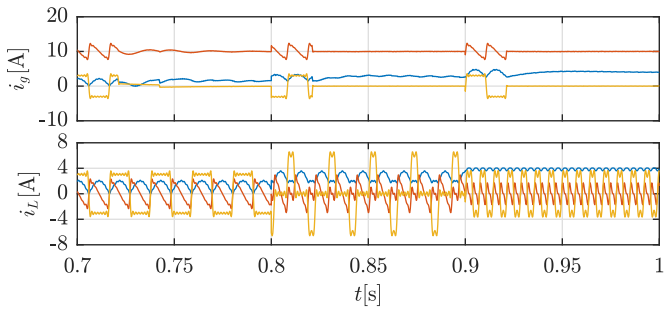

Fig. 13. Simulation results for local non-linear load connection. Variables are shown in a theoretical synchronous reference frame (dq0): blue, d-axis; red, q-axis; orange, 0-axis. Top, grid current in synchronous reference frame. Bottom, load current in synchronous reference frame.

D. Error from communication delays

As stated in Subsection IV-B, communication delays can affect the error of the resultant current since the output current reference is affected by the delay in the communication channel. Several cases are analyzed in order to detail the effect of this phenomenon.

In Case 1, both the central and the single-phase controllers work at the maximum frequency (10 kHz) without any delays (ideal case). This case is used as reference. In Case 2, the central and the single-phase controllers work at the nominal frequency (1 kHz and 10 kHz) without any delays (perfect real case). In Case 3, the central and the single-phase controllers work at the nominal frequency with the same random communication delay for all the single-phase controllers (quasi-random real case), using a normal distribution with a mean value of 0 (no delay) and a variance of 2% of the nominal communication period. In Case 4, the central and the single-phase controllers work at the nominal frequency with different random communication delay for each single-phase controller (random real case), using the same distribution as in Case 3.

To determine the effect of communication delays, a cumulative trapezoidal integration of the absolute value of the error is performed. This way, the area between the actual value and the reference value is calculated, so that the deviation from the reference value is obtained. Results from Case 1 are used as the reference value for the rest of the cases.

Applying the described cases to the first reactive current reference change, the results of Table II are obtained. As can be seen, the error results get worse if communication delays are considered. Nevertheless, the reference reconstruction implementation reduces the effect of delays into the system, regardless of the analyzed case.

VI. Experimental results

The modular power converter proposed during this paper is also tested experimentally. For that purpose, the experimental setup shown in Fig. 14 is used. The experimental tests analyzes four features of the modular converter: DC link voltage control, reactive power compensation, non-fundamental harmonics mitigation and negative sequence correction.

TABLE II
Cumulative error [A.ms] results from communication delays. Case 1 is used as a reference for the rest of the cases. a) Without reference reconstruction; b) With reference reconstruction.

	CASE2		CASE3		CASE4	
TIME [s]	A)	B)	A)	B)	A)	B)
0.30÷0.40	7.0	0.7	18.0	12.7	18.0	12.5
0.30÷0.32	5.9	0.4	16.3	11.1	16.5	11.2
0.32÷0.34	0.9	0.2	1.4	1.3	1.0	0.9
0.34÷0.36	0.2	0.2	0.3	0.2	0.3	0.3
0.36÷0.38	0.0	0.0	0.1	0.1	0.1	0.1
0.38÷0.40	0.0	0.0	0.0	0.0	0.0	0.0

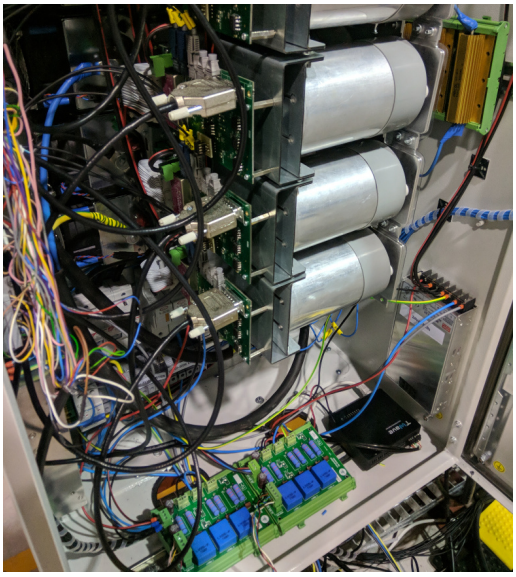

Fig. 14. Experimental setup of a modular converter with a central controller and intelligent single-phase power cells.

The DC link voltage control test is shown in Fig. 15. The reference for the DC voltage is a ramp of 1 s with a final value of 450 V (note that the grid line RMS voltage is 230 V for the experimental tests). As can be seen, the converter current phase is in reversed with respect to the grid voltage, so that active power is absorbed by the converter to charge the DC link.

The reactive power compensation test is shown in Fig. 16. The reference profile for the reactive current consists of a step from 0 A to -10 A and, after 0.4 s, another step from -10 A to $+10$ A. As can be seen, the dynamic response is quite good and there is not error at steady state.

Non-fundamental harmonics mitigation and negative sequence correction are shown in Fig. 17 and Fig. 18. As can be seen, the converter is able to inject current with non-fundamental harmonics and negative sequence to compensate the effect of non-linear/unbalanced loads connected to the grid.

Finally, a THD comparative is done between the implemented modular single-phase control and a three-phase control in dq axis, which was previously implemented in the experimental setup. The THD for the modular control is 5.02%, improving the THD for the three-phase which is 6.71%.

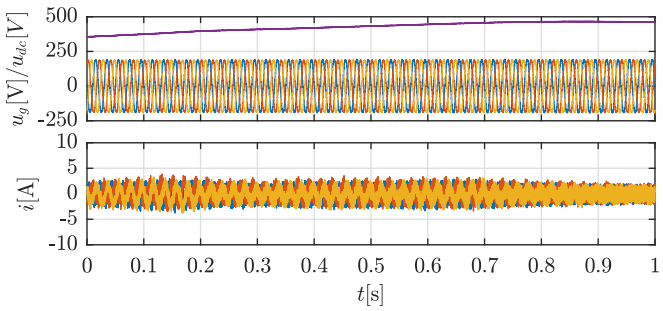

Fig. 15. Experimental results for DC link voltage control. Variables are shown in phase coordinates (abcn): blue, phase A; red, phase B; orange, phase C. Top, grid voltage and DC link voltage (purple). Bottom, converter current.

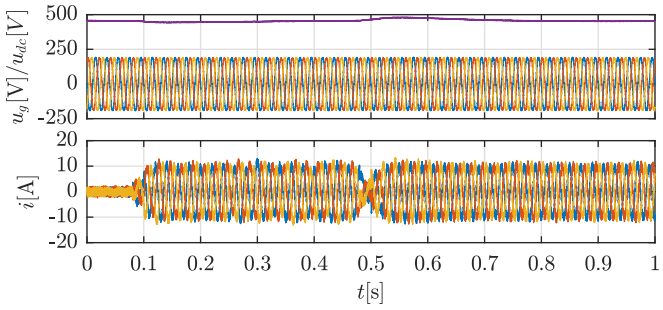

Fig. 16. Experimental results for reactive power compensation. Variables are shown in phase coordinates (abcn): blue, phase A; red, phase B; orange, phase C. Top, grid voltage and DC link voltage (purple). Bottom, converter current.

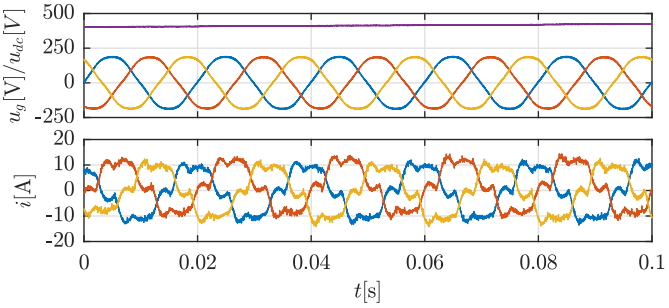

Fig. 17. Experimental results for harmonics mitigation. Variables are shown in phase coordinates (abcn): blue, phase A; red, phase B; orange, phase C. Top, grid voltage and DC link voltage (purple). Bottom, converter current.

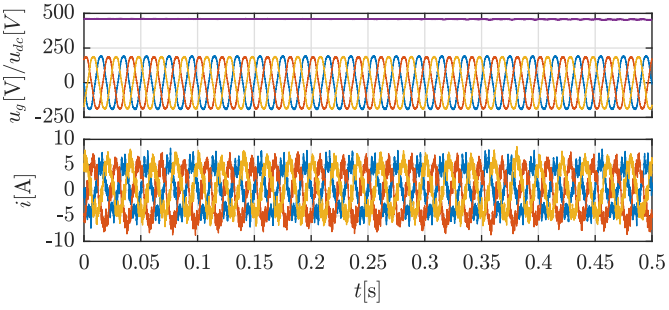

Fig. 18. Experimental results for negative sequence mitigation. Variables are shown in phase coordinates (abcn): blue, phase A; red, phase B; orange, phase C. Top, grid voltage and DC link voltage (purple). Bottom, converter current.

VII. Conclusions

This paper has presented a distributed control alternative based on DRC which can be applied to modular power converters. The proposed alternative was tested via simulations and experimentally, obtaining proper results in terms of steady-state error and transient behavior. Communication delays, frequency shifts and harmonic compensation are analyzed, and a reference interpolator is proposed for mitigating its effects. Simulation and experimental results confirm the viability of the approach.

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