

A Test Circuit for GaN HEMTs Dynamic Ron Characterization in Power Electronics Applications

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Abstract— Wide bandgap devices such as GaN HEMTs are a promising technology in the field of Power Electronics. Due to the physical properties of the Gallium nitride and the device design, they can outperform their Silicon counterparts for the design of highly efficient power switching converters. However, its design should face certain effects that can diminish its performance. One of such effect is the degradation mechanism known as dynamic on-resistance (dynamic R_{ON}), being its mitigation one of the main objectives in the design of the device. In this paper, a circuit is proposed for assessing if this effect is present in GaN transistors in power electronics applications. The circuit allows testing the GaN HEMTs with different stress voltages and times maintaining the desired current level, and allows for repeating the test in successive switching pulses, with adjustable switching frequency and duty cycle, always with the same current, mimicking a real power electronics application.

Index Terms— Semiconductor device reliability, Wide band gap semiconductors, GaN HEMTs, dynamic on-resistance

I. INTRODUCTION

THE use of Wide Bandgap Semiconductors is becoming more common in power electronics, since they can outperform traditional Silicon devices in terms of parasitic capacitances and on-state resistance. This allows power electronic designs at higher frequencies, which enable smaller size in the reactive components and therefore, a smaller size of the converter, while maintaining or even increasing the efficiency. One of the most used devices is the Gallium Nitride (GaN) High Electron Mobility Transistor (HEMT).

However, these devices can have drawbacks which should be addressed, first at the device design stage, and then, at the applications side. One of such effect is the one known as dynamic R_{ON} or current collapse. Under certain conditions, which will be shown in section II, the current capability of these devices is diminished.

This manifests in a higher than expected on-state resistance $R_{DS(on)}$. If this effect takes place during power converter operation, it can degrade its performance and therefore, should be considered during the design process. In order to assess if these effects are present, several methods have been proposed in semiconductor device literature [1]–[3] with commercial pulsed I/V characterization system as well as in power electronics ones, under switching characterization [4]–[8]. However, the test conditions in these methods, may not faithfully represent the conditions at which the transistors will be switching in a power converter. In [9]–[11] different laboratory setups along with a characterization procedure for the dynamic R_{ON} extraction in presence of thermal and voltage stress have been presented. In [9] the power switch is directly characterized inside a half-bridge like circuit, very similar to the final application, but the current over the power switch is implemented by a voltage-controlled current source and not by an inductive load as occur in real power converters. These references focus on analyze the dynamic R_{ON} degradations under temperature, off-state voltage, duty or frequency variations. In our study, we propose a circuit similar to the double pulse tester that allows to characterize the dynamic R_{ON} working under real switching conditions with a voltage and repetitive current stress for multiple pulses, which is not possible to achieve with the classical double pulse test (DPT). In the classical DPT, the DUT must be turned on in order to charge the inductor with the desired current for the test. Although it is possible to apply a voltage stress before the DUT is initially turned on with zero current. This may alter the root cause of the dynamic R_{ON} effects, which is going to be explained in section II. Moreover, during this inductor charge time the DUT will experience self-heating, thus altering too these root causes. Therefore, in this paper a test circuit designed to overcome the aforementioned DPT shortcomings is presented, allowing for a more faithfully reproduction of the conditions faced by the power transistors in most power electronics applications, whilst enabling for precise and variable stress times.

This paper is organized as follows: Section II explain the origins of the dynamic R_{ON} and its effects over a transistor. Section III show tests designed to assess if a device suffers from this effect and its implication in a power electronics application. Experimental results are shown in section IV. Finally, conclusions are addressed in section V.

II. ORIGINS OF DYNAMIC R_{ON}

The most common GaN transistor used in power electronics is the HEMT, a very simplified diagram of an AlGaIn/GaN HEMT can be seen in Fig. 1. HEMTs are a type of Field Effect Transistor in which the conductive channel is a 2D Electron Gas (2DEG). This 2DEG is formed at the interface between a layer of Aluminum Gallium Nitride (AlGaIn) and GaN due to the different conduction band energy between both materials. When a heterojunction is formed in a semiconductor, a transfer of electrons takes place from the material with higher energy to the material with lower energy, where the electrons have a lower energy state. This induces a high concentration of electrons in the heterojunction creating this way the channel known as two-dimensional electron gas (2DEG). The density of the 2DEG can be modulated by the gate to source voltage, therefore, the device could be turned off by applying a gate to source voltage lower than its threshold voltage. The current passing through the 2DEG saturates, making the device behave as a current source when the drain to source voltage is high enough either to deplete the 2DEG near the drain, establishing a pinch-off or to saturate the electron mobility of the 2DEG. If the current is lower the device will behave as a small resistor.

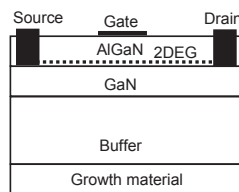


Fig. 1: GaN HEMT Structure.

So far, commercial HEMTs and most of the proposed designs are lateral devices. When a lateral device is in off-state and the drain to source voltage is high enough, the epitaxial layer has an electric field parallel to the conductive channel. This field can make charges to get trapped in the surface or in the defects of the epitaxial layer. These charges can act as voltage source that counteracts the gate to source voltage externally imposed to control the device. One of the effects of these charges, is that the current that the devices can carry before reaching saturation is lower than the one that the devices was originally designed for, then the drain to source on-state resistance is bigger than intended [12]. As this effect varies with the time that the drain to source voltage is applied, it is known as dynamic R_{ON} . Often in literature this effect can also be referred as drain current collapse [2], [13].

The amount of charges trapped depends very much, among other factors, on the device and epitaxial design, the voltage that the device withstands in off-state and the time that this voltage is applied. When the device is turned on for a period of time long enough to remove the charges, the effect is reversed. This time will depend on the device design, the current through the channel and other numerous parameters. The mitigation of this effect is one of the main drivers on the epitaxy layer and surface design ([14], [15]) and nowadays, in order to find this effect, the device has to be in off-state withstanding voltage for times that are in the range of several milliseconds.

In power electronic applications the devices are constantly turning on in resistive mode (the drain to source voltage is very small) and off (when they have to withstand voltage between drain to source) at a rate determined by the switching frequency that the designers of the circuit have chosen. Usually, switching frequencies are in the range of tens to hundreds of kilohertz. The use of GaN devices has started to increase this range up to the Megahertz range. So, the times when the transistors are withstanding voltage are in the order of microseconds. The literature reports much larger time scales for the charge trapping processes involved. However, in certain situations, such as in inverters and motor drives, bridgeless PFC converters, light load burst modes, fault modes or combinations of converters in which one is processing power and others act as a backup, the transistors can be withstanding voltage for much longer times. For example, in an inverter based in a full bridge, the transistors are held at off-state for half the mains period (20 ms in Europe 16.6 ms in USA and Japan). The same will happen in a totem pole bridgeless PFC [16], which is one of the great applications of GaN adoption. Then the transistors will resume switching at a kHz or MHz range. In order to test the effects over a transistor which has been held in off-state, withstanding high drain to source voltage for a long period of time and then switched on and off several times, the test presented in section III-A has been designed. It is important to note that this effect is highly variable with transistor design, epitaxial layer design, surface termination and stress characteristics that will be hard to establish general rules that apply to every device from the observations. However, dynamic R_{ON} test can provide information, which could be useful to the power converter designer to estimate losses and to the device designers to optimize the device designs.

III. INDUCTIVE SWITCHING TEST

A. Double Pulse Tester description.

In power electronic applications is very common that the current through an inductor is diverted through several switches. This means that a transistor in off-state should carry a significant current when it is turned on. For this reason, in order to evaluate the switching performance of a transistor, the DPT is usually performed [17]. The DPT circuit is shown in Fig. 2(a) and the waveforms for the test can be seen in Fig. 2(b). The DPT under inductive load is a common circuit used to evaluate the switching performance of a transistor or a diode. This circuit allows to measuring switching and on-state losses for a fixed $V_{DS}=V_{test}$ and $I_b=I_L$. During the first pulse the inductor current is charged to the desired value, and the falling edge of this pulse and the rising edge of the following pulse are corresponding to the turn-off and turn-on switching transients of the DUT, at any desired voltage and current levels. The test sequence is as follows:

- 1- First turn-on the DUT. The DUT is set to on-state to allow the charge of the inductance to the desired current value. The measurement of this turn-on losses is not considered because the current is always zero at the start of the test.
- 2- Turn-off the DUT. When the current value has reached the

desired value for the test, the DUT is turned-off. At this switching, turn-off losses can be measured because the current has reached to the proper value.

- 3- Second Turn-on the DUT. After a desired off-state stress time the DUT is turned-on again to measure the turn-on losses. It is important that the current through the inductor is kept almost constant during the off time in order to measure the turn-on and turn-off losses under similar current values.

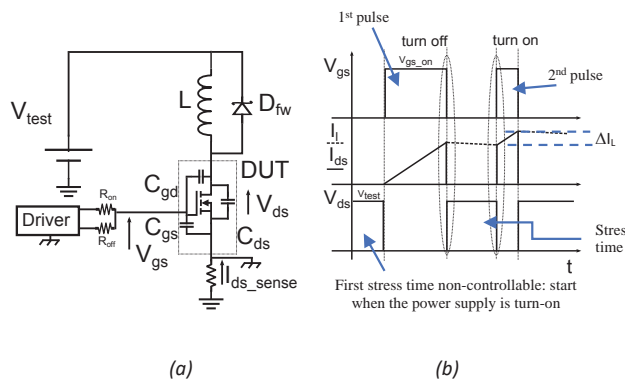


Fig. 2: Dual Pulse Test: (a) The DPT circuit, (b) Waveforms involved in the DPT test.

One important figure of merit is the on-state resistance $R_{DS(on)}$, defined as the ratio of the drain to source voltage, V_{ds_on} , once the gate has reached its final value V_{gs_on} , to the current through the device, I_{ds_on} . This $R_{DS(on)}$ will determine the losses over the device after the switching process, these losses are the so-called conduction losses. Both, switching and conduction losses, determine the power dissipation that the transistor will be withstanding during the converter operation, providing that the current level and voltage are the same as in the DPT test. Therefore, the DPT test provide a faithful measurement of the losses over the device and gives information to the designer about the device capabilities.

However, due to the relevance of trapping over the losses in the devices, information about the dynamic R_{ON} effect is very remarkable to the power converter designers. In the literature, two main mechanism of trapping are reported, one of them induced by the off-state stress voltage applied and the second is related to switching events [18]. Therefore, dynamic R_{ON} must be studied with an accurate control of the off-time stress and under multiple pulse test.

Using the classical DPT, precise control of the stress time is not achievable since the power voltage source (V_{test}) will be applied to the DUT once it is turned on. Another limitation is the different current level switched by the DUT at the turn-off and at the turn-on. After the first gate to source voltage pulse, while the DUT is in off-state, the inductor current will decrease due to the voltage drop in the freewheeling path. Only with unrealistically big inductances, the current can be kept constant. To give a quantitative example of how big must the inductor be, let us consider the off-time applied, 500 ms in our case, and a voltage drop in the freewheeling diode around 1 V. If we set an inductor current ripple of 10 %, which for the maximum current of 7.5 A represents 0.75 A, then the inductor value needed

would be higher than 667 mH, based on the inductor charge equation.

In addition, with the DPT the DUT first turns-on without current and this current is gradually increased through the DUT. This could induce self-heating effects over dynamic resistance, which are demonstrated to be critical in the dynamic R_{ON} measurements. In order to have a measurement closer to the real converter applications, the circuit on Fig. 3 is presented.

B. Multiple Pulse Tester description.

In the multiple pulse tester developed (see Fig. 3), the current through the inductor is charged using Q_4 instead of the DUT, avoiding this way self-heating effects. Also, the control of stress time is independent due to the use of two switches Q_1 and Q_2 . Additionally, the use of a series resistor (R_{damp}) with the inductor, allows to maintain the same current level, taking the ripple into account, during all the pulses applied to the DUT. By pulse we will refer to a pulse in the gate source voltage of the DUT (V_{gs}) so the DUT is in on-state for the pulse duration.

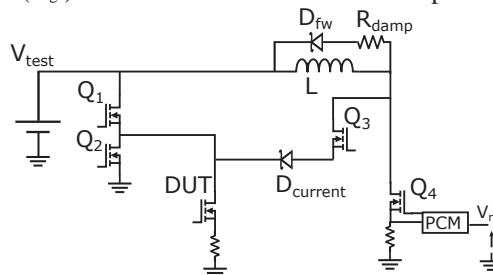


Fig. 3: Circuit for the dynamic R_{ON} test.

The proposed current and time independent stress DPT works as follow: Before the switching of the DUT, the current is kept almost constant by the switching action of Q_4 , which is controlled by a Peak Current Mode control (PCM) circuit intended to be used in switching power supplies. When Q_4 is on, the current through the inductor (sensed by the resistor in series with the transistor) raises until it reaches its programmed value set by V_{ref} . At this moment Q_4 is turned off and the current diverts through the freewheeling diode D_{fw} , as in the classical DPT case. Sometime later, programmed by the switching frequency of the PCM, Q_4 is turned on again and the process repeats as in a peak current-mode controlled switching power supply. Before the DUT is stressed by the voltage source V_{test} , its voltage is kept at zero by Q_2 . This is the situation depicted in Fig. 4(a). When the stress time is applied Q_1 is turned on and Q_2 off, and therefore, the voltage across the DUT is V_{test} . The PCM is keeping the current through the inductor constant before and during the stress time, the diode $D_{current}$ prevents a short circuit when Q_4 is on, as can be seen in Fig. 4(b). After the stress time finish, Q_1 is turned off and Q_4 is permanently turned off. At this moment, the current through the inductor will decrease, and when this current level crosses the predefined current level for the test, Q_3 will be turned on and, a delay after, the DUT will be switched on. The delay between DUT and Q_3 is set in order to not affect the first turn-on transition of the DUT due to the turn on transition of Q_3 . This delay has a fixed part which is around 1 μ s, and a variable part which depends on the

time needed by the current to fall and cross a trigger level previously fixed in the digital oscilloscope.

At this moment, when the oscilloscope is triggered, the auxiliary output of the oscilloscope will send an enable signal to the trigger input of an arbitrary signal generator. The arbitrary generator will start the previously defined repetitive pulses to drive the DUT for the test. During this period the circuit is on the state shown in Fig. 4(c) and the current and the drain-source voltage of the DUT will be recorded on the oscilloscope. Fig. 5 shows a picture of the test circuit for the dynamic R_{ON} characterization.

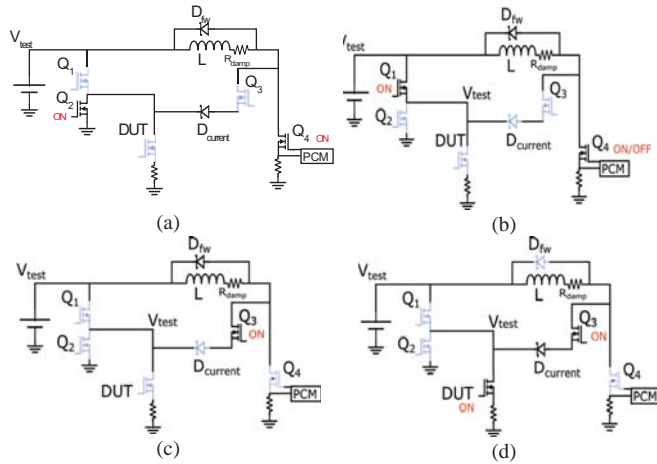


Fig. 4: Test procedure: (a) Current precharge, (b) Voltage stress, (c) Pre-test stage, (d) Multipulse Test.

More than one pulse will be always done in order to assess if the charges, causing the dynamic R_{ON} effect, can be removed after one switching period. The current at the beginning of each pulse has to be the same in order to be able to compare the first, second and next pulses. For this purpose, the R_{damp} is placed in series with the load inductor. This is the way to control the di/dt in the on and off times for the inductor current. The value of this resistor has been calculated with (1), where V_{test} is the voltage applied to the DUT during the stress interval, V_{F_Dfw} is the forward voltage of the free-wheeling diode, D is the duty of the DUT and I_{L_avg} is the average current level of the inductor that sets the desired value for the drain current.

During this process the circuit remains in the state represented in Fig. 4(d). Finally, Q_3 is turned off to remove the current while the DUT is still switching, resetting the DUT to its original state. The time Q_3 is in on-state it is called t_{test} . In Fig. 6, all the switching signals mentioned in the above explanation are shown in order to easy follow the switching procedure.

$$R_{damp} = \frac{V_{test} + \left(1 - \frac{1}{D}\right) \cdot V_{F_Dfw}}{\frac{I_{L_avg}}{D}} \quad (1)$$

IV. EXPERIMENTAL RESULTS

A. Hardware and test description.

The circuit described in section III-B and depicted in Fig. 3 has been implemented in a PCB to test GaN devices with a

careful design of the gate drive circuit, component selection and board layout, to minimize the parasitic inductance and capacitance of both, the gate loop and the power loop.

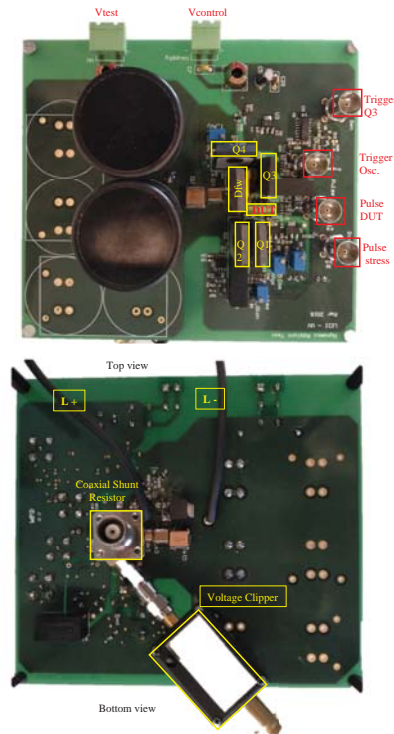


Fig. 5: Photograph of the test circuit for the dynamic R_{ON} characterization.

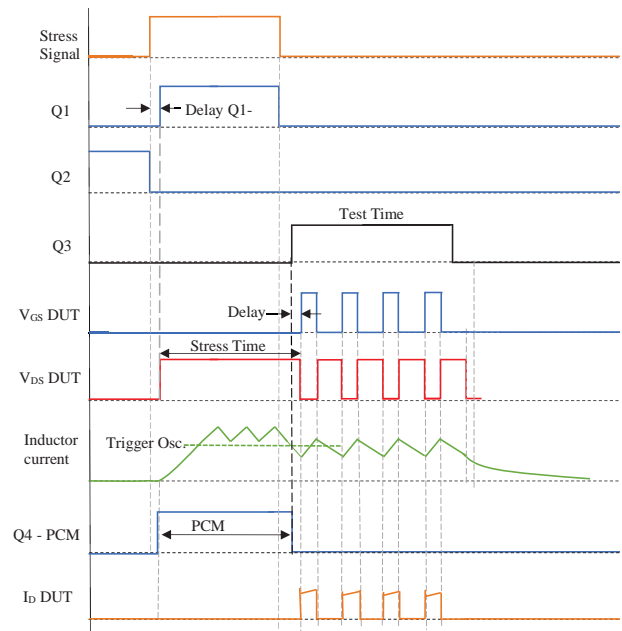


Fig. 6: Waveforms for the inductive switching test.

Transistors Q_1 , Q_2 and Q_3 are SiC MOSFETs C3M0280090D (Wolfspeed) to minimize the output capacitance as possible and Q_4 is a SiC MOSFET C2M0025120D (Wolfspeed) to have the lower output capacitance but being able to drive high currents during the current precharge time without need of a heatsink. Diodes are Silicon Carbide Schottky diodes, D_{fw} is C5D50065D

(Wolfspeed) and D_{current} is C4D05120A (Wolfspeed) to allow fast commutation processes. For the inductor, two different single layer air core inductors have been made. For the devices below 200 V the value of the inductor is $696 \mu\text{H}$ and for the devices over this voltage an inductor of 2.48 mH has been used. The values of the inductors are selected in order to have current ripple between 5 % and 40 % of the current level desired in the DUT, depending on the voltage and current conditions, and always guaranteeing the continuous conduction mode. The resistance in series with the inductor is calculated from (1), and changed in every test depending on the conditions in order to have the same current in all the pulses.

Current through the DUT is measured by a low inductance coaxial shunt resistor of $50 \text{ m}\Omega$, SDN-414-05 from T&M Research Products with a bandwidth of 2 GHz. A good precision in the on-resistance measurement is needed, but it is a difficult task because it is hard to accurately measure the drain-source voltage drop at the DUT. The problem is the large dynamic range of the input signal. If we select a small voltage range per division, the oscilloscope input amplifier is overloaded and an accurate determination of the on-state voltage is not achievable with standard measurement equipment. To solve this problem, the drain-source voltage of the DUT is measured with a combination of a passive voltage probe (PMM511A) of 500 MHz bandwidth and a commercial voltage clipper clp150015A from Springburo with a clamping voltage of 2.5 V and a settling time around 200 ns.

In our test campaign, a gate signal of 50 % duty with an on-time of $10 \mu\text{s}$ has been applied. This is the situation depicted in Fig. 7, see how similar the real waveforms are to the theoretical ones depicted in Fig. 6. The main difference is the overshoot of the current, mainly caused by the parasitic capacitances of D_{rW} and the inductor. These waveforms, in each of the pulses, are recorded and analyzed for checking the effects of the dynamic R_{ON} by a 9-bit resolution digital oscilloscope HDO9404 (4GHz) from Teledyne LeCroy.

B. Results.

In order to evaluate the on-resistance several tests were performed with enhancement mode Gallium Nitride devices. Several approaches have been proposed to obtain normally-off or enhancement mode (e-mode) devices. We select two options commercially available. One is the technology developed by Efficient Power Conversion that has chosen to modify the heterojunction under the gate to deplete the two-dimensional electron gas (2DEG) of electrons. Another solution is a recessed gate metal-insulator electron mobility transistors (MISHEMTs) made by GaN Systems. In order to have some samples from each device architecture, we have selected the EPC8004C and the GaN Systems GS66508P, encompassing different current and voltage levels. Also, one Silicon MOSFET device (IRF540) has been tested in order to have a reference without change in his $R_{\text{DS(on)}}$ due to trapped charges thanks to the optimization of the passivation processes. The test over this device has been used also as a dry-run test to validate the hardware and measurement procedure.

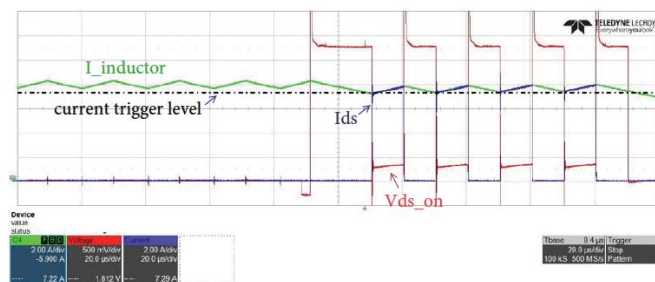


Fig. 7: Waveforms of the test: Full test waveform with $19 \mu\text{s}$ stress time

The $R_{\text{DS(on)}}$ is measured for different current levels (2.5 A, 5 A and 7.5 A). A total of 7 different stress times were defined, these are $19 \mu\text{s}$, $64 \mu\text{s}$, $514 \mu\text{s}$, 20 ms (the grid period in Europe), 50 ms and 500 ms. The extraction of the $R_{\text{DS(on)}}$ parameter has been done defining a small window to obtain the average value at the final of the on-time in each pulse. This calculation has been obtained automatically by defining a mathematical function in the digital scope. For all the devices under test, we have chosen a gate to source voltage to ensure the minimum $R_{\text{DS(on)}}$ in the channel (EPC and GaN Systems devices $V_{\text{GS}}=5 \text{ V}$ and Silicon device $V_{\text{GS}}=10 \text{ V}$). For the voltage stress we have chosen the 80 % of the absolute maximum voltage range for each device, as is done in real applications.

Before starting with the dynamic test, it is necessary to know the accuracy of our measurement system. First, we have estimated in 2 %, the error of our measurement system, considering the drain voltage and drain current measurements accuracy. Secondly, we have measured 50 times the $R_{\text{DS(on)}}$ of the Silicon MOSFET IRF540 in a single pulse. The results are shown in Fig. 8, and the standard deviation (σ) calculated from these results has been $0.558 \text{ m}\Omega$. Assuming that the measurements behave as a normal distribution, 99.7 % of the samples should lay in the $\pm 3\sigma$ interval around the average. Therefore, any measurement outside this interval it is highly unlikely to be due to the randomness of the measurements. This result proves that the measurement in our setup are repetitive and the error obtained will be used to determine if any possible change in the $R_{\text{DS(on)}}$ could be due to the error or to the stress time applied.

The results of $R_{\text{DS(on)}}$ in the first pulse for the DUTs can be seen in Fig. 9 where the $R_{\text{DS(on)}}$ measurement is plotted. In order to have a reference, the $R_{\text{DS(on)}}$ measurement with the minimum stress time was done 50 times extracting the mean value and the standard deviation.

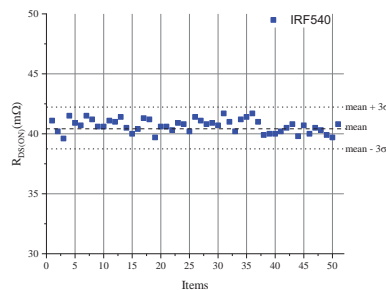


Fig. 8: Repetitive measurements with 2.5 A and $19 \mu\text{s}$ stress over IRF540.

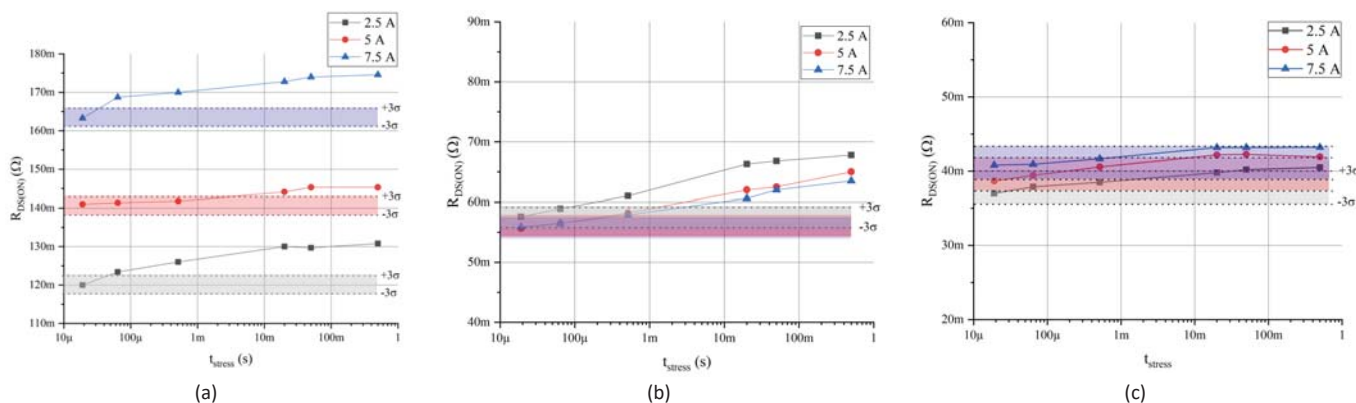


Fig. 9: Measured $R_{DS(on)}$ in the first pulse for different current levels, increasing the stress time. a) EPC results b) GS results and c) Silicon MOSFET results.

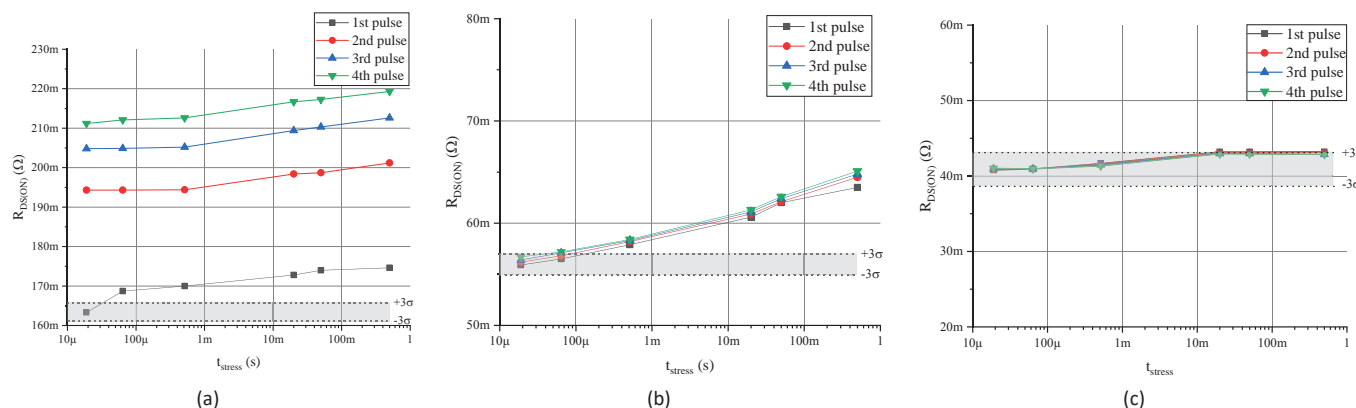


Fig. 10: Measured $R_{DS(on)}$ for 7.5 A, increasing the stress time in four pulse switching sequence. (a) EPC results (b) GS results and (c) Silicon MOSFET results

The limits that determine the statistical significance of the measurement are represented by a colored area of width $\pm 3\sigma$ about the mean value for the case of 2.5 A and the minimum stress time of 19 μs . It can be seen how the stress time does not affect significantly the value of the $R_{DS(on)}$ for the silicon MOSFET shown in Fig. 9(c), since the variations are inside the 3σ limit defined. This agrees with the theory in the sense that the $R_{DS(on)}$ of a Silicon MOSFET should not be affected by the stress voltage applied during the off-time. However, a significant drift, beyond the 3σ is observed in GaN Systems device. It can be appreciated in Fig. 9(b) how the $R_{DS(on)}$ increases with the stress time a 17.7 % for the maximum stress time. The EPC8004 device shows an increase on the $R_{DS(on)}$ with stress time less significant (a 9 % for the maximum stress time, Fig. 9(a)).

It is important to check if the dynamic R_{ON} effect is permanent or if it is removed when the converter works in its normal mode: switching continuously. Therefore, the next step done was to evaluate the $R_{DS(on)}$ not only in the first pulse after the stress but in the following pulses. Measurements were carried out in the second, the third and the fourth pulse maintaining the same drain current level thanks to the proposed test circuit. Fig. 10 shows the results for the maximum current (7.5 A) and the four pulses of the tests done. The results show that the $R_{DS(on)}$ increases very significantly with each pulse for the EPC devices. This effect is not seen for the GaN Systems or Silicon MOSFET devices. This strong influence over the dynamic resistance could be very critical in real power

applications. The desired behavior would be that during the on-state time the traps are recovered, and thus the $R_{DS(on)}$ does not increase in the following pulses. However, if the detrapping time constants are longer than the on-state time, then the detrapping process is not finished before the next off-state when the voltage stress is applied and a new trapping process takes place. Thus, the $R_{DS(on)}$ increases with each pulse, eventually this process will stop when an equilibrium is reached. Fig. 10(a) show how the dynamic resistance of the EPC8004 increases with the number of pulses. In order to see how big is that influence on the final resistance, we have increased the number of pulses up to 100, for the minimum stress time of 19 μs and a voltage stress of 80% maximum rated drain-to-source voltage. The results are shown in Fig. 11(a), where it can be seen how the resistance increases from 148.2 m Ω in the first pulse to 324.6 m Ω in the 50th pulse, which represent an increment of 219 %, eventually this rise in $R_{DS(on)}$ seems to stop there. This increase does not happen in GS66508P, which is shown in Fig. 11(b) under the same conditions.

This increase in dynamic resistance, could be due to two phenomena, the first is the self-heating. It is well-known that self-heating can induce a measurable increase in the on-resistance. The second can be the hot-electron trapping that can get place during the switching events. In order to demonstrate that the $R_{DS(on)}$ increase is mainly due to the hot electron trapping and not to the self-heating during self the multi-pulse test we have repeated the test, which results are shown in Fig. 11(a), with the same bias conditions but now heating the DUT

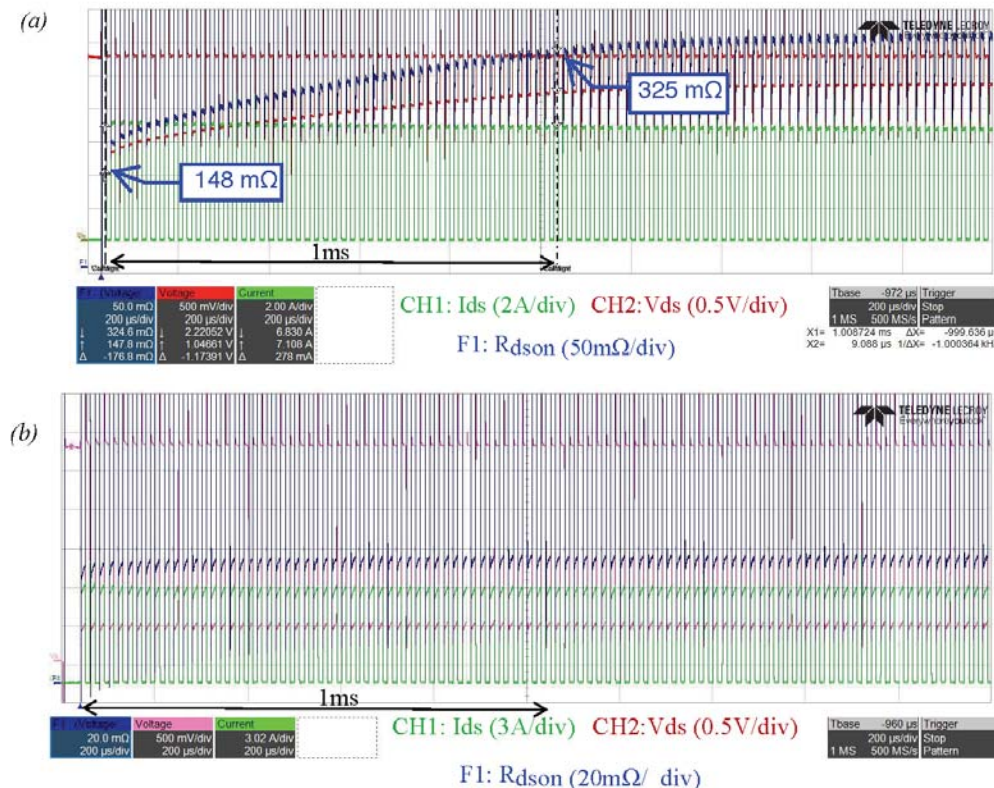


Fig. 11: 100 pulse measurement with 7.5 A, $t_{\text{stress}}=19 \mu\text{s}$ and $V_{\text{stress}}=80\% V_{\text{DS,max}}$ at room temperature over (a) EPC8004 and (b) GS66508P devices

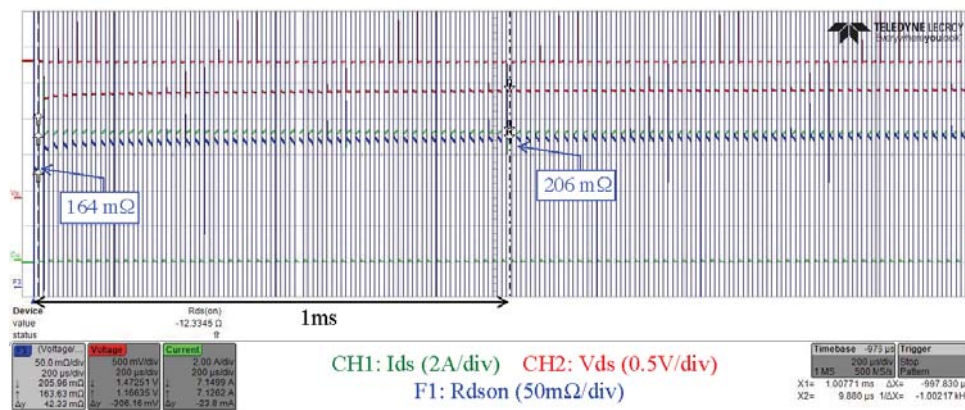


Fig. 12. 100 pulse measurement with 7.5 A, $t_{\text{stress}}=19 \mu\text{s}$ and $V_{\text{stress}}=80\% V_{\text{DS,max}}$ over EPC8004 for a case temperature of 100 °C

externally up to 100°C (the maximum operating temperature is 150°C). The ambient temperature has been measured with a thermocouple in the case of the DUT and the test was performed after the temperature stabilized at 100°C. The results for the tests at 100°C can be seen Fig. 12. In both tests, at room temperature and at 100°C, the conduction and switching losses will be approximately the same, since the current, voltages and switching frequencies are the same. In fact, the only expected change in the power dissipation comes from the additional dissipation due to the increased $R_{\text{DS(on)}}$ because of the increased temperature.

However, the experimental results show that the $R_{\text{DS(on)}}$ decreases from 324.6 mΩ to 205.6 mΩ measured at the pulse

50. It is known [19], [20] that high temperature is a factor to increase the detrapping process, thus reverting the cause for the increase of the $R_{\text{DS(on)}}$ due to the trapping process. Therefore, the increase in the $R_{\text{DS(on)}}$ at room temperature during the multi-pulse test (Fig. 11a) is not mainly due to the increase of temperature by self-heating but, most likely, due to an accumulation of trapped charges.

It is demonstrated by Rosseto et al. [21] that hot electron effects that take place during switching events can induce a measurable increase in dynamic resistance and the solution to this problem could be using soft-switching conditions.

V. CONCLUSIONS

In this paper, a test circuit for dynamic R_{ON} characterization is proposed. This circuit overcomes some of the typical Double Pulse Tester limitations. The main improvements are the full control over the following characteristics: the drain voltage stress time, the repetitive constant current level and the possibility to make multiple pulses varying frequency and duty cycle conditions. This full control allows designers to faithfully reproduce the real conditions, at which, devices will be submitted in the real power electronic applications. All the different tests enabled by the proposed circuit are carried out and reported using two commercial GaN HEMTs, with different device technology, and one Silicon MOSFET transistor for comparison purposes.

The measurements done over the two different GaN HEMT structures have shown that the $R_{DS(on)}$ behaviour can be really different and cannot be evaluated in one single pulse. When multiple pulse measurements are carried out, as happens in real application, one of the structures tested have shown the effect of the hot electron trapping in the switching. This trapping induces a significant $R_{DS(on)}$ increase, around 200 % of the typical value. This increase degrades the performance of the device and can result in life time reduction, or even, the device breakdown due to thermal effects. The power electronics designers must consider the real value of the $R_{DS(on)}$ that depends on the voltage and current levels supported, the switching frequency and the type of switching (soft or hard) in order to estimate the conduction losses of the power devices. These measurements suggest that in certain devices, the decision to incorporate soft switching techniques can bring advantages beyond the traditional switching losses reduction. It is known that soft switching minimizes the trapping effects due to hot electrons. Then, in the devices affected by a strong dynamic R_{ON} effect soft switching can also reduce the conduction losses, since the R_{ON} increase is minimized.

Therefore, this circuit has shown two main advantages that are the full control of the off-state stress, and the possibility of switching the DUT under the same current level in multiple pulse conditions, simulating real converter applications since the first pulse. Both advantages, but mainly the second, have demonstrated to be really useful, because of the needed of multiple pulses with adjustable switching frequency and duty cycle, to evaluate correctly the dynamic resistance influence on the real application.

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REFERENCES

- [1] B. Lu, T. Palacios, D. Risbud, S. Bahl, and D. I. Anderson, "Extraction of dynamic on-resistance in GaN transistors: Under soft- and hard-switching conditions," in *Compound Semiconductor Integrated Circuit Symposium (CSICS), 2011 IEEE*, pp. 1–4, Oct 2011.
- [2] D. Jin and J. A. del Alamo, "Methodology for the study of dynamic on-resistance in high-voltage GaN field-effect transistors," *IEEE Trans. Electron Devices*, vol. 60, pp. 3190–3196, Oct. 2013. DOI: 10.1109/TED.2013.2274477
- [3] H. Huang, Y. C. Liang, G. S. Samudra, T-F. Chang, and C-F. Huang, "Effects of Gate Field Plates on the Surface State Related Current Collapse in AlGaIn/GaN HEMTs," *IEEE Trans. Power Electronic.*, vol. 29, no. 5, pp. 2164–2173, May. 2014. DOI: 10.1109/TPEL.2013.2288644
- [4] B. Lu, T. Palacios, D. Risbud, S. Bahl, and D. I. Anderson, "Extraction of Dynamic On-resistance in GaN Transistors under Soft- and Hard-switching Conditions," in *IEEE Comp. Semic. Integr. Circuit Symp. (CSICS)*, Oct. 2011.
- [5] N. Badawi and S. Dieckerhoff, "A new method for dynamic ron extraction of gan power hemts," in *PCIM Europe 2015; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management; Proceedings of*, pp. 1–6, May 2015.
- [6] J. Böcker, *et al.*, "Experimental analysis and modeling of GaN normally-off HFETs with trapping effects," *2015 17th European Conference on Power Electronics and Applications (EPE'15 ECCE-Europe)*, Geneva, 2015, pp. 1-10. DOI: 10.1109/EPE.2015.7309328.
- [7] N. Badawi, O. Hilt, E. Behat-Treidel, J. Böcker, J. Würfl, and S. Dieckerhoff, "Investigation of the dynamic on-state resistance of 600V normally-off and normally-on GaN HEMTs," in *2015 IEEE Energy Conversion Congress and Exposition (ECCE)*, Montreal, QC, 2015, pp. 913-919. DOI: 10.1109/ECCE.2015.7309785
- [8] H. Wang, J. Wei, R. Xie, C. Liu, G. Tang, and K. J. Chen, "Maximizing the Performance of 650-V p-GaN Gate HEMTs: Dynamic RON Characterization and Circuit Design Considerations," *IEEE Trans. Power Electronics*, vol. 32, no. 7, pp. 5539–5549, Jul. 2017. DOI: 10.1109/TPEL.2016.2610460
- [9] T. Cappello, A. Santarelli and C. Florian, "Dynamic RON Characterization Technique for the Evaluation of Thermal and Off-State Voltage Stress of GaN Switches," in *IEEE Trans. Power Electronics*, vol. 33, no. 4, pp. 3386-3398, Apr. 2018. DOI:10.1109/TPEL.2017.2710281
- [10] K. Li, P. Evans, and M. Johnson, "GaN-HEMT dynamic ON-state resistance characterisation and modelling," in *2016 IEEE 17th Workshop on Control and Modeling for Power Electronics (COMPEL)*, Jun. 2016, pp. 1–7.
- [11] M. Elharizi, Z. Khatir, R. Lallemand and J. Ousten, "Investigations on the Evolution of Dynamic Ron of GaN Power Transistors during Switching Cycles," *CIPS 2018; 10th International Conf. on Integrated Power Electronics Systems*, Stuttgart, Germany, 2018, pp. 1-6.
- [12] Agnihotri, Shantanu et al. "Modeling of trapping effects in GaN HEMTs" in *2015 Annual IEEE India Conference (INDICON)*. 10.1109/INDICON.2015.7443658
- [13] M. Meneghini, E. Zanoni, and G. Meneghesso, "Gallium nitride based hemts for power applications: High field trapping issues," in *Solid-State and Integrated Circuit Technology (ICSICT), 2014 12th IEEE International Conference on*, pp. 1–4, Oct 2014.
- [14] R. Vetury, N. Q. Zhang, S. Keller, and U. K. Mishra, "The impact of surface states on the dc and RF characteristics of AlGaIn/GaN HFETs," *IEEE Transactions on Electron Devices*, vol. 48, pp. 560–566, Mar. 2001. DOI:10.1109/16.906451
- [15] M. J. Uren, *et al.*, "Intentionally carbon-doped AlGaIn/GaN HEMTs: Necessity for vertical leakage paths," *IEEE Electron Device Letters*, vol. 35, pp. 327–329, Mar. 2014. DOI:10.1109/LED.2013.2297626
- [16] Z. Liu, F. C. Lee, Q. Li, and Y. Yang, "Design of GaN-based MHz totem-pole PFC rectifier," *IEEE. Journal of Emerging and Selected Topics in Power Electronics (Volume: 4, Issue: 3, Sept. 2016)*. DOI:10.1109/JESTPE.2016.2571299

- [17] B. Baliga, *Fundamentals of Power Semiconductor Devices*. Springer 2nd edition 2019, Springer International Publishing, ISBN 978-3-319-93987-2.
- [18] Po-Chien Chou *et al.*, "Comprehensive dynamic on-resistance assessments in GaN-on-Si MIS-HEMTs for power switching applications" May. 2018, *Semicond. Sci. Technol.* 33 055012. DOI:10.1088/1361-6641/aabb 6a
- [19] Yang Li-Yuan *et al.*, "High temperature characteristics of AlGaIn/GaN high electron mobility transistors", *Chinese Phys. B* Vol. 20, No. 11, Nov. 2011. DOI:10.1088/1674-1056/20/11/117302
- [20] Sandeep Kumar *et al.*, "Temperature and Bias Dependent Trap Capture Cross Section in AlGaIn/GaN HEMT on 6-in Silicon with Carbon-Doped Buffer", *IEEE Trans. Electron Devices*, vol. 64, No. 12, Dec. 2017.
- [21] I. Rossetto *et al.*, "Evidence of Hot-Electron Effects During Hard Switching of AlGaIn/GaN HEMTs," in *IEEE Trans. Electron Devices*, vol. 64, no. 9, pp. 3734-3739, Sep. 2017. DOI:10.1109/TED.2017.2728785

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