A very simple analog control for QSW-ZVS source/sink dc-dc converters with seamless mode transition

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***Abstract*— A simple, analog, control circuit is proposed for seamless transition between source and sink modes in a Quasi-Square-Wave Zero Voltage Switching (QSW-ZVS) source/sink dc-dc converters. The inductor current is controlled by a variable-width hysteretic current mode control. The upper and lower bounds of the hysteretic band are clamped to ensure QSW-ZVS operation with a single current command and independently from the power flow direction. This enables the control of any PWM converter able to operate in QSW-ZVS with a single control loop. Implementing a complex multi-mode or look-up-table based digital control is no longer required. A 50W buck converter and a 100W boost converter are built to demonstrate the proposed control circuit.**

Keywords—QSW-ZVS, TCM, analog control, HCMC, ZVS.

I. INTRODUCTION

Point-of-load applications usually require compact, inexpensive, but efficient solutions. A well-known approach is the use of Quasi-Square-Wave (QSW-ZVS) mode of operation [1], also known as Triangular Current Mode (TCM) [2]. In these modes, Zero Voltage Switching (ZVS) can be achieved [1]–[3] thanks to the resonant sub-interval during the dead-time. When a synchronous converter is used, it is possible to keep ZVS operation even for bidirectional power flows. The ZVS can be guaranteed for any power by varying the switching frequency according to the load [4]. Soft-switching operation allows to increase the efficiency of QSW-ZVS converters or to reduce their size by increasing the switching frequency with the same power loss. These two properties make this mode very interesting when aiming to obtain a compact and efficient converter.

The operation of QSW-ZVS converters is based on three intervals: magnetizing interval (on-time), demagnetizing interval (off-time) and resonant interval (dead-time). These intervals can be controlled by different ways. Traditionally, digital controllers are widely used [2], [5], [6]. As it is well known, digital control has the advantage of flexibility; hence, those applications that require some kind of reconfiguration are typically controlled with a digital platform. This is the case of dc micro-grids [7], [8]. In other cases, it is required that the QSW-ZVS power converter has to work in a certain operational range

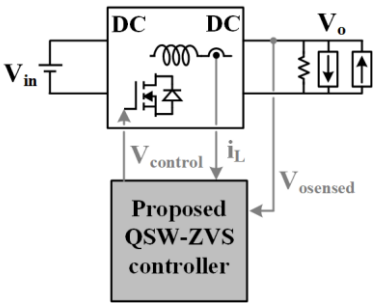

Fig. 1. Output voltage regulated source/sink converter supplying active and passive loads.

(e.g. input voltage range). In such a case, the digital control enhance the implementation of very complex techniques, such as dead-time regulation [6], current sharing with interleaving or phase shedding. [9]. In all the previously stated applications, the control stage is implemented on a Digital Signal Processor (DSP) or on a Field-Array Programmable Gate Array (FPGA). In either case, in cost sensitive applications these platforms are not allowed.

Nowadays, the use of more electronics loads and power converters is an obvious trend. This is particular relevant in some applications, such as automotive dc buses with energy storage systems [5] or DDR (Double Data Rate) Memory terminators [10]. These applications require the management of active loads. The active loads can both demand power from the bus or inject current into it, as shown in Fig. 1. The converter must regulate the output dc bus for any connected load, providing a certain quality of service. This kind of converters are usually known as source/sink converters [10], as they can source current to the bus, if a passive load is used, or sink it back into the primary power source if an active load is connected instead.

These source/sink power converters, as well as point-of-load applications, require a very simple and cost effective solution. Therefore, an analog controller seems more adequate for these applications. This work proposes a very simple analog control for dc-dc QSW-ZVS source/sink power converters. The main goal of the solution proposed here is to implement a controller

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stage which guarantees ZVS operation with a seamless transition between source and sink modes (i.e. when a passive or an active load is connected to the dc bus). Moreover, the solution has a reduced component count which can be easily implemented in a dedicated Integrated Circuit (IC).

This paper is organized as follows. In Section II, a basic description of QSW-ZVS behavior is introduced, along with a detailed explanation and analysis of the proposed controller. The experimental results are summarized in Section III, remarking those important aspects in the design. Finally, the main conclusions of this work are outlined in Section IV.

II. DESCRIPTION OF THE PROPOSED CONTROL CIRCUIT

A. *Voltage mode control for bidirectional QSW-ZVS converters*

As it was mentioned before, QSW-ZVS operation is rather simple. At the end of the magnetizing interval (i.e. at t_{on}) the peak current through the inductor (I_{ctrl}) must reach approximately twice the desired average output or input current. At the end of the demagnetizing period (i.e. at t_{off}) the current through the inductor should be slightly negative ($-I_{ZVS}$). This value should be large enough to discharge the MOSFET output parasitic capacitance during the resonant period (dead-time) [3]. As $-I_{ZVS}$ is fixed and has to be reached every switching period, the average output current depends solely on I_{ctrl}. Therefore, the only way to increase I_{ctrl} is by varying the switching period.

When the converter operates in source mode, the value of I_{ctrl} is determined by t_{on}. However, as QSW-ZVS requires an inherent variable switching frequency, the end of the switching period is estimated by the event ZCD, which guarantees a certain ZVS current. This event depends on the inductor current measurement and the voltage control, as can be seen in Fig. 2(a). However, in sink mode (i.e. when the power flows from the load to the source), the t_{on} command conflicts with the ZCD, while the switching period and the value of I_{ctrl} cannot be controlled, as seen in Fig. 2(b).

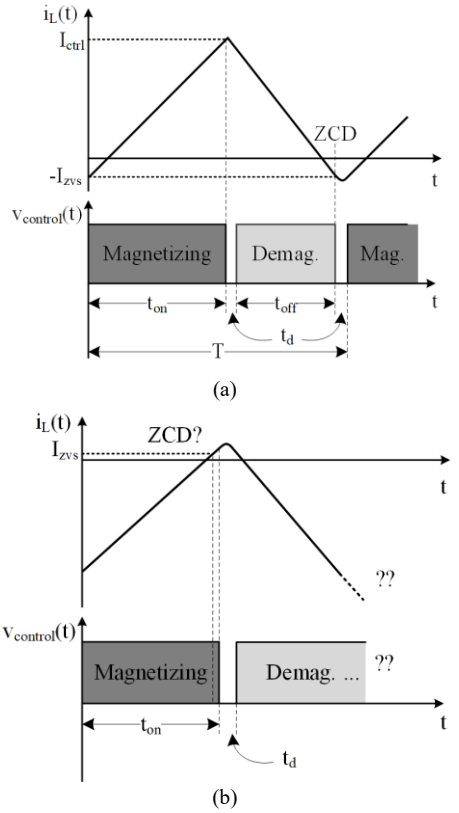


Fig. 2. Inductor current and gate signals for the main switch and the synchronous rectifier of a QSW-ZVS converter with traditional voltage mode control: (a) forward power flow (source mode) (b) reversed power flow (sink mode).

B. *Control method proposal*

As it was stated before, in QSW-ZVS converters the inductor current is always varying within an upper and a lower bound. Therefore, it seems appropriate to employ a hysteretic current mode control (HCMC) [11], [12]. This control mode imposes the use of a current sensor for measuring the current through the inductor; nevertheless, this was already required for traditional voltage control. Traditional HCMC has a fixed-width hysteretic band, which does not ensure that the current reaches $\pm I_{ZVS}$. For bidirectional QSW-ZVS operation, the hysteretic bandwidth has to vary in order to keep the inductor current between I_{ctrl} and $-I_{ZVS}$ for source mode and between I_{ZVS} and a negative I_{ctrl} for sink mode.

Variable-width HCMC has been previously implemented digitally [5], [12], adding and subtracting half the bandwidth to

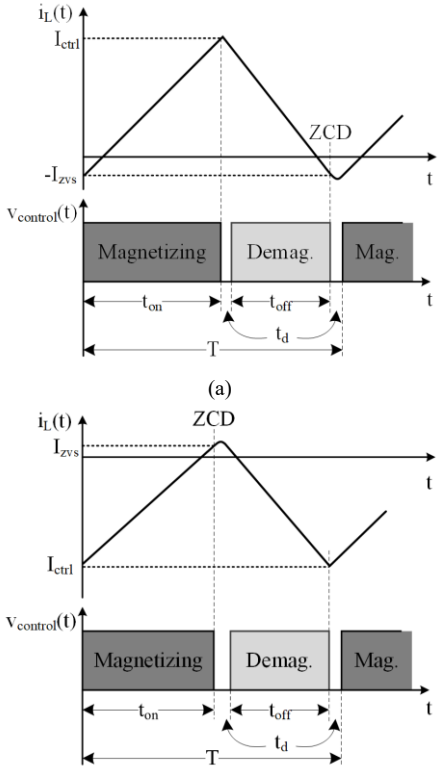


Fig. 3. Inductor current and gate signals of a QSW-ZVS converter with variable-width HCMC control: (a) source mode (b) sink mode.

the control value to generate the upper and lower. As this approach is not simple to implement with analog circuitry, a different solution is taken. For unidirectional power flow, $-I_{ZVS}$ could be used as the lower, fixed bound, while I_{ctrl} is the upper, controllable bound, as can be seen in Fig. 3(a). If I_{ctrl} is provided by a control loop, there is no need to implement analog adders, greatly simplifying the circuit. However, when I_{ctrl} becomes negative and the power flow has to be reversed, I_{ZVS} has to be used as the upper, fixed bound while I_{ctrl} is the new lower, controllable bound, as it is depicted in Fig. 3(b).

In order to implement this variable HCMC controller, the circuit shown in Fig. 4 is proposed. A simple voltage loop compensator can be used for obtaining the controllable bound V_{Ictrl}. After this operational amplifier, two diodes are used for clamping V_{Ictrl} voltage to the maximum or minimum current needed for achieving ZVS (V_{IZVS} and $-V_{IZVS}$). The clamped voltages are then compared to the current measurement (V_{iL}). These comparators generates the upper and lower bound respectively. A latch generates the gate signals based on two events: Set and Reset. At the beginning of the switching cycle, the latch is set and the main switch of the converter is on, magnetizing the inductor. When V_{iL} reaches the upper bound (i.e. $V_{Iupper} = \max\{V_{Ictrl}, V_{IZVS}\}$), the latch is reset, the main switch is turned off and the inductor is demagnetized. When V_{iL} reaches the lower bound (i.e. $V_{Ilower} = \min\{V_{Ictrl}, -V_{IZVS}\}$), the latch is set and a new switching cycle starts. It should be noted that Fig. 4 shows how the control is implemented with the scaled voltages provided by the sensor and control loop and not the actual currents. Using the proposed circuit, when V_{Ictrl} is greater than V_{IZVS}, power flows from input to output and operates in source mode. If V_{Ictrl} becomes smaller than $-V_{IZVS}$, the power flow is reversed and the converter sinks current. When V_{Ictrl} takes a value between V_{IZVS} and $-V_{IZVS}$, no current is transferred and the converter operates at zero power at its maximum switching frequency, which depends on the value of I_{ZVS} and the inductor value.

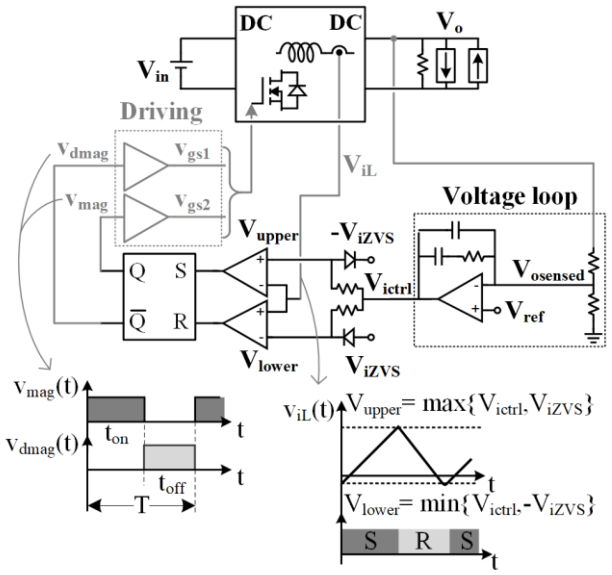


Fig. 4. Proposed implementation of the variable-width HCMC controller.

In this work, the voltage V_{Ictrl} is set by voltage loop for regulating the output voltage. However, the circuit shown in Fig. 4 can be applied to control any electrical variable of the power converter, such as the input voltage or the average output current. Finally, an appropriate MOSFET driver should be used to ensure that the dead-time is long enough to achieve ZVS. The dead-time can be either fixed [3] or adaptive [6].

III. EXPERIMENTAL RESULTS SOURCE/SINK BUCK AND BOOST CONVERTERS

A. Converter design

In order to validate the proposed control circuitry, two different prototypes were built in the laboratory. First, a simple synchronous buck converter is used to illustrate the seamless mode transition. Second, a synchronous boost converter is also built to demonstrate the flexibility of the controller. The main characteristics of both power converters and their components are summarized in Table 1.

The design of the power stage follows the traditional procedure described in the literature. Both converters use exactly the same power MOSFETs because of their relative low price and size, their low on-resistance and an equivalent output capacitor of just 302pF. The converters were designed slightly different: the buck converter is designed to provide a maximum power of ±50W switching at 40kHz, whilst the boost converter is developed for providing ±100W with the same switching frequency at full load. In order to do so, inductance value is different for each topology: 69.6µH for buck and 33µH for boost converter. Moreover, power inductor of buck converter is custom designed based on a RM8 bobbin, whilst the one used in the boost converter is a commercial one from Coilcraft. Taking into account the inductance value and the output capacitor of the power MOSFETs, the necessary amount of negative current I_{ZVS} is roughly 150mA and 300mA respectively for both converters. In both cases, the control circuitry is a simple type II regulator to provide the control command V_{Ictrl} and to get a stable output voltage. It is designed with a relatively small bandwidth and phase margin to clearly show its effect in the measurements. The driver is a basic ISL6700 half-bridge driver, with fixed dead-times.

TABLE 1. COMPONENTS AND MAIN SPECIFICATIONS FOR BUCK AND BOOST PROTOTYPES.

Parameter	Buck prototype	Boost prototype
V_{in} [V]	48	24
V_o [V]	24	48
f_{sMin} [kHz]	40	40
f_{sMax} [kHz]	320	420
P [W]	±50	±100
Inductance [µH]	69.6, RM8, N97, EPCOS. Litz wire 0.3mm. 97 turns	33, SER2918H-333KL. Coilcraft
Output capacitance [µF]	445	450
Transistors	TPH7R006PL, Toshiba 60V, 60A, 8.9mΩ, 302pF	
Switch driver	ISL6700, Intersil	
Current sensor	CQ-3200. Hall-effect. AKM Semiconductors	

The current sensor is a critical point in this kind of controls. The current measurement should be both accurate and noise-free to keep the ZVS condition and to regulate the output voltage. Hence, the selection and implementation of the current sensor becomes a key design aspect. For this work, a CQ3200 Hall effect current sensor [13] is chosen due to three main reasons. First, this sensor does not require any additional circuitry, saving cost and volume and reducing the component count.

Second, this current sensor incorporates an offset to measure the bidirectional current flow. This avoids the use of symmetrical power supply voltages across the whole control circuit. Finally, this sensor has a bandwidth of 1MHz, which is considered enough to reproduce the triangular inductor current.

However, this bandwidth may cause that the current sensor will slightly clip the peak and valley measurements of the current. This clipping is more significant for larger values of i_L and should be accounted for when setting the clamping voltages for I_{ZVS} and $-I_{ZVS}$. In both prototypes, potentiometers are used to compensate this clipping effect and to adjust $\pm I_{ZVS}$ values to ensure that the converter is always working properly under ZVS regardless of the sensor effect. The use of an embedded current sensor could minimize this clipping effect, if the whole controller was implemented in a single IC. Another possibility is to use an extremely high bandwidth current sensor; however, the increase in the cost should be taking in to account before addressing this solution. A third option could be the implementation of a dynamic estimator, which could vary the clamping voltages according to the processed power and the clipping effect. Nevertheless, this solution is even more complex and expensive and it is not recommended for cost sensitive applications.

A detailed schematic circuit is shown in Fig. 5 for the buck converter prototype. A rail-to-rail operational amplifier (LT6220) is used for implementing the type-II compensator as a voltage loop. The output of this operational amplifier is clamped as it was mentioned before, using two simple potentiometers (P_1 and P_2). These voltages stablish the upper and lower bounds for the current. The inductor current is measured by using the said CQ3200 Hall effect current sensor. The signal provided by this current sensor is then compared with the upper and lower bounds by means of two rail-to-rail fast comparators (LMV7219). After the comparators, the latch is implemented using two NAND gates (model SN74LVC1G00). The Q signal is, for this buck converter, the magnetizing control signal, and the complementary one is the demagnetizing control signal. The dead-times are constant and they are set by a simple RC network; both R_{td} and C_{td} values are calculated for the needed dead-time to achieve ZVS; a pull-down resistor (R_{pd}) is also added for avoiding noise. A generic half-bridge driver (ISL6700) is employed for properly driving both MOSFET transistors. It should be noted that the magnetizing control signal is connected to the gate of S1 transistor (i.e. the main transistor in source mode, HO output) and the complementary one is connected to S2 (i.e. to the synchronous rectifier in source mode, LO output). Finally, and auxiliary power supply is employed to obtain the driving voltage (10V) and the voltage needed for the control stage (5V).

In case of the boost converter prototype, the detailed schematic is almost equal for that employed in the buck converter. Two small differences must be pointed out. The first one is that the magnetizing and demagnetizing control signals are crossed when compared to the buck converter. Therefore, for the boost converter the Q output of the latch should be connected to the LI input of the driver, because the main transistor in source mode (S_1) is now referred to ground in this converter. Complementary, the demagnetizing control signal is connected to HI input of the driver, because the synchronous rectifier in source mode (S_2) is floating. The second difference is obvious: the type-II compensator is different when compared to the previous buck converter. These two differences only depend on the power stage topology used and they only affect to the connection of the driver. The proposed control stage remains the same for both cases. Both prototypes can be seen in Fig. 6, buck in Fig. 6(a) and boost in Fig. 6(b).

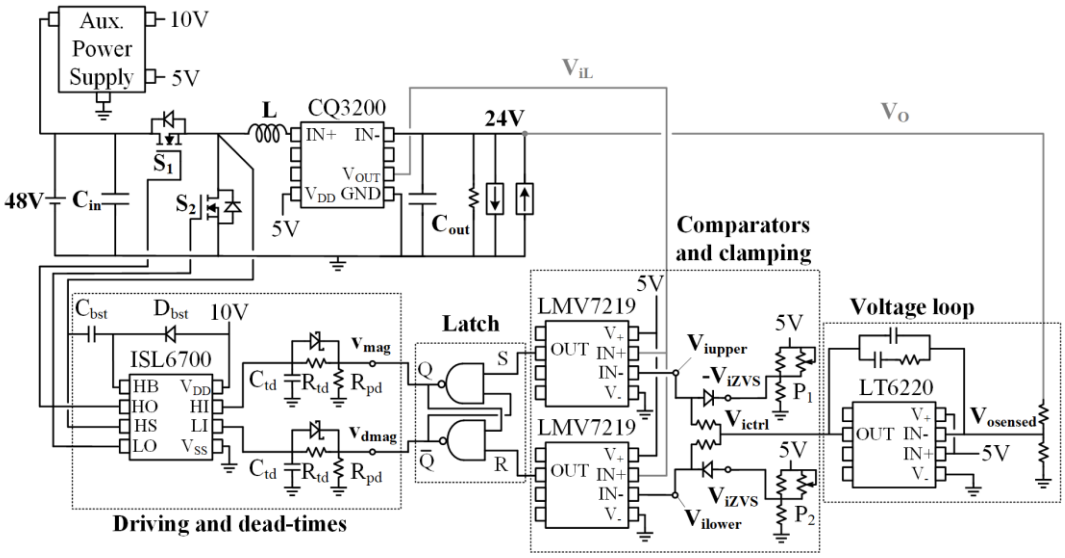
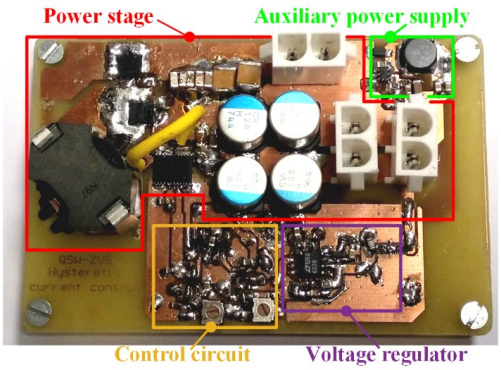
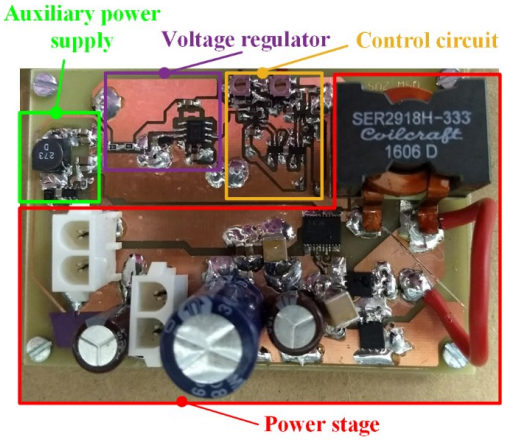


Fig. 5. Detailed schematic for buck converter prototype.

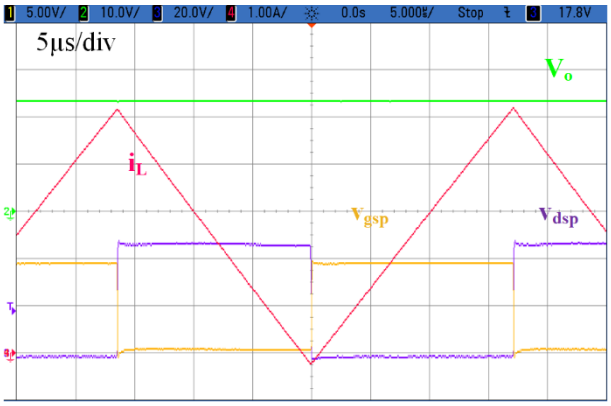


(a)

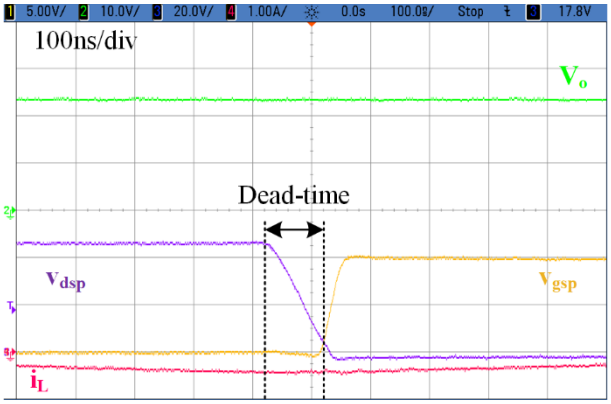


(b)

Fig. 6. Pictures of both prototypes. (a) Buck converter. (b) Boost converter.



(a)



(b)

Fig. 7. Buck converter measured waveforms at 50W. CH1: Gate-to-source voltage (5V/div). CH2: Output voltage (10V/div). CH3: Drain-to-source voltage (20V/div). CH4: Inductor current (1A/div). (a) 5µs/div. (b) 100ns/div.

B. Experimental measurements

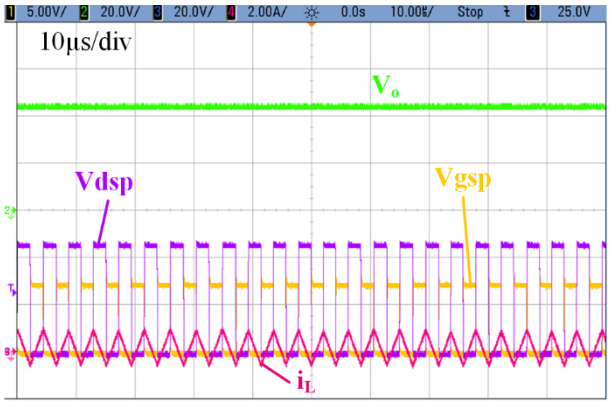
For the results shown in Fig. 7, the buck converter operates in steady state while processing 50W in source mode. the gate-to-source and drain-to-source voltages of the main power MOSFET are shown in both waveforms. In Fig. 7(a) it can be seen how i_L closely matches the expected waveform when operating at full load. With an output current of 2.08A, the maximum value of i_L is slightly above 4A and its minimum is about 200mA. Due to the manual adjustment required with this implementation, the exact desired value of $-I_{ZVS}$ is not reached and the switching frequency is close to but slightly lower than the expected 40kHz. However, this does not significantly affect the correct operation in QSW-ZVS and the measured efficiency in this operating point is 95.5%.

The same conclusions can be extracted for the operational waveforms of the boost converter. In this, two different captures of the main waveforms are shown in Fig. 9. Once again, the gate-to-source and drain-to-source voltages correspond to the main MOSFET. In this case, these waveforms are measured at two different power levels, in order to show how the control guarantees the QSW-ZVS operation in the whole power range. More specific, in Fig. 9(a) the boost converter works at 10W whilst in Fig. 9(b) it provides 100W to the passive load. As in the case of the buck prototype, the proposed controller keeps the boots converter properly working in QSW-ZVS, as can be seen in the close-up depicted in Fig. 8. Even with the variation of the output power level, the control ensures the valley current through the inductor, achieving full ZVS during the turn-on, as can be seen in Fig. 8(a) at 10W and in Fig. 8(b) for 100W.

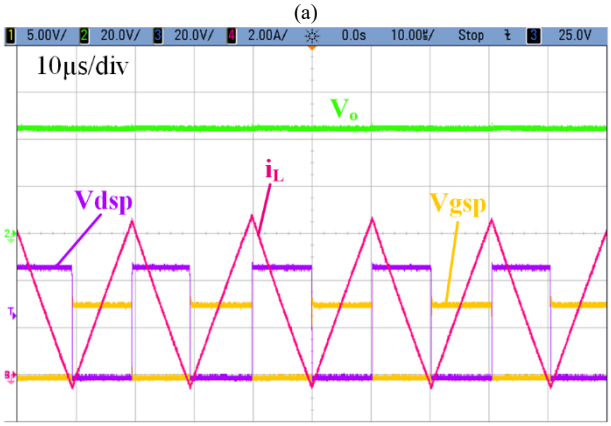
The converters used for testing this control have not been optimized in terms of overall losses. However, the obtained efficiency is high enough due to the operation in QSW-ZVS. The measured efficiency of the buck converter peaks a maximum value of 96.48% at 25W approximately. On the other hand, the efficiency of the boost converter is slightly different in comparison with the previous one. This is mainly to the different design considerations made and the used of different inductance value, materials and components. In particular, this measured reaches a maximum of 97.75% at 28W. Then, it slowly drops to 95% at full load. It should be noted that both efficiencies are measured taking into consideration the control and driving power consumption.

Fig. 10 shows some dynamic behavior of the proposed control under different source and sink mode transitions. For simplicity, only the buck converter waveforms are shown to illustrate these transitions. The zero reference is the same for all four channels. It must be noted that channels 1 to 3 have an offset of 1.65V due to the current sensor, which is indicated Fig. 10.

Fig. 10(a) shows a load step from -50W to 50W. The three operational modes can be seen in this snapshot. First, the

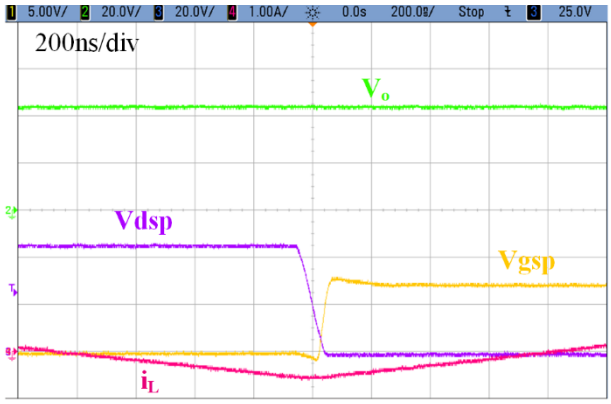


(a)



(b)

Fig. 9. Boost converter measured waveforms. CH1: Gate-to-source voltage (5V/div). CH2: Output voltage (20V/div). CH3: Drain-to-source voltage (20V/div). CH4: Inductor current (2A/div). Time scale: 10µs/div. (a) At 10W. (b) At 100W.



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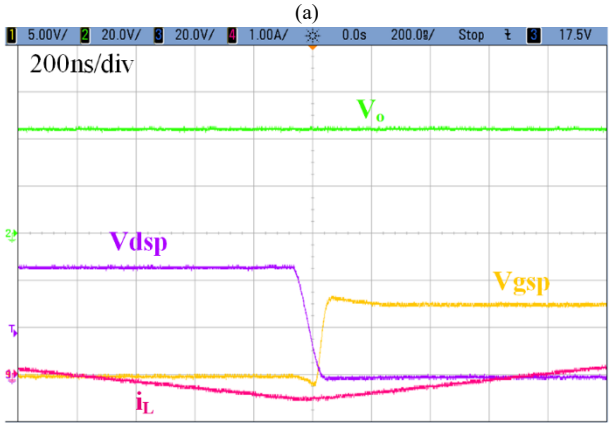


(b)

Fig. 8. Boost converter waveforms detail during the turn-on of the main MOSFET. CH1: Gate-to-source voltage (5V/div). CH2: Output voltage (20V/div). CH3: Drain-to-source voltage (20V/div). CH4: Inductor current (1A/div). Time scale: 200ns/div. (a) At 10W. (b) At 100W.

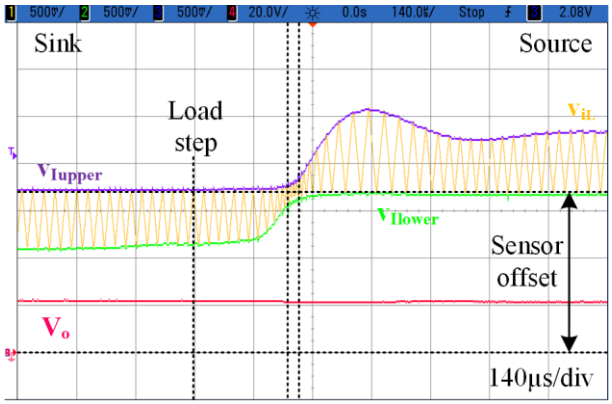
inductor current is negative and the converter is operating in sink mode. Its upper bound is V_{IZVS} and its lower bound is V_{Ictrl}. Shortly after the load step, V_{Ictrl} increases, reducing the width of the hysteresis band and the inductor current valley. When V_{Ictrl} approaches zero, no current is transferred to any port and the hysteresis band is defined by V_{IZVS} and $-V_{IZVS}$. At this point, the converter operates at the maximum switching frequency. As V_{Ictrl} continues increasing, it goes over V_{IZVS} and keeps enlarging the width of the hysteresis band, increasing the inductor current peak to enter source mode and provide the required current to the load. The control loop has a relatively small phase margin, around 55º. Due to this, a small overshot can be seen in V_{Iupper}. This slow loop was set in order to see clearly all the transitions. In spite of this limited dynamics, it can be seen that V_o does not change significantly.

Fig. 10(b) shows a transition when a passive load is disconnected, more precisely when the output power goes from 50W to 0W. Once again, it can be seen how the converter operates in three modes. First, the converter is working in source mode with a positive average inductor current. Shortly after the load step, V_{Ictrl} decreases, and for a few switching cycles there is no net power transferred in any direction. Ideally, the converter should stay in this mode until a load (either passive or active) was connected again to the output bus. However, the control loop has to compensate the offset in the output voltage caused by the load disconnection. The extra charge stored in the output capacitor of the converter is transferred back to the input source and the converter enters in sink mode with a slightly negative current.

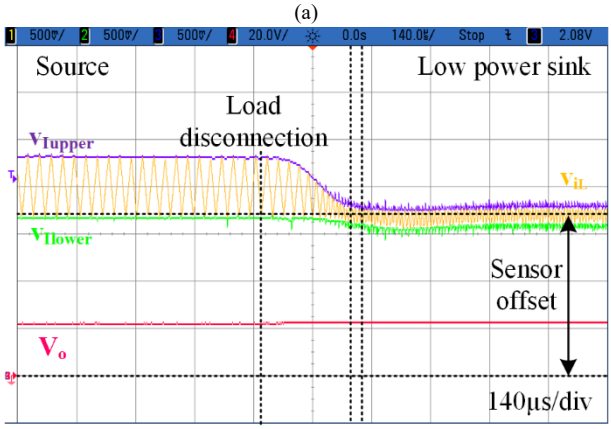
Finally, the same waveforms are depicted in Fig. 11 when the converter works with no load (i.e. processing 0W). Despite the fact that the output voltage is being regulated and the inductor current is kept within the upper and lower bounds, it can be seen the effect of the noise in the proposed control circuitry. While the current measurement is rather clean, both V_{Ilower} and V_{Iupper} have some spikes and harmonics related to the switching frequency noise. This issue can be mitigated by integrating the control stage in a single IC and with an optimized Printed Circuit Board (PCB) layout taking into account these noise-sensitive paths.

IV. Conclusions

In this work, a simple, analog, control circuit for a QSW-ZVS source/sink converters has been presented and its principle of operation has been demonstrated with two different power converters. The proposed analog control is based on a HCMC controller. The control stage has low component count (a latch, two comparators, a clamping circuit a dead-time generation and a gate driver stage). It allows to regulate the output voltage while keeping ZVS operation and simultaneously adapting the switching frequency to the load. The proposed control also has a



(a)



(b)

Fig. 10. Dynamic behavior of the QSW-ZVS source/sink buck converter: (a) load step from -50W (sink) to 50W (source) (b) load step from 50W (source) to 0W. CH1: Measured inductor current, v_{iL} (500mV/div). CH2: Lower hysteretic bound, v_{Ilower} (500mV/div). CH3: Upper hysteretic bound, v_{Iupper} (500mV/div). CH4: Output voltage (20V/div). Time scale: 140µs/div.

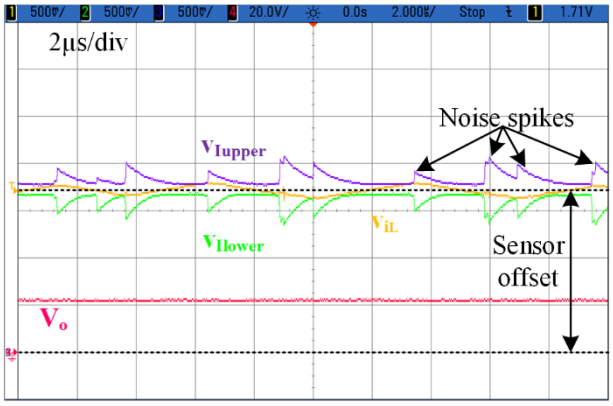


Fig. 11. Steady-state operation of the QSW-ZVS source/sink buck converter at 0W, showing the control commands. CH1: Measured inductor current, V_{iL} (500mV/div). CH2: Lower hysteretic bound, V_{Ilower} (500mV/div). CH3: Upper hysteretic bound, V_{Iupper} (500mV/div). CH4: Output voltage (20V/div). Time scale: 2µs/div.

seamless transition between source and sink modes and it can work even at no load.

On the other hand, the proposed control is highly dependent on the current sensor. A high-bandwidth and highly linear current sensor is mandatory for this controller if no distortion in the inductor current nor voltage spikes were permitted. Nevertheless, part of these problems can be minimize if an integrated circuit is used instead of discrete elements.

While the proposed control circuit offers basic functionality, it can be used as a core building block for enhanced implementations including features such as variable dead-times or additional control loops (e.g. voltage droop control or current limiting), due to the flexibility on the hysteretic band. Finally, the extension of this analog controller for multi-cell QSW-ZVS converters with current sharing and interleaving technique should be addressed in future works.

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