Flexible and Fault Tolerant Distributed Control Structures for Modular Power Electronic Transformers

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Abstract—**This paper addresses the design and implementation of distributed control structures for Modular Power Electronic Transformers (PETs). Medium voltage modular PETs are characterized by a large count of controlled power devices (easily in the range of hundreds or even thousands) and strict isolation requirements, both between modules in the high-voltage side and between the primary and secondary sides of each module as well. Due to this, distributed control structures have significant advantages compared to centralized ones. However, design of the distributed control structure is not trivial. Energization and start-up of the PET, as well as the required reconfigurations in the event of a module failure, to maintain the PET operative, can be especially challenging in this case. This paper discusses potential flexible, fault tolerant distributed control structures for modular PETs. Performance of the proposed solutions is verified experimentally.**

Keywords—Power electronic transformer, distributed control, fault tolerance.

I. INTRODUCTION

Power Electronic Transformers (PETs), also known as Solid State Transformers (SSTs), are envisioned as an evolution of Line Frequency Transformer (LFTs) [1], capable of providing substantially improved functionalities aside from reduced volume and weight, thanks to the use of controlled semiconductors [2]. PETs can indeed act as enabling technology for specific applications in traction, off-shore and future grids among other [3], [4].

Several PET topologies have been proposed, selection mainly depending on application requirements [5], [6]. Modular multilevel topologies are especially appealing for medium and high voltage applications, due to their scalability and intrinsic redundancy. Modular PET pile-up identical modules of relatively low voltage, to provide much higher terminal voltages.

Regarding modular PET operation, the analysis during normal operation has been thoroughly studied in the literature [7], [8]. However, there are two special modes of operation which have received little attention, still they can be critical determining the functionalities and performance of the PET: 1) Energization and start-up, and 2) reconfiguration of the PET in the event of a module failure (assumed redundancy is implemented).

Regarding SST design, two aspects will be critical in this case: 1) Selection of Auxiliary Power Supply (APS) needed to feed the auxiliary electronics of each module (drivers, sensors, local control …) and 2) design and implementation of the control structure. Either centralized or distributed solutions can be used in both cases. Aspects to be considered for the selection between centralized/decentralized options include: 1) APS complexity and isolation requirements; 2) Control hardware complexity; 3) Difficulties/flexibility during energization and start-up; 4) Difficulties/flexibility for the reconfiguration in the event of a module fault.

Table I summarizes the main characteristics and challenges for different configurations. It is observed from this table that the use of distributed APS along with a distributed control structures enormously simplifies the complexity (and cost) of the hardware. However, this is at the price of higher complexity during energization and

TABLE I.   CENTRALIZED VS DISTRIBUTED SOLUTIONS

		Auxiliary power supplies (APS)	
		Centralized	*Distributed*
Control	*Centralized (one central controller)*	✓ Energization and start-up: easy (independent of external grids configuration) ✓ Reconfiguration in the event of module failure: easy ✗ APS design: difficult due to isolation requirements ✗ Not fully modular (not directly scalable) ✗ Central control computational requirements: large ✗ DIO[a] and OF[b] count for the central control: large	✗ Energization and start-up: not trivial (strongly dependent on external grids configuration) ✗ Reconfiguration in the event of module failure: not trivial ✓ APS design: easy (low isolation requirements) ✗ Not fully modular (not directly scalable) ✗ Central control computational requirements: large ✗ DIO and OF count for the central control: large
	Distributed (one local controller per module)	✓ Energization and start-up easy (independent of external grids configuration) ✓ Reconfiguration in the event of module failure: easy ✗ APS design: difficult due to isolation requirements ✓ Fully modular (easily scalable, except APS!) ✓ Central control computational requirements: low ✓ DIO and OF count for the central control: low	✗ Energization and start-up: not trivial (strongly dependent on external grids configuration) ✗ Reconfiguration in the event of module failure: not trivial ✓ APS design: easy (low isolation requirements) ✓ Fully modular (easily scalable) ✓ Central control computational requirements: low ✓ DIO and OF count for the central control: low

[a.] DIO stands for digital inputs/outputs of central controller
[b.] OF stands for Optical Fiber connections between central controller and module elements (drivers, error signals, sensors …)

start-up process and during the reconfiguration in the event of a module failure. Discussion of energization and start-up process in modular PETs using distributed APSs was presented in [9].

Reconfiguration of the PET in the event of a module failure (i.e. fault ride-through) is critical in many applications [10]. Recently, fault tolerance and redundancy methods for modular PETs in the case of a module failure [11], especially hot redundancy techniques, have received significant attention [12]-[14]. These techniques implicate online replacement of faulty modules with backup ones, without discontinuing PET operation, while controlling the resulting transition. However, this is not the preferred solution for temporary module faults affecting to auxiliary elements (e.g. APS output interruption or communication interruption). These faults last for milliseconds and can be efficiently tolerated and overcome if a correct ride-through procedure is implemented rather than bypassing the whole module. This is addressed by the present paper proposing a simple fault ride-through procedure to overcome these faults.

The paper also discusses different distributed control structures for modular PET based on two basic criteria: 1) flexibility during energization and start-up process, and 2) capability of reconfiguration in the event of failure of auxiliary elements of the module without discontinuing the normal operation of the PET.

The paper is organized as follows: Section II discusses the PET topology and the proposed distributed overall control structure. Section III shows the different potential options for implementing the local module controller. Section IV discusses the proposed ride-through process step-by-step and finally section V shows experimental results for riding through a worst case fault scenario applying the proposed strategy to a full-scale PET module.

II. PET TOPOLOGY AND PROPOSED CONTROL STRUCTURE

The PET topology considered in this paper is a three-stage topology, based on a Cascaded H-bridge (CHB) converter, interfacing a HVAC and a LVAC grids [9], [15] (see Fig. 1), though, the concepts being discussed can be applied to other modular configurations [15].

The AC/DC front-end converter in the HV side is a CHB modular structure. The middle DC/DC stage uses Dual Active Bridges (DABs), which provide the required isolation between HVAC and LVAC by means of a High Frequency Transformer (HFT). Each full-bridge of the CHB is connected to a DAB forming one PET module (Fig. 2). LV sides of DABs are parallelized to form a LV high current DC link. A 3-phase DC/AC converter interfaces the LVDC link with the LVAC grid.

Auxiliary electronics of each module are fed from its DC links (Fig. 2) by APS_{HV} and APS_{LV} [9].

A distributed control structure is proposed. Each PET module has an FPGA (i.e. local controller) which controls the DAB. All local controllers communicate with the central control through a communication ring based on TosNet protocol [16].
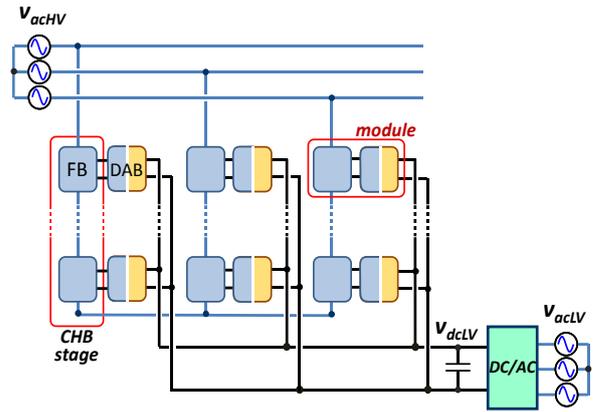
Fig. 1. Three-stage CHB based PET
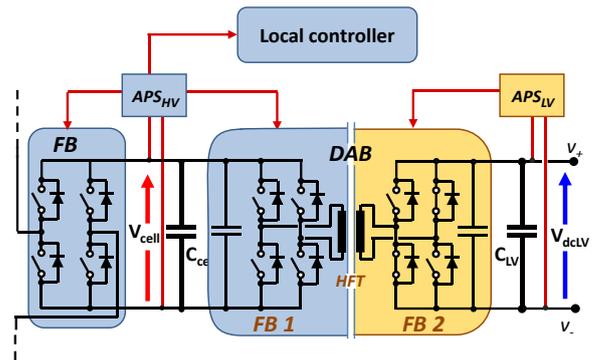
Fig. 2. PET module consisting of an HB and a DAB

The current command for each DAB is received from the central control through this ring. Voltage commands for the CHB stage are produced by the central control and transferred to the local FPGA, which is connected to the corresponding gate signal of the power devices.

Different options for the local controller and communications are discussed in the following section.

III. LOCAL CONTROLLER DESIGN

Four different structures have been considered for implementing the local controller. They are schematically shown in Fig. 3. Optical fiber (OF) signals communicating the local controller to the module hardware are grouped in blocks based on their function. Each block signals are detailed in Table II, showing the function, number and direction of each signal.

A. Single FPGA

The FPGA performing the local control is referred to the HV side, being fed therefore from APS_{HV}. All signals required to control LV side are sent/received using OF. LV side of the controller has ADCs for the module LV side measurements.

All module gate signals are sent from the FPGA to the devices through OF. However, voltage and current measurements of each side are directly connected to their corresponding ADC through cables.

Since the FPGA is powered from the HV side, energization is only possible from HV port. Energization from LV port would require re-cabling, which is not considered viable in practice.

a) Single FPGA

b) Two FPGAs, symmetrical

c) Two FPGAs, Master-Slave

d) Two FPGAs, fully redundant
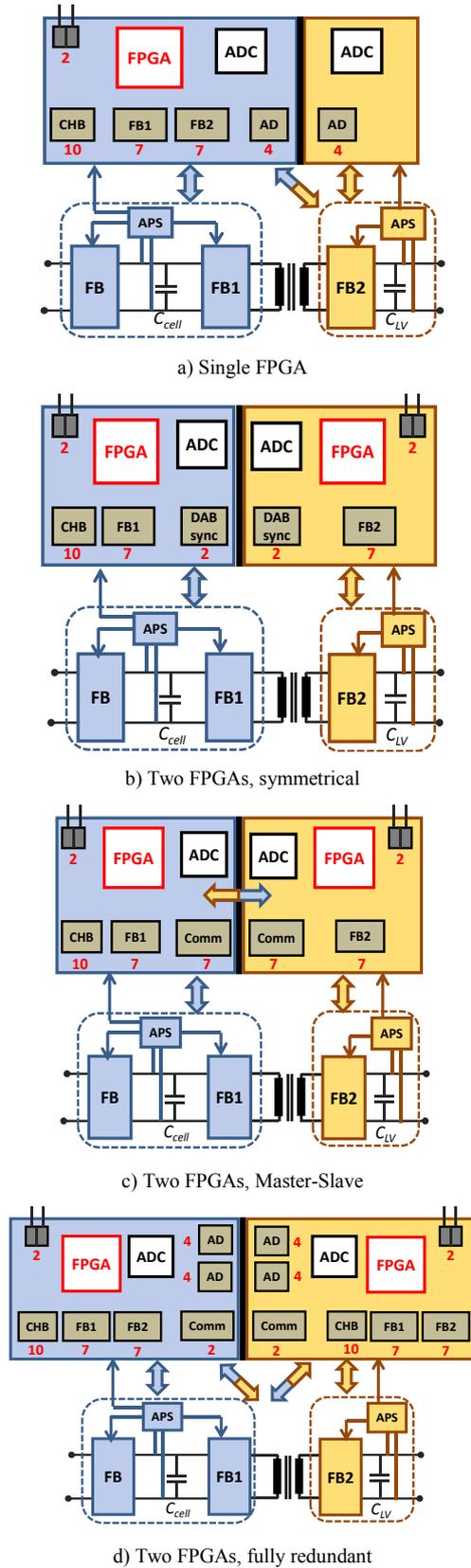
Fig. 3. PET local controller designs. OF are grouped in blocks (grey) based on their function indicating their count in red. Communication transmitter and receiver are shown on top. Arrows show signals sent/received between controller and module, same colour represents signals referred to the same reference while combined colour represents signals requiring isolation. Thin Arrows indicate cable connection while thick arrows indicate OF. Each controller is divided into two sides, HV (blue) and LV (orange), each side is fed from the corresponding APS. ADCs are also shown.

B. Two FPGAs, symmetrical

To enable energization from both sides of the PET, HV and LV sides of the controller can be made symmetric by using an FPGA on each side. Each FPGA controls the devices of its side of the module through a dedicated communication ring connected to the central control. Two communication rings are therefore required. An additional synchronization signal communicating both FPGAs is required for DAB control.

The only difference between both sides, in hardware as well as in the tasks carried out by both FPGAs, would be the CHB control signals. The FPGA at the HV side is responsible for the control and protection of the CHB full bridge. It receives through its communication ring the corresponding information and sends gate signals to the CHB devices through OFs.

C. Two FPGAs, Master-Slave

It is similar to previous option but both FPGAs now communicate locally. One works as Master. It receives commands through its communication ring, controls the power devices on its side of the module and sends the signals required by the Slave FPGA to control power devices on its side of the module.

Due to the local communication link between both FPGAs, on the one hand, this option provides redundancy in the communication ring. In case of communication breakdown with the Master FPGA, the central control enables the Slave FPGA communication ring. In this case, FPGAs switch roles, but PET operation remains unaffected. However, the OF count is higher than for the previous two options.

D. Two FPGAs, fully redundant

In this option, each side of the controller is able to control all the module devices completely independent of the other side. Each side has its own FPGA and ADCs, both FPGAs communicate internally. All OF/signals are duplicated to provide full redundancy.

TABLE II. LOCAL CONTROLLER OF SIGNALS

Block	Signal Function		No.	i/o FPGA
CHB (x10)	Full Bridge gate signals		4	Out
	CHB Enable		1	Out
	Pre-charge contactor		1	Out
	CHB driver Fault		2	In
	CHB driver Reset		2	In
FB1 FB2 (x7)	DAB Full Bridge 1 gate signals		4	Out
	Driver Fault Signal		1	In
	Driver Reset signal		1	In
	Driver Ready signal		1	In
DAB sync (x2)	Synchronization Transmitter/Receiver		2	Inter-FPGAs signal
Comm (x7)	DAB sync	Synchronization Transmitter/Receiver	2	Inter-FPGAs signal
	Data Transmitter/Receiver		2	
	CHB synchronization		1	
	Fault/Status Transmitter/Receiver		2	
AD (x4)	Data		2	In
	Chip select (CS)		1	Out
	Clock (CLK)		1	Out
Ring (x2)	Communication ring Transmitter /Receiver		2	Central-local signal

TABLE III. COMPARISON BETWEEN LOCAL CONTROLLER OPTIONS

	a) Single FPGA	b) Two FPGAs, symmetrical	c) Two FPGAs, Master-Slave	d) Two FPGAs, fully redundant
OF count	34	32	42	72
Redundant controller	No	No	No	Yes
Redundant communication ring	No	No	Yes	Yes
Start-up from both ports feasible	Requires Re-cabling	Yes	Yes	Yes

This option shows the highest reliability, but this is at the price of the highest hardware requirements.

Main properties of the four implementations are summarized in Table III. With option (a) the PET can be energize only from one side. Option (b) solves this issue, also providing the lowest OF count, however in both options redundancy is compromised due to the communication ring. If this ring fails, the PET has to be stopped. Option (c) solves this issue using a moderate OF count. Finally, option (d) provides the highest redundancy, but this is at the cost of a significant increase in OFs.

It can be concluded that the design of the local controller determines operation-critical characteristics of the full PET. Therefore, this design is totally dependent on the application requirements based on the priority. It is clear that there is a trade-off between reliability and hardware complexity, and eventually cost.

From this analysis based on the discussed PET application, option (c) is selected as it allows energization of the PET from both sides and provides a good trade-off between redundancy and OF count.

IV. MODULE LOCAL FAULT RIDE-THROUGH USING A TWO-FPGAS MASTER-SLAVE CONFIGURATION

There is a number of events which can produce a module fault. Faults affecting to power elements (semiconductors, drivers, DC-link capacitors), will force to by-pass the module. However, certain faults affecting to auxiliary elements, can be overcome without discontinuing the operation of the PET.

The selected control topology (option (c) in Fig. 3c) can overcome two fault situations without disconnecting the module:

1. Communication ring faults, both transitory and permanent type failures (thanks to the redundancy of the communication ring)

2. External or internal transient events causing APS temporary malfunction.

A worst-case fault scenario can be defined as a fault with consequences leading to enough cell capacitor voltage drop to make APSs switch off and eventually all module electronics are not powered. This is considered the most challenging case for two reasons: (1) the module

power devices becomes uncontrolled and only the diodes conduct blocking the power transfer through the module which implicates disconnecting the PET from the grid, and (2) once fault is cleared, the ride-through process has to re-energize and start-up the module with no monitoring or control (i.e. the FPGA and communication ring are not powered) [9]. The reconfiguration process when a fault of this type occurs must be therefore carefully designed.

The previously mentioned fault situations are discussed in this section. For each fault situation, causes and consequences of the fault on the module and the PET are discussed, the worst-case scenario being identified. Finally a step-by-step process for automatic fault ride-through is proposed for this scenario.

The following operation conditions for the PET are considered:

- PET is energized from the LV port.

- Master FPGA is the LV side one.

- CHB is transferring maximum active power to the HV grid, which is the most adverse condition as it results in faster discharge of the cell capacitor and eventually in the highest risk of an unexpected APS turn-off.

A. Communication ring faults

Communication ring faults can be either transitory or permanent.

The cause of transitory faults can be a temporary loss of power of the OF connectors at either end (i.e. transmitter or receiver) or a misconfiguration of central or local FPGA controllers, e.g. due to switching noise. On the other hand, the cause of a permanent communication fault can be a physical disconnection/break down of the OF cables.

In both fault cases, the consequences can vary from a slight voltage drop to a total discharge of the module DC-link capacitors (C_{cell} and C_{LV}) leading to switch off of the APSs and eventual loss of power in the full module. These consequences are totally dependent on the time from the instant a fault is detected till normal operation is recovered. In case of transitory fault, this time depends on the fault duration and the speed of the ride-through procedure. On the other hand, for a permanent fault, it would also depend on the time required to switch between both rings, resulting therefore in a higher total reconfiguration time than the transitory case.

Based on the previous, worst-case scenario can be defined as a permanent fault causing enough voltage drop in the capacitors to switch off the APS as this would be the most challenging scenario to reconfigure.

The latter scenario is considered, where the master communication ring fails permanently and causes APS_{HV} to switch off. Fig. 4 shows the proposed automatic reconfiguration/ride-through procedure which can be divided into seven events as follows:

(1) Fault starts. Communications failure is detected by Master FPGA and Central control. Master FPGA disables DAB and V_{cell} starts discharging. Central control attempts to recover Master ring. No response is

detected (i.e. permanent failure is considered) and consequently central control starts using Slave communications ring. FPGAs switch roles.

(2) V_{cell} drops below APS threshold causing APS_{HV} output voltage to decrease.

(3) Minimum CHB supply voltage is reached, and CHB is disabled. V_{cell} discharge rate is decreased.

(4) Fault state is cleared once communication is recovered, since APS_{LV} is ON, the re-boot procedure is automatically started. FB2 is enabled charging V_{cell} through FB1 diodes.

(5) V_{cell} reaches APS_{HV} threshold voltage, a delay is noticed before APS_{HV} output becomes active (i.e. t_{APS}).

(6) APS_{HV} output is active, a delay is again noticed till CHB is powered and enabled (i.e. t_{CHB}).

(7) CHB is enabled, normal operation is resumed.

B. Auxiliary power supply temporary malfunction

APS temporary malfunctions are identified as a temporary loss of APS output power causing power off of module electronics. There are several causes for APS malfunction, these include:

- Voltage sags at one of the PET terminals. This is a very common grid event [17]. This causes a voltage drop in the cell voltage. If the cell capacitor voltage drops below the input threshold voltage of the APS, it causes one or both APSs in the module to temporarily switch off.

- A fault in the communication ring and the transient during its reconfiguration procedure may cause disruption of the local controller operation affecting the control of the DC-link capacitor voltages.

- Voltage drop in the APS output capacitor voltage due to internal module transients e.g. transients caused by devices at the switching instants.

The consequences of a temporary APS malfunction is dependent on the APS location with respect to the energization port or primary module side (i.e. LV port, as previously assumed, see Fig. 2).

On one hand, if the fault happens to APS_{HV}, it results in losing control over CHB full-bridge power devices and their parallel diodes block the power transfer to the load. Since no active power would be supplied by the module, the cell capacitor rate of discharge significantly slows down allowing for relatively faster ride-though and fault recovery process.

On the other hand, a malfunction of APS_{LV} blocks power transfer to the secondary side. However, since APS_{HV} is operating normally, CHB devices are switching and active power transferred to the load causes the cell capacitor to discharge rapidly before eventually APS_{HV} switches off. In this case, cell capacitor (C_{cell}) is discharged and reconfiguration would implicate re-energizing the cell first (i.e. pre-charging cell capacitor). Therefore, this is considered as the worst-case scenario.

Consequently, the case presented here is a transient fault affecting APS_{LV} output voltage.

Similarly, Fig. 5 shows the proposed automatic reconfiguration/ride-through procedure which can be divided into eight events as follows:

Fig. 4. Automatic communication ring fault ride-through scheme. Fault duration is highlighted in red.
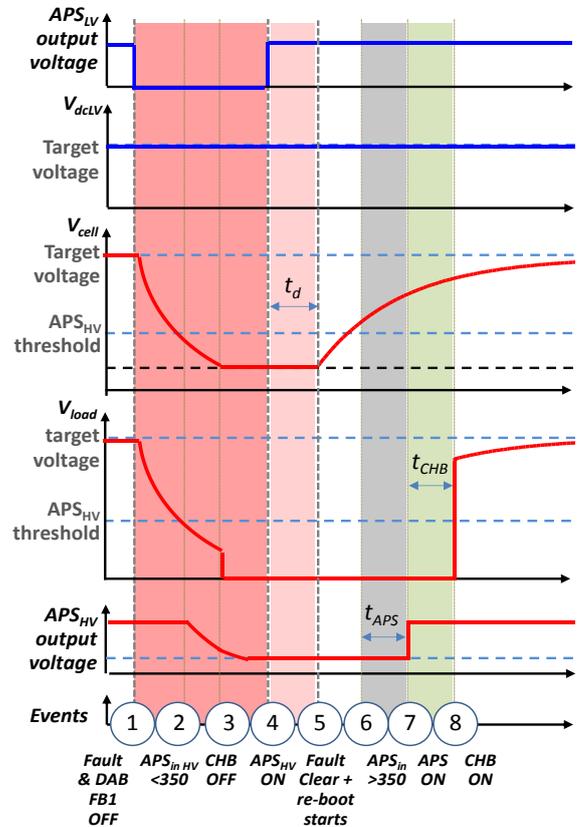
Fig. 5. Automatic APS fault ride-through scheme. Fault duration is highlighted in red.

(1) APS_{LV} output is zero powering off all LV side of the controller. Master communication ring is disabled which is detected by central control. Master FPGA loses power disabling gates of DAB FB2 and stopping power transfer to the HV side. V_{cell} starts discharging.

(2) V_{cell} drops below APS threshold causing APS_{HV} output voltage to decrease.

(3) Minimum CHB supply voltage is reached, and CHB is disabled. V_{cell} discharge rate is decreased.

(4) APS_{LV} output is recovered, Master FPGA and communication ring are powered which is detected by central control and finally Fault state is cleared. t_d represents the time period from APS_{LV} recovery till fault clearance.

(5) The re-boot procedure starts automatically.

(6) V_{cell} reaches APS_{HV} threshold voltage.

(7) APS_{HV} output is active.

(8) CHB is enabled, normal operation is resumed.

This section described two cases of faults the selected control structure can tolerate and ride-through automatically. However, the proposed procedure is valid and can be applied for riding through any type of fault tolerated by all the presented local controller structures.

V. EXPERIMENTAL RESULTS

The proposed methods have been tested on the PET module, shown in Fig. 6. As shown in the corresponding schematic in Fig. 2, it is composed of the DAB full bridges, FB1 and FB2, which are built using 1.2 kV discrete SiC ROHM devices (SCH2080KE). These are driven using commercial Wolfspeed 2-channel drivers (CGD15HB62P1). Boards are designed to send/receive the driver signals between each bridge and the local module controller [18]. The full bridge of the CHB is built using 1.7 kV Infineon non-commercial Si IGBTs packaged with SiC diodes. Infineon commercial 2-channel drivers are used. The local controller board is designed based on a Xilinx Spartan 3E FPGA. It includes a PROM, a JTAG to program the PROM and the FPGA, all required OF, ADCs, connectors for receiving measurement signals from the voltage and current sensors, etc. The primary and secondary side of the local controller are isolated to maintain the required PET isolation (i.e. in this case 24 kV). This isolation is achieved using slots which are designed based on the required creepage and clearance distances. Each module has a front panel board showing the state of all the internal voltage sources, the communication ring and different faults. The main module characteristics are highlighted in Table IV.

Experimental results are presented for the case of communication ring fault ride-through. Fig. 7 shows the results for the worst scenario, in which the fault causes enough voltage drop in V_{cell} to switch off APS_{HV}. A fault is provoked at (1), gate signals of FB1 and FB2 are disabled, and APS switch off at (3). From the time gap between (1) and (3), it is possible to estimate the maximum fault duration to avoid APS switch off, which is 100 ms in this case. It is important to notice that when fault is cleared at

(4), HV side is not powered (i.e. APS_{HV} still off), only FB2 gates are enabled and V_{cell} charges through FB1 diodes.

Practically, the time required to switch between Master and Slave rings is estimated to be in the range of 0.5 ms being possible to ride-through a communication failure without discontinuing the module operation or disconnecting PET from the grid.
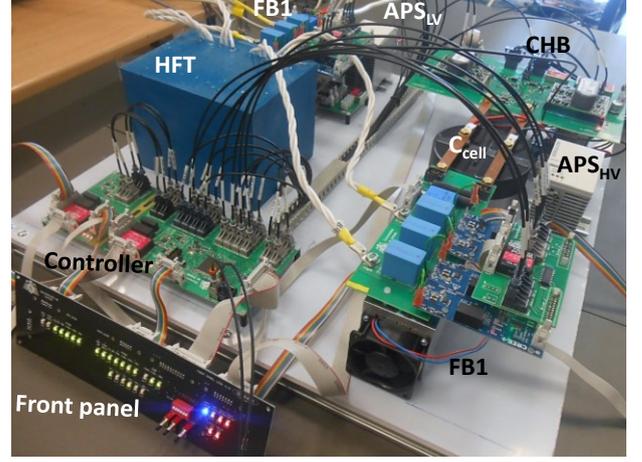
Fig. 6. CHB-based PET module prototype.

TABLE IV. PET MODULE SPECIFICATIONS

DAB	
Switching frequency	30 kHz
HFT isolation	24 kV
HFT turns ratio	1:1
CHB	
Switching frequency	5 kHz
V_{cell}	800 V
C_{cell}	600 µF(film)
APS	
Input voltage	800 V
Output voltage	24 V
Threshold (turn-on)	350 V
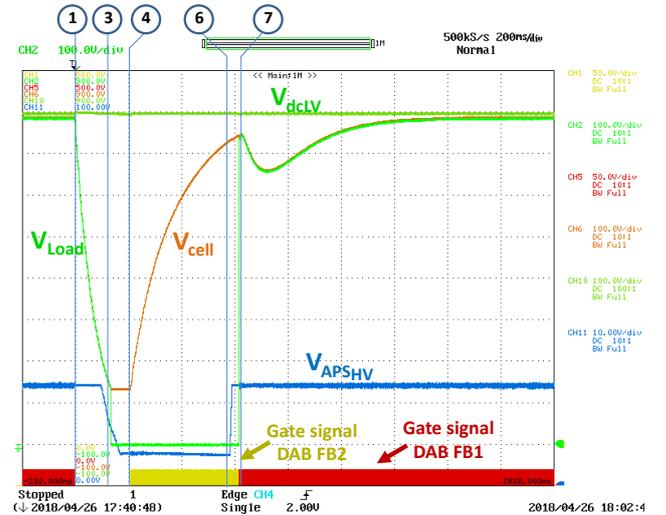
Fig. 7. Experimental Results. Automatic fault ride-through. Numbers shown on top correspond to Fig. 4.

VI. CONCLUSIONS

This paper analyses distributed control structures for modular PETs. Using distributed control and distributed (local) APSs is cheaper and simpler compared to centralized solutions. However, this results in additional difficulties during PET energization and start-up process, as well as for the fault tolerance capabilities in case of failure of auxiliary elements of the modules.

Several local controller structures are proposed. Selection being mainly dependant on the energization, redundancy and fault ride-through requirements intrinsic to each application. The selected local controller structure achieves a reliable PET energization and start-up from any port with the ability to alter the port instantaneously and provides redundancy to communication ring.

A ride-through strategy capable of automatically recovering in the case of failure has also been proposed. It is characterized by its simplicity and effectiveness without the addition of any extra hardware. It was analysed for two possible module faults; APSs transitory faults and communication ring faults. However, it can be extended for any type of transient module fault.

The proposed procedure is applied to a full-scale PET module in the case of communication ring fault. Experimental results validates the ability of the module to automatically ride-through the fault in the worst-case scenario where the module loses power.

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