

Article

Analysis of Intrinsic Switching Losses in Superjunction MOSFETs Under Zero Voltage Switching

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Abstract: Switching losses of power transistors usually are the most relevant energy losses in high-frequency power converters. Soft-switching techniques allow a reduction of these losses, but even under soft-switching conditions, these losses can be significant, especially at light load and very high switching frequency. In this paper, hysteresis and energy losses are shown during the charge and discharge of the output capacitance (C_{OSS}) of commercial high voltage Superjunction MOSFETs. Moreover, a simple methodology to include information about these two phenomena in datasheets using a commercial system is suggested to manufacturers. Simulation models including C_{OSS} hysteresis and a figure of merit considering these intrinsic energy losses are also proposed. Simulation and experimental measurements using an LLC resonant converter have been performed to validate the proposed mechanism and the usefulness of the proposed simulation models.

Keywords: soft-switching; Superjunction MOSFET; LLC resonant converter; zero voltage switching; C_{OSS} hysteresis; C_{OSS} intrinsic energy losses

1. Introduction

During the last 15 years, the acceptance of resonant converters in the industry application market has been massive, especially regarding adapters, flat panel TVs, electric and hybrid vehicle (EV/HEV), datacenters, and photovoltaic (PV) inverters, among others [1–3] (Figure 1). Besides, new markets and research centers are focusing on moving to higher frequencies to obtain further advantages and gaining power density, taking the present technologies in semiconductors to their physical limit. This is the case of gallium nitride (GaN) and silicon carbide (SiC) technologies, which are thought to be used in the market of resonant converters for low power and high-frequency applications, besides other well-known high-power applications.

A resonant topology operating at a high switching frequency and zero voltage switching (ZVS) provides high power density and is commonly chosen for the previously mentioned applications. The primary side power transistors used in a resonant converter must comply with high-voltage and high-frequency requirements, and need to be properly selected to provide good performance. However, the information given by the manufacturers of these transistors is not usually enough to calculate all the existing energy losses.

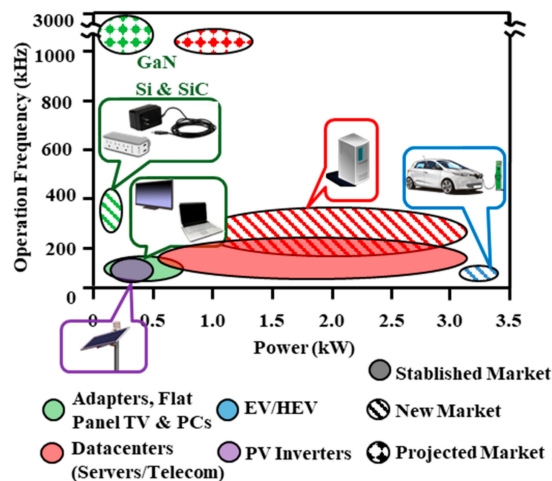


Figure 1. Markets in which resonant converters are used, for different ranges of frequencies (kHz) and power (kW). EV/HEV, electric and hybrid vehicle; PV, photovoltaic.

The parasitic output capacitance (C_{OSS}) of the power transistors has an important role in energy losses, even under ZVS conditions. Traditional switching losses models are not valid for very high switching frequencies. In the work of [4], significant energy dissipation in the process of charging and discharging C_{OSS} of Superjunction MOSFET (SJ-MOSFET) while the gate is shorted to the source is observed. In another paper [5], these intrinsic energy losses (E_i) are measured and compared in different power switches, including Silicon SJ-MOSFETs, GaN cascode, SiC cascode, and SiC MOSFETs. These E_i cannot be eliminated by using ZVS and set an upper limit for the switching frequency of the converters. Similar losses are presented in the work of [6], where energy dissipation during the charging and discharging of the junction capacitance of SiC Schottky diodes is evaluated. In the work of [7], the E_i are included for the determination of soft-switching losses of 10 kV SiC MOSFET modules. Calorimetric measurements are used to evaluate these losses (based on the charge and discharge of the C_{OSS} , and especially of the antiparallel junction barrier Schottky diode). In the work of [8], the variation of E_i with dV/dt is evaluated at very high switching frequency (1–35 MHz) in silicon (Si) and wide-bandgap active devices.

In the work of [9], these E_i are related to a significant hysteresis exhibited by the C_{OSS} of some of the most advanced SJ-MOSFETs. In a further paper [10], the physical mechanism responsible for this C_{OSS} hysteresis is briefly shown by means of mixed-mode simulations. Finally, mixed-mode simulations are also proposed to analyze E_i and the cause of the C_{OSS} hysteresis in different SJ-MOSFETs in the work of [11].

The authors of this paper have previously analyzed the C_{OSS} hysteresis and its related switching losses (including E_i) for different dead-times of three generations of SJ-MOSFETs in an LLC resonant converter in the work of [12]. Moreover, they provide a guideline to select SJ-MOSFETs of different manufacturers to improve the efficiency of this converter in a wide power range in the work of [13].

In this paper, a simple methodology is suggested to manufacturers to include information related to the C_{OSS} hysteresis and E_i of power devices in their datasheets. These data will be useful to select the optimum devices in high-frequency and soft-switching applications. Moreover, a spice model including the C_{OSS} hysteresis and a figure of merit (FoM) including E_i are proposed in Section 2 and 3, respectively. Both proposals are validated using simulation and experimental results of an LLC resonant converter in Section 4.

2. Spice Model Including C_{OSS} Hysteresis Effect

In order to design a resonant converter with low cost and high efficiency and power density, special attention is crucial during the selection of the high-voltage (~600 V) silicon SJ-MOSFET device needed.

However, even if the high-voltage SJ-MOSFETs are selected based on major vendors recommendations for soft-switching applications in resonant converters, they present different values of E_i . E_i might not seem so significant for hard-switching conditions, but it can make the difference under soft-switching operation, especially for low and medium load demands, where conduction power losses are lower and switching losses are relevant because of the high-frequency operation.

E_i is intrinsic to the structure of SJ-MOSFETs, as it is briefly reproduced in Figure 2a–c and explained in detail in the work of [12], where a physical relationship between C_{OSS} hysteresis and E_i was demonstrated, elucidating the existence of energy losses during the charge and discharge of C_{OSS} . Holes and electrons (h^+ and e^- , respectively, in Figure 2), flowing in parallel to the capacitance, originate stuck charges between the pillars that need to be removed through highly resistive paths that may vary among devices.

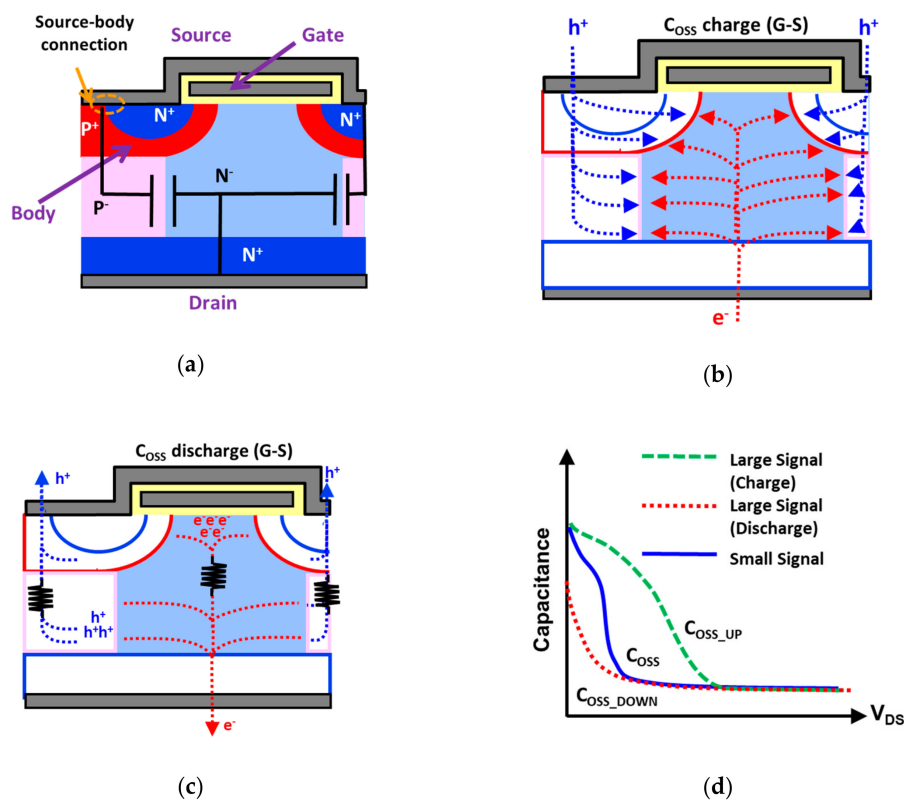


Figure 2. (a) Cross section of a Superjunction (SJ)-MOSFET basic cell. Description of (b) C_{OSS} charge and (c) C_{OSS} discharge. Electron (e^-) and hole (h^+) currents and charge pockets are indicated (red and blue). (d) Illustrative comparison between C_{OSS} extracted by small-signal (solid blue line) and large-signal (green dashed and red dotted lines).

E_i used to be neglected [14,15], but some simulation models started to consider non-linear C_{OSS} effects, and non-ZVS operation of SJ-MOSFETs [16–18]. However, C_{OSS} hysteresis discoveries are not still considered in those simulation models.

The degree of severity of C_{OSS} hysteresis varies from device to device depending on technological and geometrical features. Up to now, application notes and datasheets do not provide any information regarding this phenomenon. Besides, manufacturers only give small-signal characterization of the transistors, whereas C_{OSS} hysteresis is only detectable during large-signal analysis (Figure 2d). In order to solve this fact, a simple methodology to include in the datasheets enough information to generate simulation models predicting this behavior will be proposed.

In contrast to other reported techniques, a commercial system commonly used by power devices manufactures, an Auriga pulsed I–V system [19], is proposed. This characterization system is able to

capture measurements with very high speed and resolution (up to 0.01% of max current), and it is temperature independent. Moreover, voltage/current measurements have emerged as the preferred method of capturing different characteristics of active devices. The simple setup and the voltage and current waveforms obtained using one of the SJ-MOSFETs under test are shown in Figure 3.

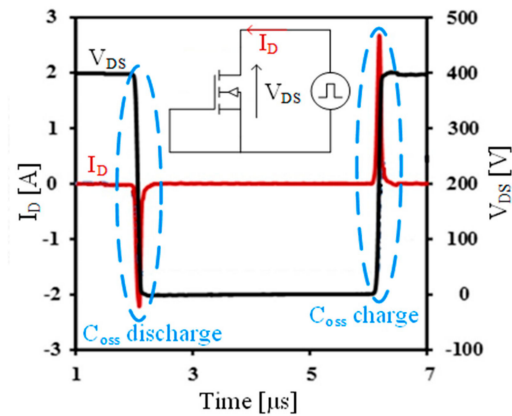


Figure 3. Auriga pulsed I–V tests: I_D and V_{DS} waveforms.

Using these voltage/current measurements, C_{OSS} large-signal curves during its charge and discharge can be inferred using

$$C_{OSS} = \frac{I_D}{\frac{dV_{DS}}{dt}}. \quad (1)$$

Following the presented procedure, C_{OSS} large-signal curves during its charge and discharge of the SJ-MOSFETs under test (Table 1) were estimated (as an example, results of device under test 1 (DUT1) are included in Figure 4).

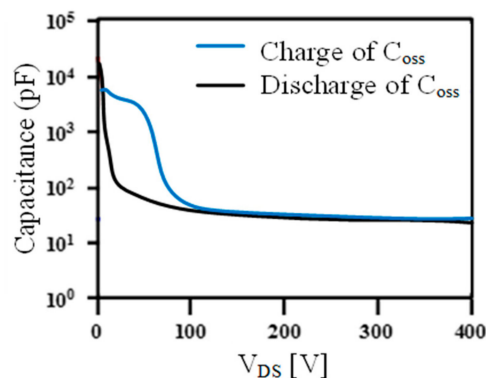


Figure 4. C_{OSS} large-signal curves of device under test 1 (DUT1) (Table 1) during its charge and discharge obtained using (1) and the Auriga pulsed I–V curves.

A detailed simulation model should include this behavior to obtain accurate simulation waveforms of the switching process. The calculated C_{OSS} could be described using a polynomial expression, but in this paper, the use of look-up-tables with pairs of values voltage-capacitance is proposed. Two different look-up-tables, one for the charge and one for the discharge, can be easily included in the spice model of the SJ-MOSFETs. This option is preferred (compared with polynomial expressions) from the point of view of saving computational time and the ease to use, follow, and change data if a different power device is chosen for simulation. The simulations results using the proposed model will be shown and compared with the experimental results in Section 4.

Table 1. List of Superjunction (SJ)-MOSFETs explicitly for LLC primary side with main electrical characteristics and figures of merit (FoMs). DUT, device under test.

DUT	Characteristics from Datasheet							FoM from Datasheet				Proposed FoM	
	R_{ON} (m Ω)	BV_{DSS} (V)	R_G (Ω)	Q_G (nC)	Q_{GD} (nC)	Q_{GS} (nC)	E_{OSS} (μ J) ⁽¹⁾	Q_{OSS} (nC) ⁽²⁾	$R_{ON} \cdot Q_G$ ($\Omega \cdot$ nC)	$R_{ON} \cdot Q_{GD}$ ($\Omega \cdot$ nC)	$R_{ON} \cdot E_{OSS}$ ($\Omega \cdot \mu$ J)	$R_{ON} \cdot Q_{OSS}$ ($\Omega \cdot$ nC)	$R_{ON} \cdot E_i$ ($\Omega \cdot \mu$ J)
1	155	600	0.9	24	8	5	2.7	140	3.72	1.24	0.42	21.64	0.049
2	168	650	0.6	60	25	12	6.4	122	10.08	4.20	1.08	20.43	0.194
3	171	600	3.4	37	13	11	4.9	106	6.33	2.22	0.84	18.03	0.116
4	165	650	6	30	13	7.4	3.6	111	4.95	2.15	0.59	18.28	0.793
5	175	600	7	29	12	6	4.6	102	5.08	2.10	0.81	17.85	0.116
6	168	600	7	29	12	6	4.1	103	4.87	2.02	0.69	17.34	0.375

¹ C_{OSS} stored energy at $V_{DS} = 400$ V. ² Output characteristic charge, result of charging C_{OSS} (time-related effective output capacitance is considered) rising from 0 to 400 V.

3. Simple Methodology to Include E_i in the Datasheets

The cumulative energy (E_{CUM}) of C_{OSS} can be calculated with the previously shown voltage and current waveforms obtained using the Auriga pulsed I–V system.

$$E_{CUM} = \int I_D \cdot V_{DS} dt. \quad (2)$$

Using (2), the energy stored during the charge and extracted during the discharge of C_{OSS} can be easily estimated. In Figure 5, an example of the value of E_{CUM} using one of the SJ-MOSFETs under test is shown as an example. As can be seen, the stored energy is higher than the extracted energy, and this difference is the value of E_i . Concretely, E_i is considered as the energy losses after applying a complete cycle of charge–discharge to the device, and consequently is directly related to C_{OSS} hysteresis.

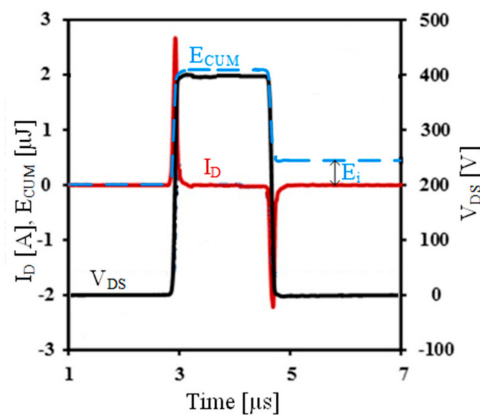


Figure 5. Auriga pulsed I–V tests: I_D and V_{DS} waveforms. Procedure to obtain the cumulative energy and the value of E_i to propose the new figure of merit (FoM).

The proposed FoM, defined as the conduction resistance (R_{ON}) multiplied by E_i , considers both R_{ON} (important for heavy loads) and E_i (crucial for low and medium loads), allowing a proper selection of SJ-MOSFETs in soft-switching applications operating at high frequencies. The lower the FoM value of an SJ-MOSFET, the higher its performance. In Section 4, the prediction of the performance of different SJ-MOSFETs using this FoM is validated with experimental efficiency results.

Besides, it is worth mentioning that, as occurring in other common FoMs, the direct and indirect proportionalities of R_{ON} and E_i with the die area result in an area-independent FoM. This is a preferred FoM approach to facilitate the benchmarking between technologies. In addition, common to other FoMs are the limitations for devices with a small die area, where the termination area could be as relevant as the active area of the transistor (R_{ON} does not perfectly scale with the die area).

4. Validation of the Proposed Simulation Model and FoM

The power supplies used in the applications mentioned in the introduction of this paper must comply with challenging standards, such as 80PLUS Titanium® [20]. An LLC resonant converter is the topology generally selected to develop this kind of power supply, mainly owing to their high efficiency and power density. More information and new models are needed to properly design these power converters operating at a very high switching frequency.

Silicon SJ-MOSFETs are the preferred devices during the design of the primary side of the LLC resonant converter as they meet the requirements regarding voltage, current, and frequency, and an accurate procedure for their proper selection for each specification is important, especially operating at a high switching frequency. The devices under test (DUT) in this work are detailed in Table 1. SJ-MOSFETs with similar voltage blocking capability, R_{ON} , and Q_{OSS} are selected in order to obtain a fair comparison under the same working conditions. In all the tests, ZVS is assured and,

consequently, differences in the value of R_G are not relevant because the switching losses were forced to be independent of R_G . Exhaustive experimental tests are carried out using an LLC resonant converter with the DUTs. Waveforms, breakdown losses, and efficiency results are analyzed and compared.

4.1. LLC Resonant Converter Description

The previously described SJ-MOSFETs were tested in a commercial evaluation board of an LLC resonant converter [21] featuring the specifications of Table 2.

Table 2. LLC resonant converter evaluation board specifications.

Parameter	Value	Parameter	Value
Primary side devices	Si SJ-MOSFETs (DUTs)	Input Voltage, V_{IN} (V)	350–410
Secondary side devices	OptiMOS BSC010N04LS	Output voltage, V_{OUT} (V)	12
Gate driver IC	2EDL05N06PF	C_R (nF)	66
Maximum power (W)	600	L_R (μ H)	15.5
Resonant frequency, f_{RES} (kHz)	157	L_M (μ H)	195
Frequency range (kHz)	90–250	Transformer turns-ratio	16:1

The fundamental requirements related to a fixed resonant tank (C_R , L_R , and L_M) and deadtimes (t_D) are fulfilled, guaranteeing the ZVS inductive mode for the whole power range and for all the transistors under examination [13]. As the devices selected share very close values of R_{ON} and Q_{OSS} , there is no need to redesign different L_M values for each transistor, reassuring ZVS the whole load range. A simplified scheme of the LLC resonant converter with the main components and the sensing methods is shown in Figure 6.

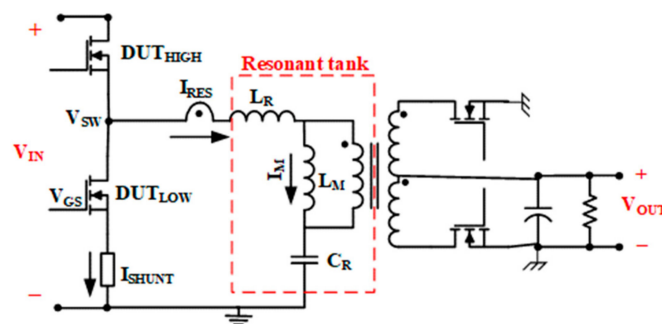


Figure 6. Simplified circuit scheme of the LLC resonant converter and sensing method.

Mixed-mode (MM) simulations were also carried out to analyze the evolution of certain signals that cannot be experimentally measured (as the current through the channel of the MOSFETs). The developed MM simulations consist of spice circuits, where the half-bridge (HB) structure of the primary side of the LLC resonant converter is replaced by TCAD (Technology Computer Aided Design) structures (finite-element structures) simulating the power transistors (DUT_{HIGH} and DUT_{LOW} in Figure 6).

Calibration of TCAD structures was done by means of process simulations in the case of own SJ-MOSFETs technologies, and by means of reverse engineering and reverse calibration technique in the case of other commercial SJ-MOSFETs technologies. Information about the doping profiles is included in the TCAD structures and data regarding voltages, power, magnetics, frequencies, and so on are extracted from the evaluation board datasheet [21].

The accuracy of the MM simulations and its good match with experimental waveforms can be seen in Figure 7. Moreover, the current through the channel of the DUT_{LOW} (I_{CH}) obtained using MM simulation (it cannot be experimentally measured) was included to verify the ZVS operation (I_{CH} falls to zero before V_{SW} is increased). As I_{CH} is zero before V_{SW} rises, the area below P_{INS} waveform

represents the energy stored in the output capacitance of the SJ-MOSFET during the turn-off (E_{off}). This energy cannot be considered as losses, because it can be retrieved in the turn-on.

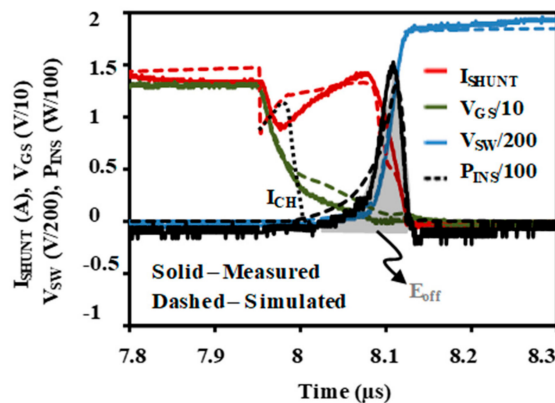


Figure 7. Simulated and measured waveforms for DUT_{LOW} during the turn-off. I_{SHUNT} , V_{GS} , and V_{SW} are referenced in Figure 6. P_{INS} is the instantaneous power (product of V_{SW} and I_{SHUNT}) and I_{CH} is the simulated current through the channel of the SJ-MOSFET.

4.2. Experimental Results, Efficiency, and Power Losses Break-Down

Several experimental measurements and waveforms are analyzed to validate the proper operation of the converter at different loads and with different DUTs. Examples of experimental waveforms measured in the converter are shown in Figure 8.

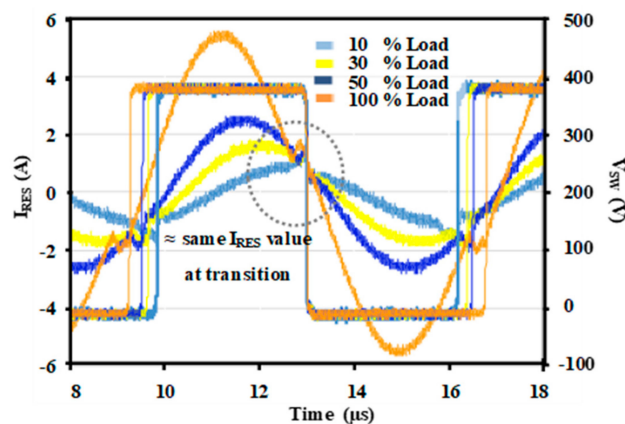


Figure 8. Experimental I_{RES} and V_{SW} measured at different loads for $DUT1$ as an example of how the resonant current varies with the load. As can be seen, different switching frequencies are also used for different loads.

In Figure 8, the current through the resonant tank (I_{RES} in Figure 6) is shown for different power levels, as well as its corresponding V_{SW} waveform. As can be seen, the I_{RES} value during the transition of both DUTs remains almost the same regardless of the load level, which will be helpful to estimate switching losses (they are calculated by means of the energy dissipated during the turn-on and turn-off) and to understand the behavior of the transistors during these transitions.

An efficiency comparison of the LLC resonant converter using all the DUTs as the primary side transistors is carried out in the whole power range, going from 10% to 100% of full load (600 W), always following the same test protocol and operating conditions. In order to minimize error measurements and its influence on the efficiency comparison, a repetitive protocol was performed using an automatic program based on Java. First, the converter is turned-on at 10% of maximum load, and it remains under this working condition for 15 minutes to achieve a constant working temperature. Then, the efficiency

at 10% of maximum load is measured (this measurement is the result of averaging 10 consecutive measurements of V_{IN} , V_{OUT} , I_{IN} , and I_{OUT}). Finally, the load is increased, and new measurements are done after one minute. This procedure is repeated to 20%, 30%, 50%, 70%, and 100% of full load. In Figure 9, the differential efficiencies obtained are shown, taken as reference DUT1, as it is the device that shows best performance for the whole range.

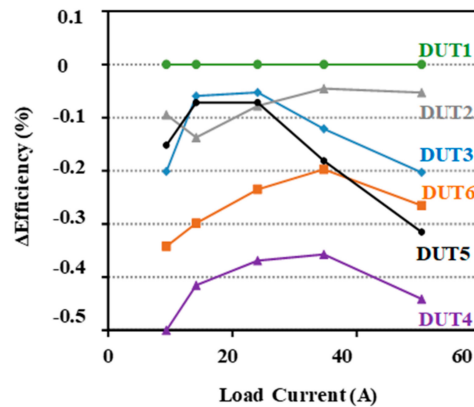


Figure 9. Differential efficiencies of the LLC resonant converter with respect to the best SJ-MOSFET (DUT1).

Using experimental waveforms of V_{GS} , V_{SW} , and I_{SHUNT} , switching (P_{SW}), driving (P_{DR}), and conduction (P_{ON}) power losses contributions from each DUT are calculated for three power loads demands of 60 W (10%), 300 W (50%), and 600 W (100%), and are shown in Figure 10a–c, respectively.

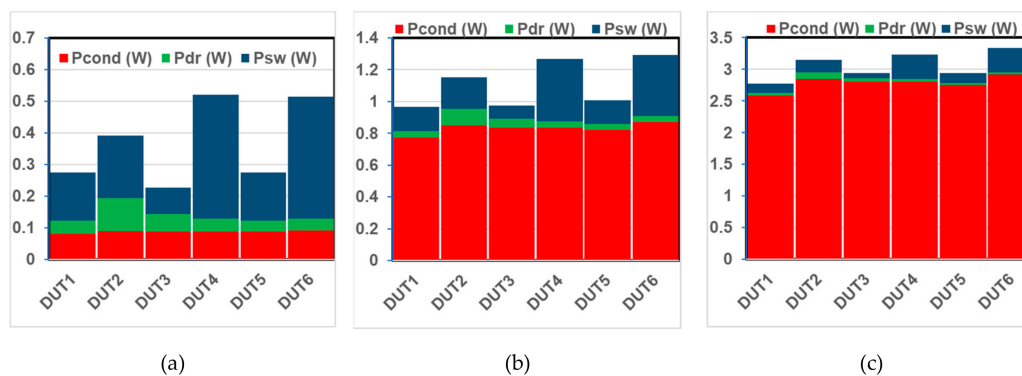


Figure 10. Measured power losses owing to driving (P_{DR}), switching (P_{SW}), and conduction (P_{ON}) at (a) 10%, (b) 50%, and (c) 100% load for each primary-side SJ-MOSFET.

In Figure 10a, at a low load, whereas low P_{ON} losses remain almost equal for all the DUTs, differences in P_{DR} losses have a small impact and P_{SW} losses are dominant. For heavy loads (Figure 10c), P_{ON} is by far the main factor of losses in the SJ-MOSFETs, yet disparity among the P_{SW} losses is discernible. At a medium load (Figure 10b), divergence in P_{SW} among transistors makes the difference (P_{ON} losses are the highest, but fairly the same value, but differences at P_{SW} have a great impact in the losses contribution). Even performing ZVS, P_{SW} losses are relevant and differences in the total power losses between DUTs are the result of $P_{SW} + P_{DR}$ at light loads (Figure 10a) and $P_{SW} + P_{ON}$ at heavy loads (Figure 10c). These P_{SW} losses under ZVS conditions are consistent with the existence of the E_i previously reported.

4.3. Validation of the Simulation Model Including C_{OSS} Hysteresis

The developed spice model of all the SJ-MOSFETs under test includes the definition of the C_{OSS} with two look-up-tables with pairs of values voltage-capacitance, one for the charge and one for the

discharge (obtained using the procedure presented in Section 2). On the basis of the circuit proposed in Figure 6 and using the proposed spice models of the SJ-MOSFETs, some simulations of the LLC resonant converter are carried out using LTSpice. In these simulations, emphasis is on the primary side of the converter and the accurate definition of the C_{OSS} value. Experimental and simulated V_{SW} waveforms are compared in Figure 11 and good agreement is obtained.

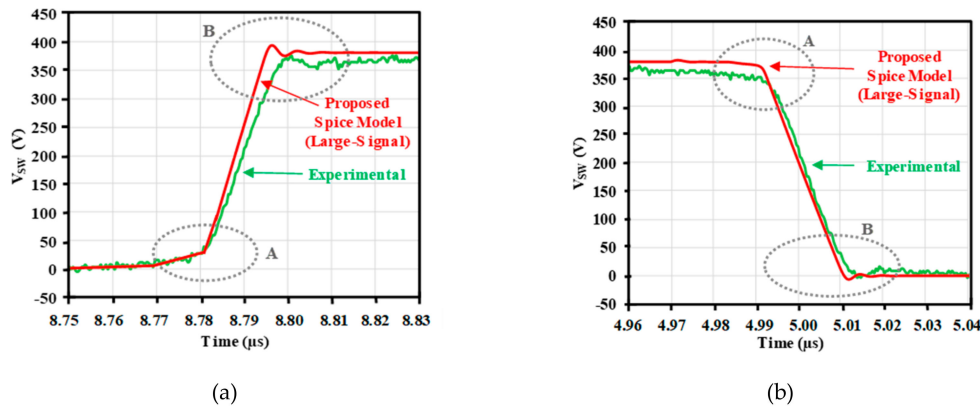


Figure 11. V_{SW} waveform extracted by experimental measurement (green) and simulation with the proposed large-signal spice model (red) during (a) the increase of V_{SW} and (b) the decrease of V_{SW} .

It should be noted that the equivalent capacitance seen from the port defined by V_{SW} is the parallel combination of the output capacitance of DUT_{LOW} and DUT_{HIGH} (two nonlinear capacitors), defined as

$$C_{eq} = \frac{C_{OSS_{DUT_{LOW}}}(V_{SW}) \cdot C_{OSS_{DUT_{HIGH}}}(V_{IN} - V_{SW})}{C_{OSS_{DUT_{LOW}}}(V_{SW}) + C_{OSS_{DUT_{HIGH}}}(V_{IN} - V_{SW})} \quad (3)$$

Taking into account that the value of C_{OSS} of each SJ-MOSFET is different during its charge and discharge, C_{eq} is not symmetric (as presented in previous works not including the C_{OSS} hysteresis [15]) and a different value is obtained when V_{SW} goes up and down. As can be seen in Figure 12, the equivalent impedance during the increase of V_{SW} (C_{eq1}) has the same value at high voltage than the equivalence impedance during the decrease of V_{SW} (C_{eq2}) at low voltage. Consequently, in Figure 11, similar V_{SW} evolution can be seen in the corners marked as A and B during the increase and the decrease of V_{SW} . The proposed spice model captures the corner asymmetry (see corners A and B have different curvature) when V_{SW} goes up and down during DUT_{LOW} turn-off and turn-on transitions, thus being consistent with the existence of a C_{OSS} hysteresis and matching the experimental measurements.

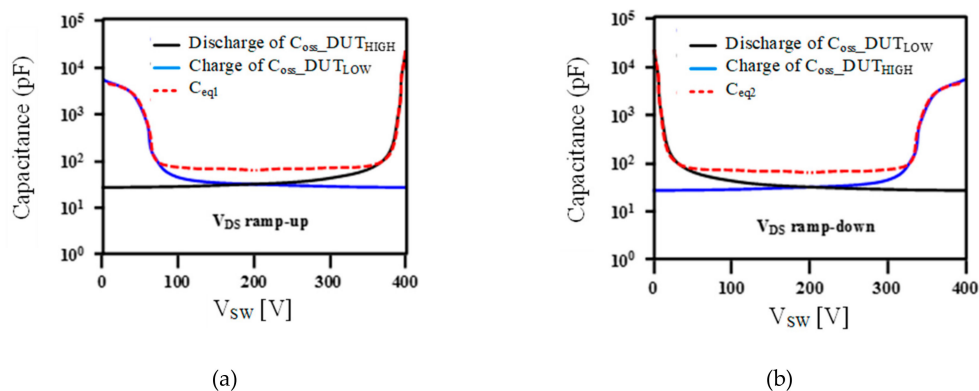


Figure 12. Derivation of C_{eq1} and C_{eq2} , which are asymmetric with respect to the charge and discharge of the C_{OSS} of DUT_{HIGH} and DUT_{LOW} . (a) Increase of V_{SW} and (b) decrease of V_{SW} .

4.4. Validation of the Proposed FoM including E_i

In Figure 9, there is not a clear trend regarding the efficiency that DUTs show for different load demands. Some of them might be suitable for low power, but, in contrast, their performance is worse at full load. That is the case of DUT5. FoMs based on the information provided by the datasheet do not always explain these differences in operation. For example, the worse performance at full load of DUT5 can be explained by its high on-resistance, but the performance for a light load of DUT5 is better than the performance of DUT6, while their switching characteristics are almost the same (even a bit better than those of DUT6).

Consequently, new FoMs are needed to know in detail where the power losses come from, as a great percentage of the converter total losses is attributable to the primary-side SJ-MOSFETs [13] for the whole load range. The proposed FoM should allow a proper selection of the SJ-MOSFETs in an LLC resonant converter. In the last column of Table 1, the value of the proposed FoM for all the DUTs is included, while in Figure 13, these values are compared with respect to DUT1.

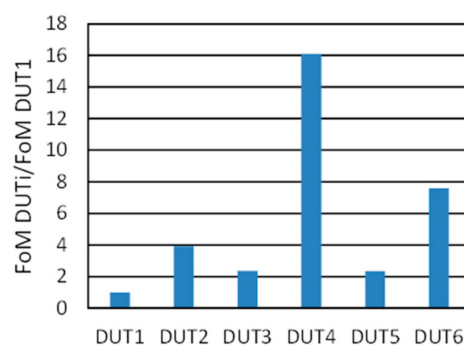


Figure 13. Comparison of the proposed FoM of the DUTs.

The best performance of the LLC is obtained with DUT1, which also has the lowest value of the proposed FoM. DUT2, DUT3, and DUT5 have low values of the proposed FoM and the performance of the LLC with them is also good, especially at medium and light loads. DUT4 has the highest value of the proposed FoM, and the LLC with this DUT has the lowest performance.

As can be clearly seen, the proposed FoM can predict the better performance of the LLC with DUT5 than with DUT6 (especially at light load), which cannot be explained using the characteristics from datasheets.

5. Conclusions

The existence of E_i in power devices, which produces significant switching energy losses in high switching frequency power converters, even under ZVS, has been shown in this paper. Moreover, E_i are related to a C_{OSS} hysteresis.

A simple methodology using a commercial system is suggested to manufacturers to provide E_i (which is not included in datasheets) and information about the C_{OSS} hysteresis. The relevance of the C_{OSS} hysteresis information is validated by developing simulation models that accurately match the experimental charge and discharge waveforms of the C_{OSS} . These new models will allow the designer to better predict the behavior of the power devices and their corresponding power losses, in order to be able to design more efficient applications.

Efficiency experimental results on an LLC resonant converter are used to validate the suitability of the proposed FoM including E_i , to properly select the transistors used in soft-switching power converters operating at high frequencies.

The impact of these kinds of losses is important in high switching frequency power converters and should be properly modelled to be able to predict the performance of different commercial power

transistors in case the designer needs to compare several of those for a certain application; consequently, new data and models are needed.

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Nomenclature

V_{IN}	input voltage of the LLC converter.
V_{OUT} :	output voltage of the LLC converter
DUT_{HIGH}/DUT_{LOW}	primary side MOSFETs under test
L_R	discrete series resonant inductance of the resonant tank
L_M	magnetizing inductance of the resonant tank
C_R	discrete resonant capacitor of the resonant tank
V_{GS}	gate-to-source voltage of the DUT_{LOW}
V_{SW}	drain-to-source voltage of the DUT_{LOW} . Switching voltage
I_{RES}	current through the resonant tank
I_{SHUNT}	drain-to-source current through DUT_{LOW}
I_{CH}	simulated current through the channel of the DUT_{LOW}
P_{INS}	instantaneous power dissipated in the DUT_{LOW} . Product of I_{SHUNT} and V_{SW} .
C_{OSS}	non-linear output capacitance of the MOSFETs
G, S, and D	gate, source and drain terminals of the MOSFETs
P	p-doped zone
N	n-doped zone
E_i	intrinsic energy losses after charging and discharging C_{OSS} up to a certain drain-to-source voltage (V_{DS}) in off-state
E_{CUM}	cumulative energy in the MOSFET when applying a voltage pulse on it during off-state.
P_{SW} , P_{DR} , and P_{ON}	switching, driving, and conduction power losses of the MOSFETs

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