Design and Control of a Modular 48/400V Power Converter for the Grid Integration of Energy Storage Systems

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***Abstract*—Battery energy storage systems are increasingly used to stabilize and balance energy supply systems. For stationary applications, as UPS, electrochemical battery modules are often used, being Li - Ion and lead acid the most popular choice mostly due to power ranges, energy capacity and reversible capability. The present paper is focused in the design of a modular converter to boost the voltage of a Li - Ion battery module from 48 to 400 Volts, with a maximum power of 18 kW. The selected power converter topology is based on a DC/DC converter built by an interleaving synchronous rectifier (ISR) connected in series to a Three Phase Dual Active Bridge (TPDAB). The paper includes an study on alternative topologies, the dynamic average model for the selected approach, the control system design, the selection and implementation of a hardware prototype and the validation of the complete system using simulation under PLECs.**

I. Introduction

Typical energy storage systems (ESS) are based on super-capacitors, flywheel, electrochemical cells or fuel cells. In the field of stationary applications Li - Ion battery cells have increased its use due to high cell voltage, up to 5V, i.e. $LiCoPO_4$, large gravimetric energy density and high efficiency with values up to the 97% [1]. Despite the Li - Ion cells having one of the highest cell voltages, the required number of series-connected cells together with the increased power requirements, creates the need of boosting the voltage to values which can vary between 400 V and 800 V. A typical solution to boost the voltage is to series connect the required number of cells to achieve the desired voltage. However, in order the manufactures to decrease the number of offered configurations, it is demanded to have a base module that can be easily interconnected for different applications. This connection among the different modules could be either passive or active (by means of power conversion stages). Fig. 1 a) shows the passive alternative, either by series or parallel connection. This alternative could trigger different problems regarding the unbalance among the modules and often implies battery system with higher energy than required, thus increasing the costs. For that reason, in this paper an active modular connection shown in Fig. 1 b) is considered. More precisely, this research is focused on the modular dc/dc converter used as the basic block of the proposed active alternative.

Modular structures present an active capability for the energy transfer among battery modules. Additionally, they enable the optimization of the needed energy storage, add the possibility of incorporating additional modules to already existing systems and include the galvanic isolation in the power converter, thus avoiding the low frequency transformers. However, including the additional conversion stage requires new designs, able to deal with large transformation gains (around 1:10), important low-side current capability, simmetrical power transfer capability and high efficiency [2] [3].

For this paper, the modelling, design and control of a modular $48/400$ V, 18 kW bidirectional DC/DC converter is proposed. The design is able to deal with a high-transformation ratio and high power density, [4], [5]. The designed power converter could be easily combined with others in order to increase the output voltage and/or current.

This paper is organized as follows. In Section II a review of different DC/DC topologies and the selected converter are presented. In Section III, the average model of the adopted topology is developed. Section IV presents the selection criteria for the different components. In Section V the design of the control is presented. Section VI includes the simulation results based on PLECs and Matlab. Section VII shows the prototype setup and Section VIII the conclusion for the presented work.

II. Power Converter Selection

The present application proposes a DC/DC converter that boosts the voltage of a Li - Ion module from 48 V to 400 V with a maximum power of 18 kW. The main design constraints are: 1) High transformation ratio, 2) High currents at the battery side: Up to 360 A (2 C) at nominal voltage, 3) The capability to transfer bidirectional power, 4) Modular design, 5) High converter efficiency.

The present work has been partially supported by the predoctoral grants program FPU for the formation in university teaching of Spain MECD under the grant IDs FPU16/06829. This work also was supported in part by the Research, Technological Development and Innovation Program Oriented to the Society Challenges of the Spanish Ministry of Economy and Competitiveness under grant ENE2016-77919-R; by the European Union through ERFD Structural Funds (FEDER).

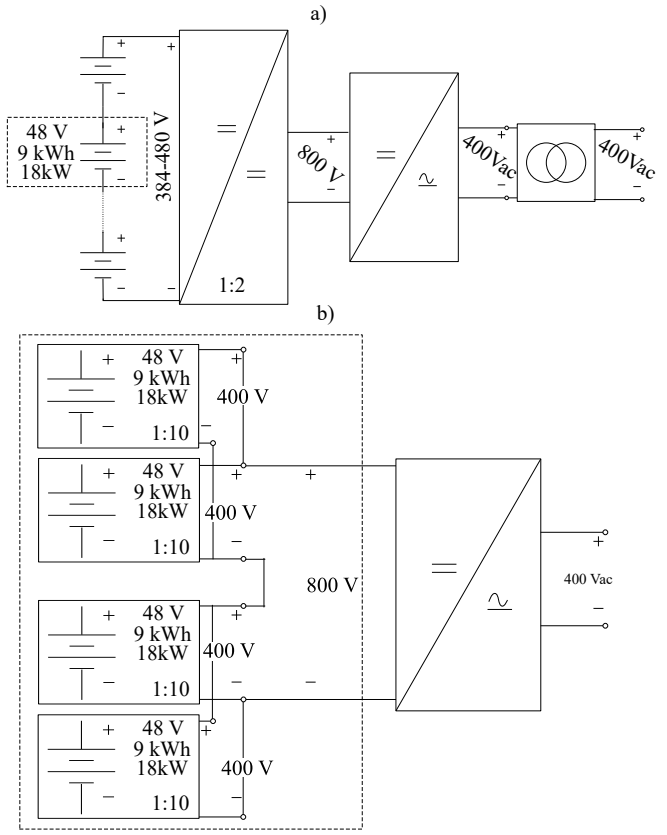

Fig. 1. Converter application structure. a) Presents the typical passive structure. b) Presents the proposed structure for the 48/400 converter.

For the initial analysis, a literature review for the comparison of several DC/DC topologies have been done (see Table I). Based on that, the TPDAB has been selected as the most suitable topology. The superior aspects of the TPDAB are:1) High efficiency, 2) Current capability, 3) Simplicity for control implementation, 4) galvanic isolation by means of a high frequency (HF) transformer.

Regarding the current capability, it must be noticed that alternative solutions require device parallelization. Alternatively, parallel-bridge connection could be considered. However, this will turn in additional transformer per bridge, increasing the system costs and decreasing the power density.

An easier approach, selected in this paper, is to incorporate a previous conversion stage built by an ISR, used to boost the TPDAB operation voltage. Main advantages of the ISR are: 1) Reduced current ripple at the battery side, 2) Avoids parallel devices, 3) Enables the modular capability of the power converter by increasing the number of ISR legs. It is recalled that the TPDAB has to be adapted to the different power levels, but the topology remains unchanged, 4) Reduces the turns ratio of the TPDAB.

This first stage is also responsible for generating an stiff DC-link voltage at the primary side of the converter, regardless of the battery voltage. This allows to increase the efficiency of the TPDAB by reducing the maximum current in the primary side and avoids the device parallelization. The voltage at this DC-link (V_{pDC}) is selected to be 115 V. This is the minimum voltage that allows to carry out the maximum power within the selected devices current limits (a safe margin of 20% is still kept).

The final topology of the dual-stage converter is presented in Fig. 2. The first stage, based in an ISR, is similar to the one presented in [5], but removing the integration of the first-stage for an improved system modularity. As commented before, the proposed approach also allows to easy increase the input current capability by adding extra parallel legs. The second TPDAB stage is responsible for the control of the 400 V dc-link. The proposed topology consists in two 3-phase full bridges connected to a HF transformer. The maximum transfer power is determined by the equivalent series inductor.

III. System Modelling

The system modelling is based on the average representation for the circuit presented in Fig. 2. For easing the discussion, the models of the two stages are derived independently. The $\widehat{\ }$ symbol is used for the representation of average variables.

A. ISR Model

The average model of the ISR stage is derived by considering the TPDAB stage as an external current source connected to the 115 V dc-link. The dynamics are analysed considering the value commanded to the current source to be dependant on the demanded power.

Based on the synchronous rectifier model, the average voltage across each inductor ($\widehat{V_L^{ISR}}$) is given by the battery voltage (V_{BAT}) minus V_{sw}, the average voltage at the a^{ISR}, b^{ISR} or c^{ISR} phases (1).

$$\widehat{V_L^{ISR}}(t) = \widehat{V_{BAT}}(t) - \widehat{V_{sw}}(t) \tag{1}$$

Where the switching voltage dependent directly on the duty ratio, (2).

$$\widehat{V_{sw}}(t) = (1 - \widehat{d_{isr}}(t))\widehat{V_{pDC}}(t) \tag{2}$$

Considering the voltage-current relationship at each of the inductors to be given by (3), the current at the battery can be expressed by (4) as the sum of the currents through each ISR leg.

$$\frac{d(\widehat{I_L}(t))}{dt} = \frac{-R_{ISR}}{L_{ISR}}\widehat{I_L}(t) + \frac{1}{L_{ISR}}(\widehat{V_{BAT}}(t) - \widehat{V_{sw}}(t)) \tag{3}$$

$$\widehat{I_{BAT}}(t) = \widehat{I_a^{ISR}}(t) + \widehat{I_b^{ISR}}(t) + \widehat{I_c^{ISR}}(t) \tag{4}$$

Assuming the inductances at each leg to be equal, and the duty ratio to be the same, it is concluded that the I^{ISR} current in all the three legs is balanced and equal to one third of the battery current. From the battery current, the average output current of the first-stage can be determined by (5). Considering the dc current demanded by the TPDAB to be I_{pDC}, the current flowing through the C_p capacitor is given by (5). From there,

TABLE I
DC/DC COMPARISON

Converter	Boost Ratio	Parallelization of legs/bridges		Isolation	Efficiency (%)	Components	
		Implementation	Cost			Switching Devices	Passive Devices
ISR[6]	1:5	Easy	Cheap	No	94 [7]	2 per leg	1 inductor per leg
DAB [8]	1:n	Easy	Cheap	Yes	88-94 [9]	4 per bridge	1 phase Trafo, 1 series inductor
TPDAB [10]	1:n	Easy	Expensive	Yes	88-96 [11]	6 per bridge	3 Phase Trafo, 3 series inductors
Push-Pull [12]	1:n	Complex	Expensive	Yes	95 [12]	2 per leg	1 phase transformer, 1 series inductor.
Half-Bridge Converter [13]	1:n	Complex	Expensive	Yes	88-96 [14]	2 per leg (3 legs)	1 phase transformer, 1 series inductor.
Double Half-Bridge [15]	1:n	Complex	Expensive	Yes	80-90 [16]	2 per leg	1 Phase Trafo, 1 series inductor, 2 capacitors per leg (2 legs).
High Gain BDC Bridge Boost [17]	1:10	Easy	Cheap	No	<Convencional BDC[17]	4 per stage	1 inductor.
Quadratic Boost [18]	1:10	Complex	Cheap	No	83-88 [19]	4 per stage	2 coupled inductors, 1 capacitor.

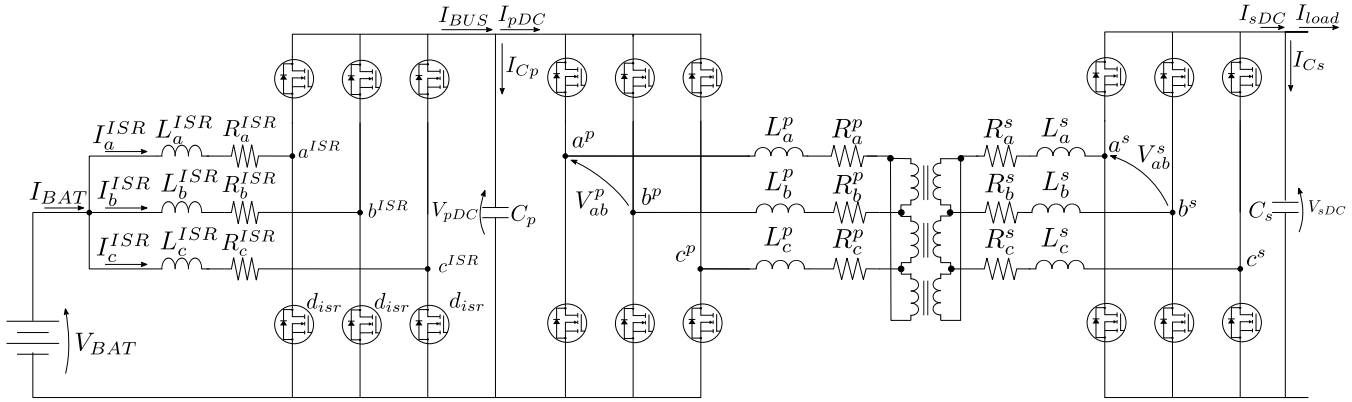

Fig. 2. Dual Stage circuit model.

the dynamic model for the output voltage, V_{pDC}, is given by (6). The average model for the ISR is shown in Fig. 3.

$$\widehat{I_{Cp}}(t) = (1 - \widehat{d_{isr}}(t))\widehat{I_{BAT}}(t) - \widehat{I_{pDC}}(t) \tag{5}$$

$$\frac{d(\widehat{V_{pDC}}(t))}{dt} = \frac{1}{C_p}\widehat{I_{Cp}}(t) \tag{6}$$

B. TPDAB Model

Considering that both DC voltages are fixed, the TPDAB can be simplified to a three phase RL impedance, (L_{TPDAB},R_{TPDAB}), neglecting the magnetic losses.

These two voltage sources have a peak voltage value equal to the fundamental harmonic of the phase-to-phase voltage (V_{ab}). Then, the phase-neutral voltage (V_{an}), can be written as $V_{an} = V_{ab}/\sqrt{3}$. The expressions for the fundamental harmonic phase-neutral voltages at the primary and secondary are described in (7) and (8). Where w is the switching frequency in rad/s, ϕ_s and ϕ_p are the phases of each bridges. V_1'' and V_2 voltages are given by (9), where V_1'' is the magnitude of the primary side voltage referred to the secondary.

$$\begin{aligned}
\widehat{V_a^p}(t) &= \widehat{V_1''}(t)\sin(wt + \widehat{\phi_p}(t)) \\
\widehat{V_b^p}(t) &= \widehat{V_1''}(t)\sin\left(wt + \widehat{\phi_p}(t) - \frac{2\pi}{3}\right) \\
\widehat{V_c^p}(t) &= \widehat{V_1''}(t)\sin\left(wt + \widehat{\phi_p}(t) + \frac{2\pi}{3}\right)
\end{aligned} \tag{7}$$

$$\begin{aligned}
\widehat{V_a^s}(t) &= \widehat{V_2}(t)\sin(wt + \widehat{\phi_s}(t)) \\
\widehat{V_b^s}(t) &= \widehat{V_2}(t)\sin\left(wt + \widehat{\phi_s}(t) - \frac{2\pi}{3}\right) \\
\widehat{V_c^s}(t) &= \widehat{V_2}(t)\sin\left(wt + \widehat{\phi_s}(t) + \frac{2\pi}{3}\right)
\end{aligned} \tag{8}$$

$$\begin{aligned}
\widehat{V_1''}(t) &= \left(\frac{4n}{\pi\sqrt{3}}\cos\frac{\pi}{6}\right)\widehat{V_{ab}^p}(t) \\
\widehat{V_2}(t) &= \left(\frac{4}{\pi\sqrt{3}}\cos\frac{\pi}{6}\right)\widehat{V_{ab}^s}(t)
\end{aligned} \tag{9}$$

$$\begin{aligned}
\widehat{V_d^x}(t) =& \frac{2}{3}\left(\widehat{V_a^x}(t)\cos(\widehat{\theta_w}(t)) + \widehat{V_b^x}(t)\cos\left(\widehat{\theta_w}(t) - \frac{2\pi}{3}\right)\right. \\
&\left. + \widehat{V_c^x}(t)\cos\left(\widehat{\theta_w}(t) + \frac{2\pi}{3}\right)\right) \\
\widehat{V_q^x}(t) =& -\frac{2}{3}\left(\widehat{V_a^x}(t)\sin(\widehat{\theta_w}(t)) + \widehat{V_b^x}(t)\sin\left(\widehat{\theta_w}(t) - \frac{2\pi}{3}\right)\right. \\
&\left. + \widehat{V_c^x}(t)\sin\left(\widehat{\theta_w}(t) + \frac{2\pi}{3}\right)\right)
\end{aligned} \tag{10}$$

The system equations can be transformed to the dq reference frame given by (10), where x can be s or p and θ_w is the reference angle. (11) is the voltage drop at the equivalent inductance. The current through this inductance can be calculates as (12), where the impedance Z_{TPDAB} can be approximate by (13) neglecting the transformer leakage impedance. The currents at the DC sides can be calculated from the power

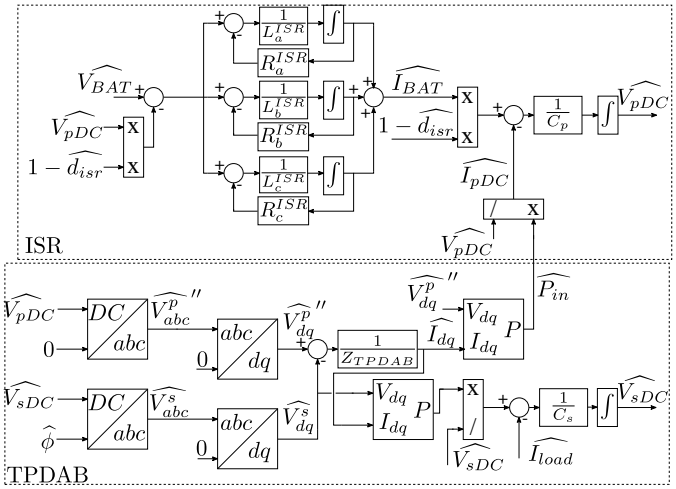

Fig. 3. Dual stage average model non-linear block diagram in time domain.

equivalence, assuming a loss-less model for both bridges, (14) and (15). Using (15), the load current at the primary side (I_{pDC}) can be calculated.

$$\widehat{V_{dq}^{L}}(t) = \widehat{V_{dq}^{p}}(t) - \widehat{V_{dq}^{s}}(t) \tag{11}$$

$$\widehat{I_{dq}}(t) = \frac{\widehat{V_{dq}^{L}}(t)}{Z_{TPDAB}} \tag{12}$$

$$Z_{TPDAB} = R_{TPDAB} + \omega L_{TPDAB} j \tag{13}$$

$$\widehat{P_{out}} = \frac{3}{2}(\widehat{V_d^s}(t)\widehat{I_d}(t) + \widehat{V_q^s}(t)\widehat{I_q}(t)) = \widehat{V_{sDC}}(t)\widehat{I_{sDC}}(t) \tag{14}$$

$$\widehat{P_{in}} = \frac{3}{2}(\widehat{V_d^p}(t)\widehat{I_d}(t) + \widehat{V_q^p}(t)\widehat{I_q}(t)) = \widehat{V_{pDC}}(t)\widehat{I_{pDC}}(t) \tag{15}$$

Using the output power, the current through C_s is calculated as (16), and therefore the voltage at the output can be expressed as (17). The final average model is shown in Fig. 3.

$$\widehat{I_{Cs}}(t) = \widehat{I_{sDC}}(t) - \widehat{I_{load}}(t) \tag{16}$$

$$\frac{d(\widehat{V_{sDC}}(t)}{dt} = \frac{1}{C_s}\widehat{I_{Cs}}(t) \tag{17}$$

IV. System Design

The main parameters for the system design are presented in Table II.

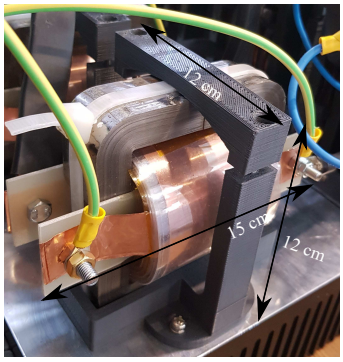

Fig. 4. Photo for one transformer core.

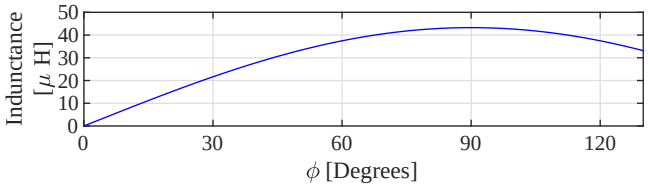

Fig. 5. Inductance curve selection.

A. TPDAB design

1) Transformer design: The selected transformer has a ratio of $8/28$, (primary-secondary). The design is optimized for 20 kHz and 18 kW. For the prototype, the transformer has been made by three independent cores for avoiding asymmetric flux distribution in the mid leg and bespoke designs. Fig. 4 shows one of the transformers arrangements.

2) Series Inductor selection: To design the needed inductor, the procedure in [10] has been followed. A balanced 3-phase sinusoidal voltage at each side of the transformer is considered. The magnitude of the first harmonic for the modulated squared waveform generated by the bridges, with 0.5 duty is considered for the analysis. Power transfer is given by (18), considering a turn ratio $n = 28/8$ and all the variables referred to the secondary. This equation shows the dependence of the phase shift between the two bridges (ϕ) and also on the inductance value. Then, for a maximum power of 18 kW and considering the phase shift from $0°$ to $120°$, the possible inductance values referred to the primary are presented in Fig. 5. The maximum inductance is obtained at $90°$, for the maximum power capability. As lower inductances will increase the theoretical power capability, this will turn into a oversized converter. For that reason, the selected inductance is $43,2$ μH. In order to make the converter symmetrical, the inductance has been split into two: the primary (1.79 μH) and the secondary (21.61 μH). With this inductance values, the power transfer in the TPDAB depending on the phase-shift is shown in Fig. 6.

$$P_{FLOW} = \frac{nV_1V_2}{\omega L_{TPDAB}} sin(\phi) \qquad \phi = \phi_s - \phi_p \tag{18}$$

TABLE II
CONVERTER PARAMETERS

Battery Pack		ISR		TPDAB	
Parameter	Value	Parameter	Value	Parameter	Value
Voltage	$41-53$ V	C_p	840 μF	C_s	420 μF
Max Power (2C)	18 kW	L_{INT}	92 μH	L_p/L_s	1.79/21.6 μH
Nominal Voltage	48 V	V_{pDC}	115 V	Transformer	HF Three Phase, 18 kW, n=28/8 (s/p)
Nominal Capacity (C)	180 A	F_{sw}	20 kHz	V_{sDC}	400 V
Current:Discharge	180 A(C)-540 A(3C)	MOSFET	IXFN360N15T2	F_{sw}	20 kHz
Current:Charge	90 A (1/2C)-180 A(C)			MOSFET p/s	IXFN360N15T2/IXKN75N60C

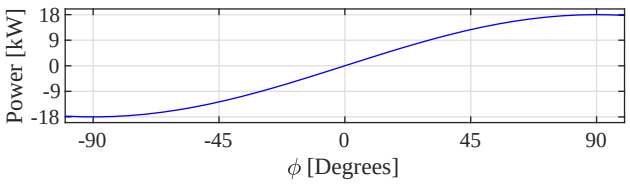

Fig. 6. TPDAB power vs the phase shift between the primary and secondary three-phase bridges.

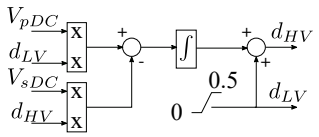

Fig. 7. TPDAB start-up control system.

B. Capacitors Selection

Film capacitors have been selected for the DC-link due to lower ESR and higher reliability [20]. The same capacitor reference is used for both DC links. For C_p, due to the high currents at the capacitor and the large voltage variation, two film capacitor in parallel, each 420 μF have been selected. At the output bridge only one film capacitor with the same value is required.

V. CONTROL SYSTEM DESIGN

The control is divided in two modes: start-up and regular operation. Start-up drives both stages during the buses pre-charging, with the main objective of achieving a reduced in-rush current to avoid transformer saturation. Regular operation requires to keep the voltages at both DC-links within safe limits near the rated values, rejecting load disturbances and controlling the battery charge and discharge current.

A. Start-Up

During the start-up procedure, the V_{pDC} is first charged to 115 V by operating the ISR stage. The proposed start-up control is shown at Fig. 7. The AC voltages at both sides of the transformer are gradually increased by adding a slow ramp that varies the primary, d_{LV}, and secondary, d_{HV}, duty ratios from 0 to 0.5. An integral controller is designed to modify the d_{HV} ramp in order to keep AC voltages sides at the same level, despite the differences bus voltages, and therefore reducing the inrush current. This avoids the use of any extra circuit, as the one proposed in the literature [21].

B. Regular Operation

During the regular operation, the converter is used for the battery control. The proposed control compromises a phase-shift control loop for the TPDAB and a cascade control loop for the ISR. The TPDAB phase-shift control demands the needed power for controlling the V_{sDC}, using (18) for the non-linear phase-to-power compensation.

C. ISR Control

Base on the average model, the control for the ISR is divided into two cascade loops: A current control loop and a voltage control loop.

1) Current Control: Following the assumption of the average design, if I_a^{ISR}, I_b^{ISR} and I_c^{ISR} are the same in each leg, a single PI controller, tuned for the plant described in 3 and considering the resistance to be negligible is used. The design has been performed so the close-loop system has a bandwidth of 1 kHz with a damping factor equal to one. The PI gains are calculated using (19).

$$K_P^c = 2\omega_n L_{ISR}, \quad K_I^c = \omega_n^2 L_{ISR} \tag{19}$$

2) Voltage Control: The voltage regulator has been designed using the Quadratic Voltage Control proposed in [22]. Where the expression that defines the system is given by (20). Following the same procedure than for the current controller, the expression used to tune the gains is shown in (21).

$$\frac{d(V_{pDC}^2(t))}{dt} = \frac{2}{C} P_{Cp} \tag{20}$$

$$K_P^p = \omega_n C_p, \quad K_I^p = \omega_n^2 C_p/2 \tag{21}$$

Since the disturbance introduced by the TPDAB is related with the demanded or delivered load power, and considering there are no losses, the relationship between the current through the inductor and the power through the capacitor is given by (22). Because the I_{pDC} is not measured, P_{in} is estimated as the power demanded by the TPDAB, P_{FLOW}. Final control structure for the V_{pDC} control is shown in Fig. 8.

$$I_L = \frac{P_{Cp} + P_{in}}{3V_{BAT}} \cong \frac{P_{Cp} + P_{FLOW}}{3V_{BAT}} \tag{22}$$

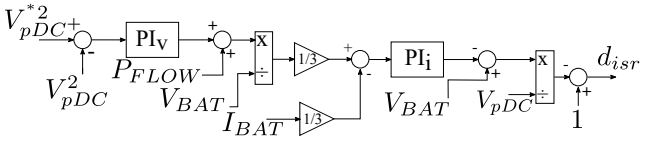

Fig. 8. ISR control structure.

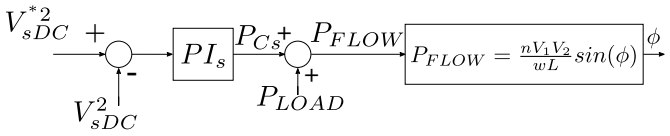

Fig. 9. TPDAB Control Structure

D. TPDAB Control

The TPDAB control has a single loop for controlling the V_{sDC} voltage. Equivalent to the V_{pDC}, a QVC control is used. The non-linear relationship between the transferred power and the ϕ angle is compensated by (18). Controller tuning is identical to the procedure shown before for the V_{pDC} control.

E. Control tuning

To tune the gains of all regulators, the cross-effects of the bandwidth and damping factor variation for each of the three controllers over the other two controlled variables have been analysed: 1) Bandwidth and damping factor for the TPDAB and ISR voltage controllers are set to 100 Hz and 1 Hz. The bandwidth and damping factor of the current controller is varied from 500 to 2000 Hz and from 0.5 to 1, respectively. Fig. 10 a) and b) shows the maximum variation at the voltages in V_{pDC} and V_{sDC}. 2) Bandwidth for the voltage controller of the TPDAB and current controller of the ISR are set to 100, 1000 Hz respectively and for both the damping factor is set to 1. Then bandwidth of the ISR voltage controller varies from 50 to 200 Hz and the damping factor from 0.5 to 1. Fig. 10 c) and d) shows the maximum deviations in V_{pDC} and V_{sDC} respectively. 3) Bandwidth for the voltage controller and current controller of the ISR are set to 100 and 1000 Hz respectively and a damping factor of 1. Then bandwidth of the TPDAB voltage controller varies from 50 to 200 Hz and the damping factor from 0.5 to 1. Fig. 10 e) and f) shows the maximum values for V_{pDC} and V_{sDC} respectively. Based on these results, the values marked with a red dot in Fig. 10 have been selected. The numerical values are listed in Table III. These parameters have been selected considering a ratio of $1/10$ between the external voltage and internal current bandwidths.

VI. Simulation Results

To test the previous behaviour, three different simulations have been performance using PLECs/Matlab: 1) Start-up using switching model, 2) Average model and 3) Switching model vs. Average model. The average model has been implemented in PLECs for the comparison with the switching model and also in Matlab to test the different control regions and the response to a 1C and 2C load cycles.

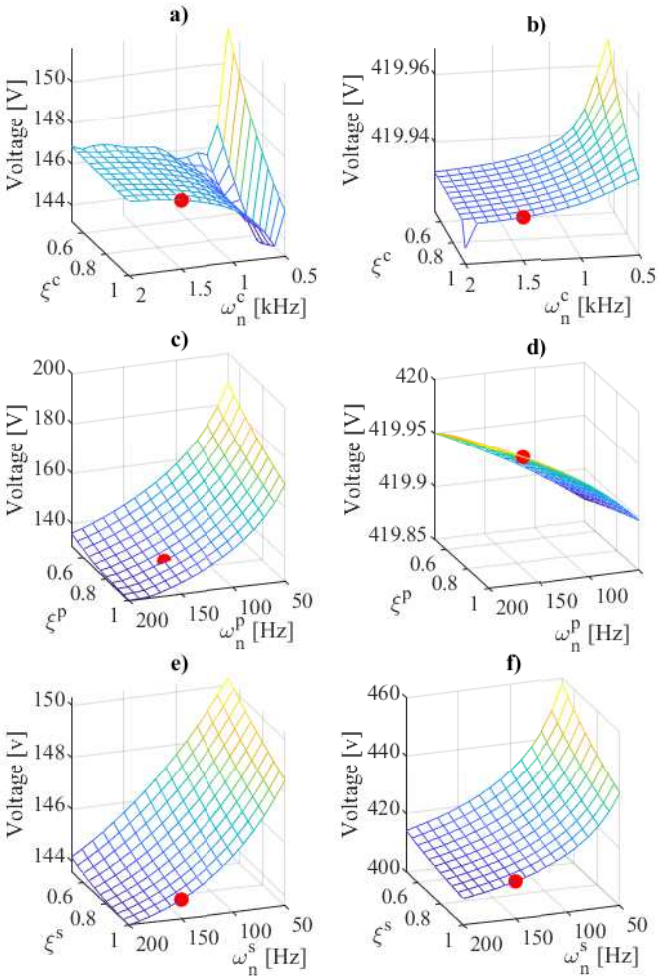

Fig. 10. Control Regions. (a) and (b): Current controller effect in V_{pDC} and V_{sDC}. (c) and (d):V_{pDC} controller effect in V_{pDC} and V_{sDC}. (e) and (f): V_{sDC} controller effect in V_{pDC} and V_{sDC}.

TABLE III
Controllers Gain Selection

	Parameters		Regulator Gains	
	w_n [Hz]	ξ	K_p	K_i
PI_c	1500	1	1.1561	3632.01
PI_p	150	0.85	0.791	373.07
PI_s	150	1	0.3958	186.53

A. Start-up Simulation Results

Simulation using PLECS has been used for validating the start-up performance, Fig. 11. The V_{pDC}, battery current, control action, are shown in Fig. 11a), b), c) respectively. V_{sDC}, transformer rms currents, modified duty ratio and three phase primary currents are shown in d), e), f) and g). The proposed control reduces the voltage difference between the primary and the secondary bridges, allowing for a reduction in the TPDAB primary side current of 20 A with respect to the base case.

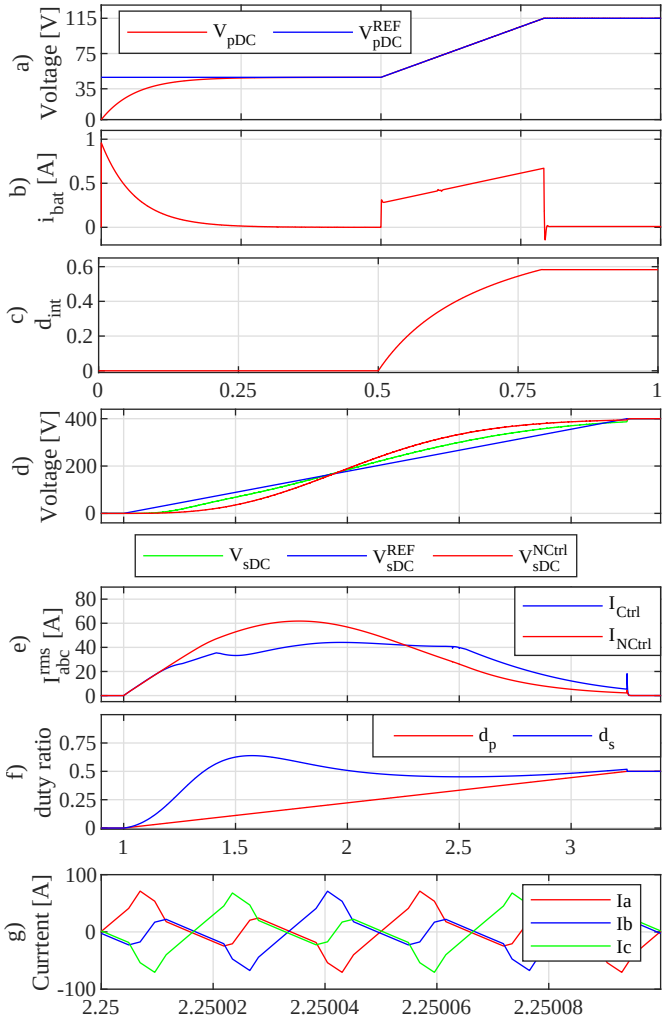

Fig. 11. Start-up results: a)Primary DC voltage, b) Average battery current, c) Interleaved duty, d) Secondary DC voltage with and without the proposed control e) Primary current rms value with and without the proposed control, f) Primary and secondary duty ratios, g) Start up current waveform at the primary.

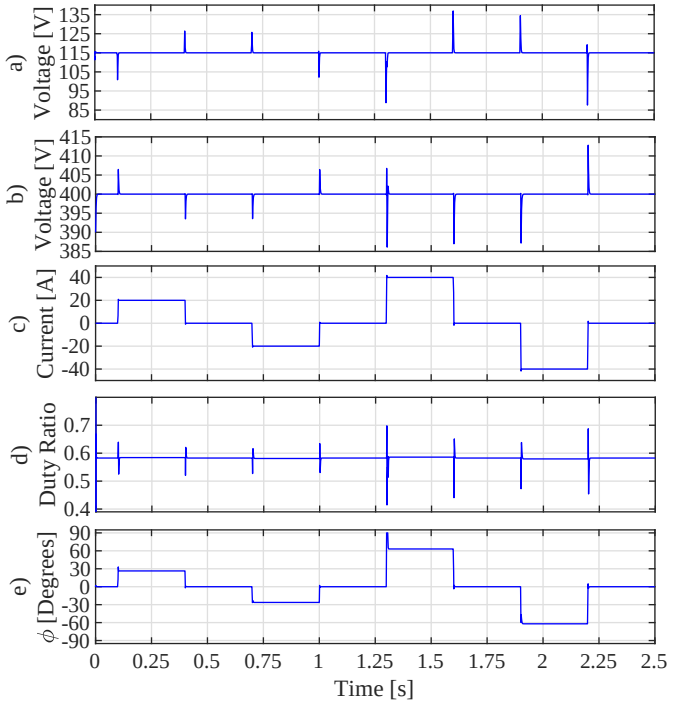

Fig. 12. Average model evaluation. a) V_{pDC} response. b) V_{sDC} response. c) Load current, positive currents means a discharge process. d) ISR control action (d_{ISR}). e) TPDAB phase shift control action (ϕ).

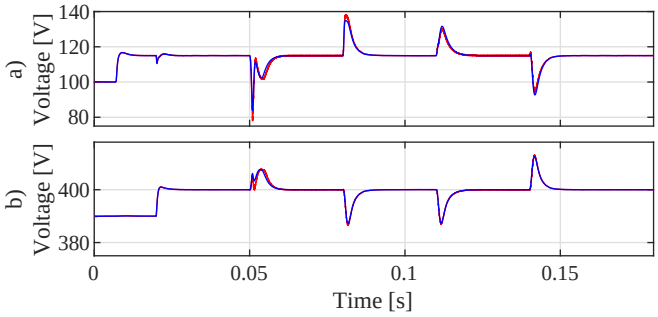

Fig. 13. Average vs switching model under a reference change and a 2C load step in discharge/charge. a) V_{pDC}. b) V_{sDC}. In both figures the switching model is shown in red and the average model in blue.

B. Average model

The proposed control system has first been evaluated with the developed average model. The results for load steps at 1 and 2C are shown in Fig. 12. The control system is tuned according to the damping factors and bandwidths selected in Fig. 10. The present results validates the expected voltages overshoots presented in Fig. 10. The V_{pDC} and V_{sDC} maximum voltages are 136 V and 414 V respectively, similar to the one shown in Fig. 10 c), d).

C. Switching model vs Average model

In order to validate the proposed average model, Fig. 13 shows a comparison between the system response for a load cycle of 16 kW, both for the average and the switching model. Clearly the responses are in good agreement, thus validating the previous average model. Table IV shows the efficiency of the switching model using PLECs with an approximate model of the selected switches to obtain the switching and conduction losses. For nominal operation (0.25-1 C), the obtained efficiency is around 96-93%. During 10-15 seconds it is possible to discharge the battery up to 2C. In this case efficiency decrease to 87%.

VII. Experimental Setup

Fig. 14 shows a first prototype of the proposed converter. The prototype consists in three different blocks: 1)DC buses that includes all the switching devices for both stages. 115 V and the 400 V are isolated by a 1 mm PVC plastic sheet. Both DC buses and inductive connection terminals are formed by a tinned copper sheet and are connected with the switching devices by tinned brass stems. Inductors are placed in another block between the DC buses and the transformer. As is

TABLE IV
SWITCHING MODEL EFFICIENCY

Loss [W]	Battery Power [W]	Efficiency
77,5	2015 (1/4 C)	96.1%
190	4060 (1/2 C)	95.3%
550	8220 (1 C)	93.3%
2200	17000 (2 C)	87%

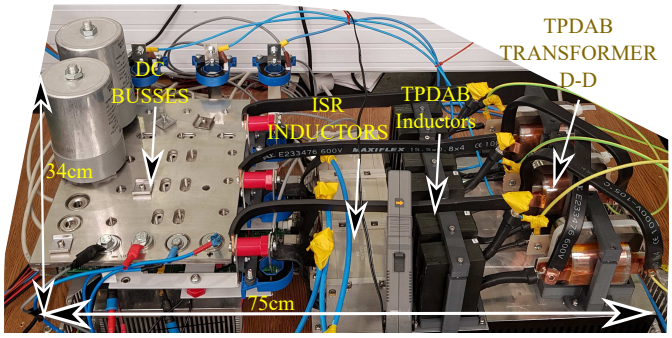

Fig. 14. Converter Model setup.

commented before the TPDAB high frequency transformer is formed by three different single phase transformers in a Delta - Delta arrangement. High current connections are formed by flexible copper sheets.

VIII. CONCLUSION

This paper has proposed a new approach for a 48/400V converter with an application to battery packs. By integrating an ISR and a TPDAB, the converter avoids semiconductors parallelization by using an interleaving approach. The presented control system includes a novel method for the converter soft-starting and an average model for a better control parameters selection. Simulation results have validated the operation, average model of the converter, control system design and estimated efficiency for a maximum discharge rate of 2C. Future works are dedicated to the testing of the built prototype and the validation with experimental results.

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