Discontinuous PWM for Online Condition Monitoring of SiC Power Modules

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***Abstract*— This paper presents the utilization of discontinuous PWM modulation for the condition monitoring of SiC power MOSFETs switching at high switching frequencies in a three-phase inverter prototype. Due to the settling time imposed by the monitoring system, accurate measurements require low switching frequency and high modulation indexes when monitoring. To overcome these limitations, a discontinuous PWM modulation strategy is proposed. This way, the monitored device does not switch during certain time, and hence the accuracy of the measurements is not compromised. The effect of the alteration of the modulation is analyzed in terms of power losses and current ripple, comparing the traditional with the proposed modulation. Moreover, online monitoring results performed in a SiC-based inverter prototype in different operating points are presented. An R_{DS}-based thermal model is presented in order to estimate online the junction temperature.**

I. Introduction

Nowadays, the integration of wide-bandgap (WBG) semiconductor devices in power electronics industry is experiencing a huge increase. The improved properties offered by materials such as SiC and GaN compared with those of Si [1], like higher electric field, electron velocity and high temperature operation, allow to obtain better semiconductor devices that lead to more efficient and smaller power electronic converters. Regarding SiC devices, their enhanced performance has favoured its industrial introduction, especially in high-power applications. In these applications, such as traction or renewable energy generation, the improvements in terms of the reduction of volume and increase of switching frequency and efficiency are even more evident [2], [3], [4].

However, the lack of maturity of these devices and the short experience with them in in-field conditions cause uncertainty regarding their long-term degradation. In order to overcome these issues, condition monitoring has been proposed as a way to predict failures and enhance the reliability of power electronics systems [5]. A recent survey among industry experts recognised condition monitoring as a key method to achieve a higher reliability in power converters [6]. There, power modules and electrolytic capacitors were considered as the components most susceptible to failure, while condition monitoring was identified as an interesting trend to improve system reliability. By employing condition monitoring, maintenance can be schedule when required. Moreover, active thermal control techniques can be implemented in order to reduce degradation and extend the useful lifetime [7].

Package-related failures are considered the limiting factor to increase the lifetime of power modules [8]. For IGBT power modules, bond-wire and solder joints degradation are the two most relevant failure mechanisms [9]. Both are caused by the thermomechanical stress caused by the power losses generated in the semiconductors [10]. Since the packaging employed for IGBTs is similar to that of SiC power modules, similar wear-out failures can be expected. Moreover, a comparison between the fatigue stress in a Si and a SiC power module was presented in [11] for the same electrical ratings and temperature profiles. The study concluded that a higher stress and theremore lower lifetimes is expected in SiC power modules due to the mechanical properties of SiC. A number of condition monitoring techniques have been presented in order to evaluate the state-of-health of the semiconductors [12]. However, it is often difficult to diagnose the root-cause of degradation, since different failure mechanism have the same failure effect.

Condition monitoring usually requires dedicated circuits, which have to reduce noise and measurement errors [13], [14]. Furthermore, the monitoring system is usually device-specific, since the damage-sensitive monitored parameters are influenced by the packaging and the internal layout of the module. Moreover, the monitoring circuit must be easily integrable in the converter, in order to be implemented in an industrial product [15]. This implies that the system must be able to perform online measurements without interfering on the regular operation of the converter. Furthermore, the monitoring system must not compromise the overall system reliability. Although several monitoring systems have been proposed in the literature, only few of them have been tested in in-field conditions [16], [17], [18], [19].

For those single-chip power modules with an auxiliary source available for control purposes, it was proposed in [20] a technique to predict the junction temperature of the Device Under Test (DUT) independently of the degradation on the bond wires. The mentioned technique consists in the use of the on-state resistance as a Temperature Sensitive Electrical Parameter (TSEP) [14], [21]. This is obtained by monitoring the on-state voltage between the drain and auxiliary source

TABLE I
PROTOTYPE SPECIFICATIONS.

Three Phase Inverter	
Power Module	Wolfspeed CCS050M12CM2
DC-Link Voltage	300 V
DC-Link Capacitance	49 μF
L_{Filter}	2.4 mH
R_{Load}	40 Ω
Output Frequency	50 Hz

$V_{DS_{aux}}$ and the drain current I_D. However, the monitoring requires certain minimum on-state times in order to work properly. This fact limits the maximum switching frequency that can be achieved by the DUT, which in turn limits the potential benefits of SiC. Similar issues have been found in other publications [18], [22].

To overcome the above limitation, a discontinuous modulation during a fundamental period of the modulation signal could be implemented for monitoring. The use of discontinuous pulse-width modulation (DPWM) has already been proposed for different purposes, being it popular due to the reduction of switching losses. This modulation has been employed to reduce thermal stress and enhance the lifetime [23], [24], [25] or to achieve higher efficiencies or power densities [26], [27], [28].

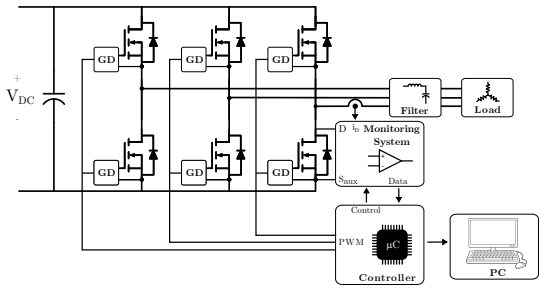
In this paper, the use of a discontinuous modulation for the monitoring of power semiconductors in inverter systems is proposed. This way, the measurements can be carried out during normal operation of the converter without interruption for monitoring purposes. This is mandatory in high power SiC-based converters, which take advantaje of the high switching frequency capabilities of SiC devices. The remainder of the paper is arranged as follows. In Section II, the set-up employed to perform the tests is described, along with the monitoring system and the DUT. Section III shows the limitation of conventional monitoring system in comparison with the proposed one. Section IV shows the experimental results at different operating points. Section V finalizes the paper with conclusions.

II. EXPERIMENTAL SET-UP

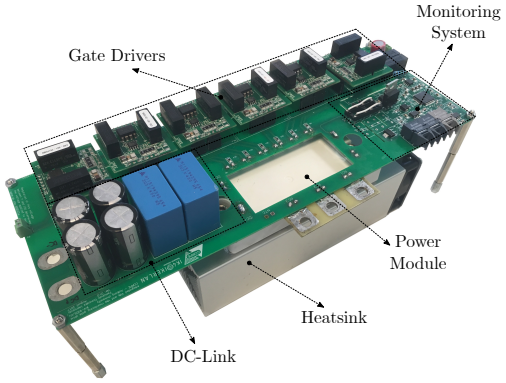
A. Prototype Specifications

In order to present the problem of monitoring at high switching frequency, a SiC-based converter prototype has been developed. In Figure 1(a), a functional diagram of the prototype is shown, along with a photograph of the set-up in Figure 1(b). Concretely, it consists of a three-phase inverter, in which the Condition-Monitoring System (CMS), whose details are described below, is implemented on one of the active switches.

The power module employed is a six-pack 1200-V/50-A MOSFET module, which consists on three half-bridge branches in parallel. The module is mounted on a forced air-cooled heatsink. For the control of the converter and the CMS, a digital microcontroller is employed along with commercial SiC gate drivers. Moreover, a DC-Link is sized in order to meet the desired performance. In Table I, the specifications of the prototype are collected.



(a)



(b)

Fig. 1. Experimental set-up: (a) Functional diagram of the components of the system. (b) Photograph of the prototype.

B. Condition Monitoring System

A condition-monitoring circuit is integrated in the described platform in order to estimate the junction temperature of the DUT. Several publications have proved that the on-state resistance R_{DS} is a valid TSEP for SiC MOSFETs [14], [21], [29]. Hence, it could be employed for the online estimation of the junction temperature. This way, if an increase of the thermal resistance of the module occurs as a consequence of the solder degradation, the resulting higher junction temperature can be predicted.

In Figure 2(a), the internal layout of the employed module is presented. In order to determine its on-state resistance, the voltage between Drain and Source V_{DS} and the drain current I_D of the DUT have to be measured. However, if the monitoring is performed between the AC and DC- terminals of the module, it comprises the voltage drop in the power source bond wires. Hence, the measurement would be sensitive to bond wire failures [30]. To avoid the mix-up of failures, the monitoring is carried out between the drain D and auxiliary source S_{aux} of the DUT. This way, the voltage drop in the power source bond wires does not influence the measurement.

The monitoring of V_{DS} is carried out employing the circuit shown in Figure 2(b) [31]. This circuit is specially designed for the monitoring of the on-state voltage of power semiconductors, since during the on-state of the DUT the current

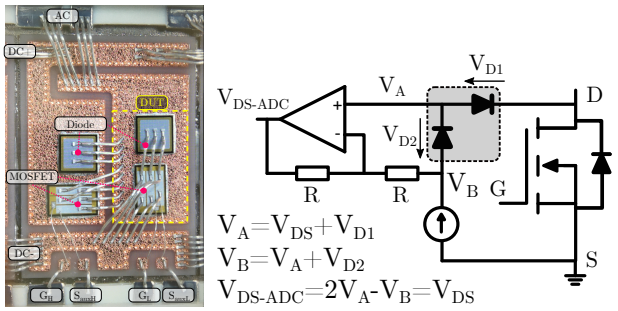


Fig. 2. (a) Internal layout of the power module and (b) circuit implementation of the monitoring system for V_{DS}.

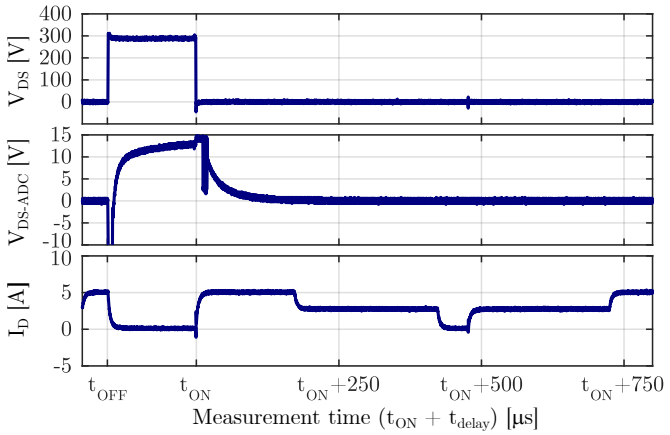


Fig. 3. Osciloscope measurement of the on-state voltage measured on the module terminals V_{DS}, the on-state voltage measured at the input of the ADC $V_{\mathrm{DS-ADC}}$ and circulating current I_{D} after turn-on.

source polarizes the two diodes D_1 and D_2 through the power semiconductor. An important fact is that the voltage through the diodes has to be equal, hence both should be matched and thermally-coupled to minimize the error. Moreover, during the off-state, the current cannot flow through the power switch. Hence, the diodes must be able to block the DC-Link voltage to protect the rest of the monitoring system.

The ADC employed for the measurements has 16-bit with input voltage of +-5V, resulting in a resolution of 0.15 mV. Its output is transmitted through fiber optics to the digital controller, and sent in a PC via RS-232. Regarding the current, it is measured with a hall-effect current transducer. The digital controller is in charge of synchronizing the PWM and monitoring signals, in order to perform the monitoring when desired.

The monitoring circuit requires a certain settling time in order to get accurate measurements. This is shown in Figure 3, where the drain-to-source voltage of the DUT V_{DS}, the voltage at the input of the ADC $V_{\mathrm{DS-ADC}}$ and the drain current I_{D} measured with an oscilloscope are shown. The measurements where captured with the DUT switching at 1 kHz with Sinusoidal PWM (SPWM) modulation and a unitary modulation index. When the DUT is in the off-state, its drain to source voltage is the DC-Link voltage, while at the input of the ADC $V_{\mathrm{DS-ADC}}$ rises to the saturation voltage of the Op-Amp. Furthermore, when the DUT is turned on, V_{DS} falls to the on-state voltage defined by the circulating current I_{D} and the junction temperature. Although an operational amplifier with 9 MHz bandwidth has been employed for the circuit, the current source, the parasitic capacitances of the diodes and the ADC imposes a certain delay between the switch on of the device and the measurement. This minimum on-state time required for monitoring limits both the modulation index and the switching frequency of the DUT, reducing the operating points of the inverter and not taking advantage of the fast switching capabilities of SiC.

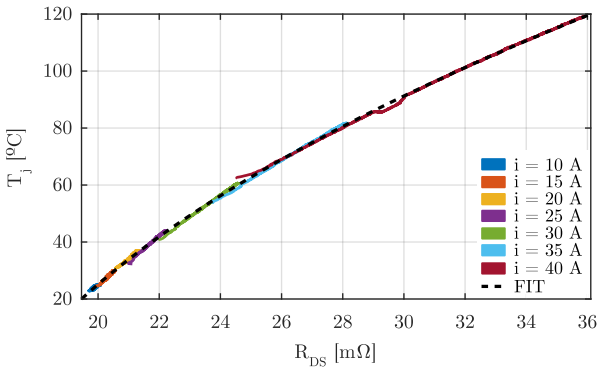


Fig. 4. Results of the thermal characterization with DC-currents and $R_{\mathrm{DS}} - T_{\mathrm{j}}$ correlation.

C. Thermal Characterization of the DUT

In order to demonstrate the feasibility of employing the on-state resistance as a TSEP, a thermal characterization test employing DC-currents and an IR camera has been carried out with the prototype. To do this, a sample module has been opened and the soft-gel that covers the active switches and the copper pad removed with a solvent. Afterwards, the module has been painted with high-temperature black paint in order to equalize the emissivity of the surface [32].

The test consisted on forcing DC-currents through the DUT while a constant positive voltage (20 V) is applied to its gate in order to dissipate conduction power losses [32]. This way, a self-heating is generated in the DUT while measurements are acquired [33], such as in a converter during operation. The monitoring system monitors once a second both V_{DS} and I_{D}, while the IR camera monitors the junction temperature.

The measurement results of the correlation between R_{DS} and T_{j} are shown in Figure 4. A curve-fitting has been employed to extract the relation between them. A second-order polynomial has been employed for the correlation, as the one in [29], resulting in the expresion:

$$T_{\mathrm{j}} = a\,R_{\mathrm{DS}}^2 + bR_{\mathrm{DS}} + c \tag{1}$$

where $a = -1.4539 \times 10^5$, $b = 1.5067 \times 10^4$ and $c = -252.1657$ are the curve-fitting parameters.

It is worth to mention that this correlation will be dependent on degradation state of the gate oxide of the DUT. Concretely, significant threshold voltage V_{TH} shifts have been reported due

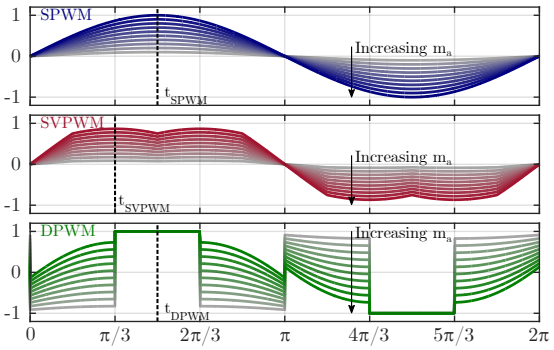


Fig. 5. Fundamental signals of the modulation strategies SPWM, SVPWM and DPWM for different modulation indexes and monitoring instants (dashed lines).

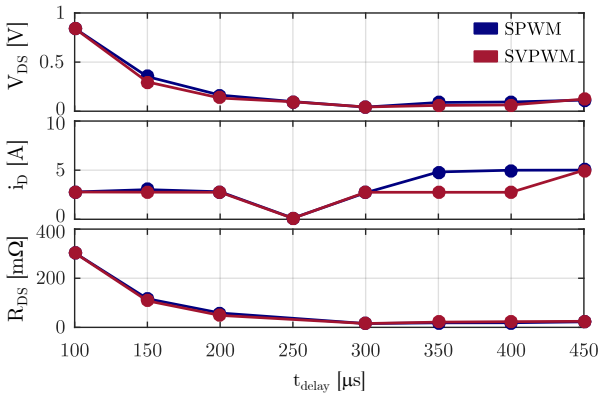


Fig. 6. Measurement results of the on-state voltage V_{DS}, the circulating current I_{D} and the resulting on-state resistance R_{DS} with SPWM and SVPWM modulations and varying t_{delay} after turn-on.

to bias temperature instabilities, caused by trapped charges in the oxide and its interface [34]. In power MOSFETs, the R_{DS} is mainly composed of three terms: channel, JFET and epitaxial layer resistance. A positive shift in the threshold voltage of a die results in a lower gate overdrive $V_{\mathrm{GS}} - V_{\mathrm{TH}}$, which is further reflected in an increase of the channel resistance [35]. This matter is specially relevant for SiC MOSFETs, since for these devices the channel resistance can make up to $50\,\%$ of the total resistance [36].

Although results in [37] show the improvement of the gate oxide ageing of SiC MOSFETs along generations, a change in the temperature coefficients of (1) is expected [38]. In order to overcome this issue, it is proposed in [39] an indicator of the V_{TH} shift based on the forward voltage of the body diode. This technique could be implemented during maintenance or in an intelligent gate-driver in order to detect the degradation of the gate oxide and carry-out a recalibration.

III. Modulation Strategies

A. Monitoring with Standard Modulations SPWM and SVPWM

As introduced above, the monitoring system limits the maximum switching frequency that can be achieved. In order to determine the settling time required, the prototype has been tested with both standard SPWM and Space Vector PWM (SVPMW) modulation strategies. Figure 5 shows the SPWM and SVPWM fundamental signals employed to generate the PWM commands in one of the half-bridge branches of the three-phase inverter for various modulation indexes. Here, the modulation index m_{a} is defined as:

$$m_{\mathrm{a}} = \frac{2V_1}{V_{\mathrm{DC}}} \tag{2}$$

where V_{DC} is the DC-Link voltage and V_1 is the fundamental peak phase voltage. The signals for the other two branches are obtained by shifting the signal shown.

The digital controller is in charge of synchronizing the measurement command signals and the PWM in such a way that the monitoring is performed during the switching period with the maximum on-state time. Therefore, the measurement instants for each modulation ($t_{\mathrm{SPWM}}, t_{\mathrm{SVPWM}}, t_{\mathrm{DPWM}}$) are shown in Figure 5, corresponding to the largest on-time of the DUT.

In Figure 6, the results of the measurements with SPWM and SVPWM, 2 kHz switching frequency and 0.95 modulation index are presented. In these tests, the time delay (t_{delay}) is defined as the elapsed time between the switch on of the DUT (t_{ON} in Figure 3) and the measurement acquisition time (t_{meas}):

$$t_{delay} = t_{meas} - t_{ON} \tag{3}$$

This parameter is varied from 100 to 450 μs in order to determine the minimum delay that ensures an accurate measurement. Figure 6 shows that the current measurement varies from 5 to 0 A during one switching period. This is caused by the intentionally low switching frequency employed for this test relative to the output phase inductance, as shown in Figure 3. The low switching frequency ensures long on-state periods to perform the measurements. As a consequence, the calculated R_{DS} at $t_{\mathrm{delay}} = 250\,\mu s$ has not been plotted in Figure 6 since the current was too low for the calculation. This can also be distinguished in the V_{DS} measurements for $t_{\mathrm{delay}} = 350$ and $400\,\mu s$, in which the current in SPWM is higher than in SVPWM, resulting in higher V_{DS}. However, the measured R_{DS} is not affected. Furthermore, the low bandwidth of the monitoring system involves a settling time of at least 350 μs in order to obtain a stable measured R_{DS}. This low bandwidth reduces the commutation noise that could alter the measurements. However, it limits the maximum switching frequency to 3 kHz, far below the frequencies reported in literature for SiC-based converters.

B. Proposed Modulation Strategy

In order to perform the measurements accurately, the modulation strategy can be modified, with the objective of avoiding the switching of the DUT and hence satisfy the required settling time. For the presented three-phase inverter, this can be obtained by implementing a Discontinuous PWM (DPWM) modulation, in which each switch of the three phase inverter

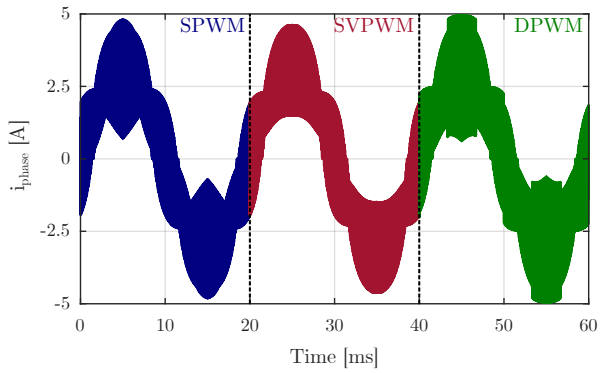


Fig. 7. Simulated output phase current i_{phase} of the inverter for SPWM, SVPWM and DPWM modulation strategies, 50 Hz fundamental frequency, 50 kHz switching frequency and unitary modulation index.

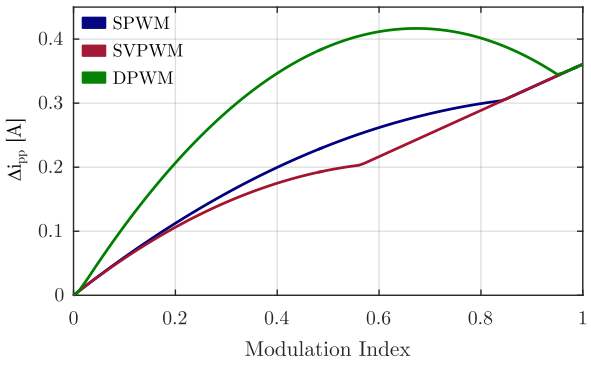
does not commutate during 1/6 of the fundamental period. Although this modulation is not novel [40], to the authors knowledge it has not been employed for condition monitoring before.

Figure 5 shows the fundamental signal for this modulation. As can be seen, between $\pi/3$ and $2\pi/3$ the signal corresponding to DPWM goes over 1 and hence during this time the switch does not commute. This fact is independent of the modulation index, allowing the CMS to measure at any operating point of the converter.

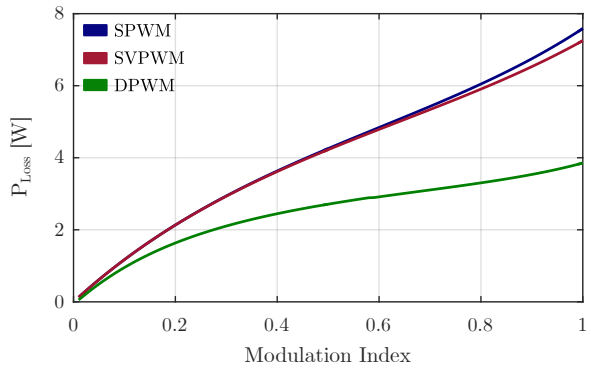
As a consequence of altering the modulation strategy, the output phase voltages are varied and so do the output phase currents. However, since in the proposed modulation a homopolar signal is injected, the fundamental current is not affected. This is illustrated in Figure 7, where the phase current of the prototype for SPWM, SVPWM and DPWM modulations considering 50 Hz fundamental frequency, 50 kHz switching frequency, unitary modulation index and a $L_{\text{Filter}} = 120\,\mu H$ are shown. A lower L_{Filter} has been employed here intentionally to increase the current ripple and show the differences. It can be seen that the current ripple at the switching frequencies is affected, but the fundamental phase current remains the same.

In order to study the high-frequency ripple along the modulation index for each modulation strategy, the system is simulated and the output current extracted. From the later, the fundamental frequency harmonic is removed and the peak-to-peak current ripple Δi_{pp} is determined. The results are shown in Figure 8(a). It can be seen that the ripple current with DPWM is higher than with the other choices for low- and medium-modulation indexes. Concretely, the increase achieves 85 % with respect to SPWM for $\text{m}_\text{a} = 0.15$ and 100 % with respect to SVPWM for $\text{m}_\text{a} = 0.56$. Moreover, for $\text{m}_\text{a} > 0.80$ the resulting high frequency ripple current increase is below 40 %, while for $\text{m}_\text{a} > 0.94$ it is equal for the three modulation strategies.

As mentioned above and reported in the literature [41], [27], [28], the use of DPWM is particularly targeted for the reduction of power losses. In order to quantify this advantage, the power losses in the semiconductors P_{Loss} have been calculated



(a)



(b)

Fig. 8. Comparison of the studied modulation strategies at 50 kHz switching frequency and varying modulation index in terms of (a) peak-to-peak high frequency ripple current Δi_{pp} and (b) MOSFET power losses P_{Loss}.

employing the available datasheet characteristics. Figure 8(b) compares the results for the three studied modulations. While losses in SPWM and SVPWM are similar, a drastic reduction of the power losses is achieved with DPWM. This reduction increases with the modulation index, being higher than 45 % for $\text{m}_\text{a} > 0.9$ The reason is the saturation of the modulation signal during 1/6 of the fundamental period, shown in Fig. 5, which causes that the switch does not switch during that time. Hence, no switching losses are generated, which is highly beneficial when switching at high frequencies.

IV. Monitoring Results with DPWM

In this section, the results of the implementation of the proposed DPWM in the presented prototype are shown. Figure 9 shows the measured output of the inverter prototype with DPWM implemented: the output phase currents and the drain-to-source voltage of the DUT. The measurements are presented for low, medium and high (0.2, 0.6 and 1) modulation indexes m_a in Figures 9(a) to 9(c), respectively. It can be seen that the V_{DS} of the DUT is held in the DC-Link voltage during 1/6 of the fundamental period and at its saturation voltage during another 1/6. Moreover, the filtered V_{DS} reflect the employed modulation signal.

The results of the high-frequency ripple current of the proposed modulation have been compared with those of the

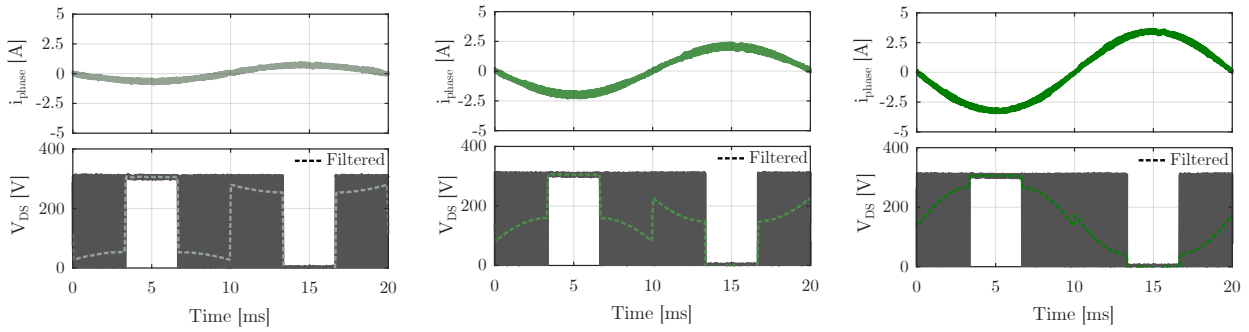


Fig. 9. Inverter output phase current i_{phase} and drain-to-source voltage V_{DS} of the DUT with DPWM at switching frequency $f_{\text{sw}} = 50\,kHz$ and different modulation indexes m_{a}: (a) $m_{\text{a}} = 0.2$, (b) $m_{\text{a}} = 0.6$, (c) $m_{\text{a}} = 1.0$.

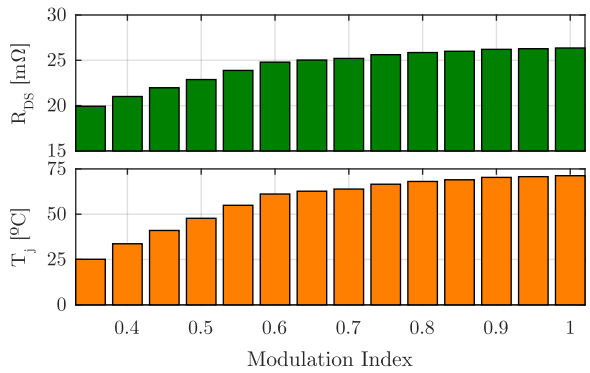


Fig. 10. Measurement results of the on-state resistance R_{DS} and temperature estimation T_{j} at switching frequency $f_{\text{sw}} = 50\,kHz$ and varying the modulation index.

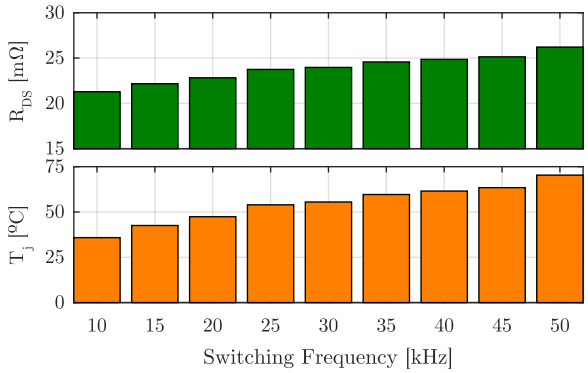


Fig. 11. Measurement results of the on-state resistance R_{DS} and temperature estimation T_{j} at modulation index $m_{\text{a}} = 0.95$ and varying the switching frequency.

TABLE II
RIPPLE CURRENT CALCULATION COMPARISON.

m_{a}	Calculated Δi_{pp} [A]	Measured Δi_{pp} [A]	Error [%]
0.2	5.79	5.11	11.72
0.6	10.47	10.19	2.64
1.0	9.31	8.93	4.06

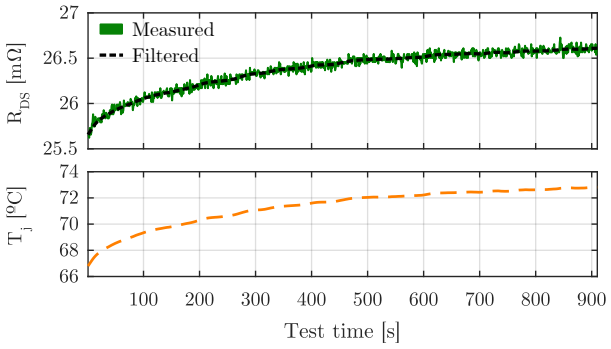


Fig. 12. Measurement results of the on-state resistance R_{DS} and temperature estimation T_{j} in long-term monitoring test at $f_{\text{sw}} = 50\,kHz$ and $m_{\text{a}} = 0.95$.

prototype considering a $L_{\text{Filter}} = 120\,\mu H$. Again, a lower L_{Filter} has been employed in order to increase the current ripple and hence reduce measurement errors. From the phase current measured with a current probe (Tektronix TCP305-A), the FFT has been calculated, then the terms at the fundamental frequency neglected and finally the current has been reconstructed via inverse FFT to determine the high-frequency peak-to-peak phase current ripple. The measured and calculated results, presented in Table II, shown a maximum error of 11.72 % at low modulation index.

Monitoring tests have also been carried out in order to verify the performance of the monitoring system at different operating points. Figure 10 shows the measurement results of the R_{DS} acquired with the device switching at 50 kHz for a modulation index range between 0.35 and 1. The results show how the acquired R_{DS} increases with the modulation index due to the higher circulating current, which causes more power losses. This is reflected in an increase of the junction temperature, estimated through the correlation presented in (1).

Moreover, in Figure 11, the results of a test in which the switching frequency is varied between 10 and 50 kHz while the modulation index is maintained at $m_{\text{a}} = 0.95$ are presented. Again, increasing the switching frequency involves higher power losses, resulting in higher measured R_{DS} and higher estimated junction temperatures.

Finally, Figure 12 presents the long-term monitoring results of the prototype tested at $f_{\mathrm{sw}} = 50\,kHz$ and $m_{\mathrm{a}} = 0.95$. Here, measurements are acquired once per second, and then translated to temperature. The temperature increase during the test is patent.

V. Conclusions

This paper presents a condition-monitoring system based on discontinuous PWM targeted for three-phase inverters operating at high switching frequencies. Employing this modulation, the device does not switch during part of the fundamental period of the inverter. This way, the output of the V_{DS} monitoring circuit is stable, and measurement accuracy is not compromised. However, power losses and output phase currents are also affected.

An inverter prototype has been designed, and the limitations of the monitoring with regular modulations have been presented. A 350 μs minimum on-state time has been determined for correct measurement, which limits the switching frequency and modulation index of the DUT. The proposed modulation is presented to overcome this issue and compared with the previous modulations in terms of current ripple and power losses. While high-frequency phase current ripple is increased, the power losses are drastically reduced due to the absence of commutation during 1/6 of the fundamental period.

Measurement results are presented with the proposed modulation in an inverter for various operating points. Moreover, based on a thermal characterization test carried out on a sample module, an online estimation of the junction temperature has been carried out.

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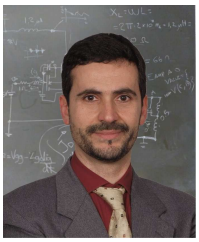

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