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SiC-Based High Efficiency High Isolation Dual Active Bridge Converter for a Power Electronic Transformer

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Received: 30 January 2020; Accepted: 1 March 2020; Published: 5 March 2020

Abstract: This paper discusses the benefits of using silicon carbide (SiC) devices in a three-stage modular power electronic transformer. According to the requirements to be fulfilled by each stage, the second one (the DC/DC isolation converter) presents the most estimable improvements to be gained from the use of SiC devices. Therefore, this paper is focused on this second stage, implemented with a SiC-based dual active bridge. Selection of the SiC devices is detailed tackling the efficiency improvement which can be obtained when they are co-packed with SiC antiparallel Schottky diodes in addition to their intrinsic body diode. This efficiency improvement is dependent on the dual active bridge operation point. Hence, a simple device loss model is presented to assess the efficiency improvement and understand the reasons for this dependence. Experimental results from a 5-kW Dual Active Bridge prototype have been obtained to validate the model. The dual active bridge converter is also tested as part of the full PET module operating at rated power.

Keywords: SiC devices; antiparallel diode; dual active bridge; power electronic transformer; high-frequency transformer

1. Introduction

A line-frequency transformer (LFT) is a key element in transmission and distribution for traditional centralized generation-based systems. Their main functionality is to interface different voltage levels in the grid [1]. LFTs are a well-established, relatively cheap, and reliable technology. However, they fail to cope with modern grid demands, such as the integration of distributed resources and energy storage systems, as well as power flow control.

The power electronic transformer (PET), also called a solid-state transformer (SST), was introduced in 1970 [2]. It is considered an alternative to LFT, as it connects two AC voltage ports while providing galvanic isolation [1]. PET is a semiconductor-based energy conversion system based on fast-switching devices, which potentially enables a significant reduction in volume and weight [3]. Moreover, thanks to the controllability of the power devices, the PET provides additional functionalities, such as reactive power, harmonics and imbalances compensation, ride-through capabilities, and smart protections.

The power semiconductor technology used in PETs has been traditionally based on Silicon (Si). However, the fast advances in wide-band-gap (WBG), specially the Silicon Carbide (SiC), power semiconductors has attracted the attention to their use in the medium voltage (MV) modular three-stage PETs [4], mainly due to their high blocking voltage along with their superior switching behavior [5,6].

Several examples of using SiC devices in different PET topologies exist in literature [7–13]. In the majority of applications, 1.2/1.7 kV commercial SiC MOSFETs are used for LV side devices, while for HV side, 10 kV non-commercial MOSFETs are used [6,8]. In some works, SiC was used in all the PET stages, such as in the TIPS (transformer-less intelligent power substation), which is an all-SiC

three-stage PET topology [12]. In [14], a detailed comparison was carried out between two cases: (1) using 10 kV and 3.3 kV SiC MOSFETs and, (2) using 10 kV and 3.3 kV Si IGBTs, for different PET topologies. Authors concluded the importance of further research into the combined use of Si IGBT with SiC MOSFETs for three-stage PETs. Moreover, authors hinted at the importance of analyzing the relevance of including a SiC antiparallel diode to justify its additional cost implication.

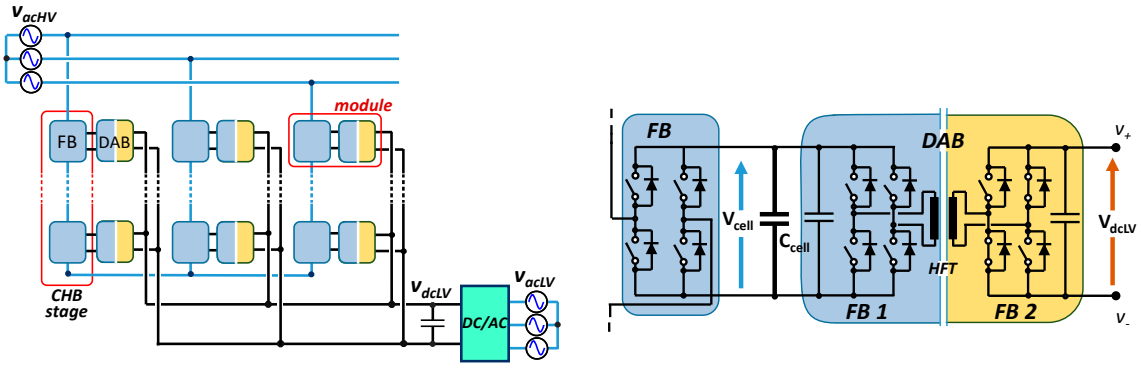
Accordingly, the contribution of this paper is thought in two aspects:

1. Studying the requirements of the devices in each of the PET stages to assess the benefit of integrating SiC and, consequently, identifying the stages making best use of it.
2. Selection of the SiC devices for the second PET stage, based on a dual active bridge converter (DAB). As will be explained, this stage presents the most benefits from using SiC devices. Special attention will be paid to the device operation intrinsic to the converter topology. The use of SiC MOSFETs co-packaged with an additional SiC antiparallel diode is also investigated. A loss model is developed to estimate the potential efficiency improvement in this case. Both devices (i.e., with only intrinsic body diode and with additional SiC diode) are experimentally compared at rated power to validate the proposed model.

The paper is organized as follows: Section 2 describes the selected PET topology. Section 3 studies the integration of SiC devices in the different stages of the PET and identifies the practical limitations to the enhancements introduced by the use of these devices. Section 4 discusses the DAB converter development where the selection of the devices is detailed and the improvements introduced by using a SiC antiparallel diode is studied. Experimental results are provided in Section 5.

2. PET Topology

The selected PET topology is shown in Figure 1, and was previously discussed in [15–20]. It is a three-stage modular PET, with a Cascaded H-Bridge (CHB) converter acting as the front end AC/DC converter providing a HVAC link (V_{acHV}). Each CHB cell integrates a DAB converter to provide the isolation between the HV and LV sides. Moreover, the integration of the DAB to the CHB cell provides the capability of bidirectional power transfer at the cell level [18,19]. The LV outputs of all DABs are connected in parallel to provide a high-current LVDC link (V_{dcLV}), which is connected to a three-phase four-leg (3P4L) converter providing the LVAC link (V_{acLV}).



(**a**) (**b**)

Figure 1. Selected Power Electronic Transformer (PET) structure: (**a**) Three-stage modular PET topology based on a Cascaded H-Bridge (CHB) converter [17]. (**b**) One PET module composed of a Dual Active Bridge (DAB) and the full bridge of the CHB.

As is clear in Figure 1, the structure is fully modular as it is formed by several identically-stacked cells. Thanks to this modular structure, the number of cells of the CHB is chosen in such a way that the cell voltage (V_{cell}) is equal to the required V_{dcLV}. In this way the design of this DAB is, to some extent, simplified using a unity transformation ratio (i.e., no step-up/down).

This PET topology requires high galvanic isolation between HV and LV sides. The isolation is provided by the DAB high frequency transformer (HFT). Table 1 shows the characteristics of the developed PET.

Table 1. Main Power Electronic Transformer (PET) characteristics.

Element	Parameter	Value
PET	Rated power	105 kW
	Number of cells	21 (7 per phase)
	HV/LV grid voltage (L-L)	6 kV/400 V
DAB	Rated power	5 kW
	Switching frequency (f_{sw})	30 kHz
	HFT isolation	24 kV
	Input voltage ($V_i = V_{cell}$)	800 V
	Transformer turns ratio (n)	1:1
	Leakage inductance (L_{lk})	423 µH
CHB	Rated power	5 kW
	C_{cell}	600 µF(film)

3. Use of WBG for PET

The superior material properties of WBG semiconductors allow power devices to operate at higher temperatures, voltages and switching frequency in comparison to Si counterparts [4,21]. Among WBG materials, SiC presents the most mature technology for high voltage devices [4]. Both 1.2 kV and 1.7 kV SiC MOSFETs are already available on the market with a wide range of current ratings [5,22,23]. The use of SiC MOSFETs not only introduces a relevant improvement to the efficiency of fast switching power converters, but also enables going to higher switching frequencies at high blocking voltage which cannot be achieved using available Si IGBTs. However, at limited switching frequency requirements (<10 kHz), especially for high power (>100 A), Si IGBTs are still the preferred choice due to cost-effectivity and reliability in addition to SiC MOSFET higher dv/dt, di/dt, and EMI issues [24].

Accordingly, to analyze the merits of integrating SiC devices in the PET, the device requirements for each of the three stages of the PET are identified below.

3.1. Device Requirements per PET Stage

In the addressed PET topology, since no step-up/down is needed, the power devices employed on both transformer sides (i.e., HV and LV sides) have the same voltage rating. These include devices of the CHB full bridge (FB), the two DAB full bridges (FB1, FB2), and the DC/AC converter devices (see Figure 1). While this is true, the specifications in terms of current ratings and commutation requirements differ significantly.

CHB: its power devices do not need to commutate fast due to the multilevel nature of the topology [25,26]. Moreover, C_{cell} size is not determined by the cell switching frequency. Therefore, SiC switching devices are not of special merit here, even when going to higher V_{cell} (i.e., to reduce the number of stacked modules), still Si IGBT would be the selected option [14]. On the other hand, SiC free-wheeling antiparallel diodes are quite interesting in this case since the CHB full bridge is required to handle positive and negative currents (i.e., not only during the dead time). Therefore, SiC diodes can effectively improve the CHB efficiency due to their reduced conduction forward voltage drop as well as lower reverse recovery time compared to Si diodes [27].

DAB: high switching frequencies can provide significant reduction of the size and weight of the converter magnetics and the input and output capacitors. Additionally, going to higher PET module voltage is not achievable using Si devices, unless the switching frequency is reduced to few kHz. Regarding the antiparallel diode, the advantages of using SiC are still a controversial issue [14,28] and, therefore, will be analyzed in this work.

3P4L DC/AC: commutation requirements are not high (in the range of few kHz [29]), and since it interfaces the LVAC grid, high blocking voltages are not required. Therefore, Si devices are a good candidate for this stage.

Considering the above discussion, for this PET, 1.7 kV Si IGBT devices with SiC freewheeling diodes are used for the CHB FB. As for the DAB, 1.2 kV SiC MOSFETs are used and possible enhancements introduced by a SiC antiparallel diode will be discussed in detail in Section 4. Finally, 1.7 kV Si IGBTs are used for the 3P4L converter.

In the next section, the possible achievable enhancements gained by employing SiC in the DAB are discussed highlighting the practical limitations intrinsic to this PET topology.

3.2. Benefits and Practical Limitations of Using SiC MOSFETs for the DAB Converter

The use of SiC MOSFETs for the DAB converter in this PET structure has two main benefits:

1. It enables increasing the switching frequency of the DAB and, therefore, decreasing the size of the HFT [30,31].
2. The high blocking voltages enable increasing V_{cell} and, therefore, for a given V_{acHV}, the number of stacked PET modules can be reduced (see Figure 1) [7,17]. This is also advantageous for the HFT. Since each module handles more power, this leads to a higher transformer power density. In order to see clearly the effect of this, Figure 2 shows the HFT power density as a function of the cell voltage where the PET total power and V_{acHV} are fixed (i.e., the number of PET modules vary). A comparative analysis regarding this relation is previously presented in [17] showing an improvement in the HFT power density as V_{cell} increases.

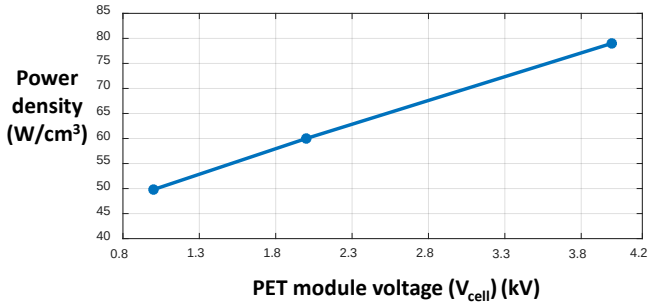


Figure 2. Theoretically calculated High Frequency Transformer (HFT) power density for three designs varying the Power Electronic Transformer (PET) module voltage (V_{cell}) and the handled power [17].

However, these SiC potential benefits may be compromised by certain practical implementation constraints.

On one hand, increasing V_{cell} has several adverse effects. High DC link voltages create practical problems for feeding the control circuitry in each cell. As commercial auxiliary power supplies (APS) do not provide the required isolation [29], each module circuitry has to be supplied from its DC link, where the HV and LV sides have separate APSs [32]. Commercial APSs can be used for voltages under 1 kV, otherwise, custom solutions must be implemented, such as the modular ISOP topology proposed in [29]. Consequently, various aspects must be considered for the selection of V_{cell}.

On the other hand, the size reduction of the HFT, in this particular case, is constrained by the high isolation required by the PET. This isolation imposes minimum clearance distances between windings, which compromises the window utilization factor resulting in a physical limit on further size reduction.

4. SiC-Based DAB Converter

The DAB (see Figure 3) is selected for the intermediate stage of the PET, as it provides galvanic isolation as well as bidirectional power flow [33,34]. The DAB is based on two active bridges interfaced

through an HFT, which provides the required galvanic isolation. This converter provides bidirectional operation by controlling the phase shift between the AC voltages generated by both bridges (V_1 and V_2). Also, this converter can have relatively high efficiency due to the soft-switching operation of all the devices at nominal conditions (zero-voltage switching, ZVS) [35,36].

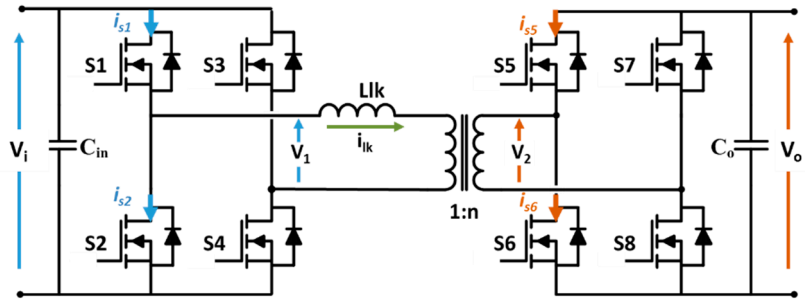


Figure 3. Dual active bridge (DAB) converter schematic.

4.1. SiC Device Selection

Regarding the selection of the SiC devices for the DAB, 6.5, 10, and 15 kV SiC MOSFETs have been reported for laboratory prototypes [37–42], but are far from being a viable commercial alternative yet. Current ratings offered in commercially available 1.7 kV SiC MOSFETs are still limited [23], and their commutation characteristic must be improved. The 1.2 kV SiC devices remain as the most mature technology available in the SiC device market. Consequently, these devices have been selected for the DAB. The DC link voltage is, therefore, set to 800 V.

Seven 1.2 kV SiC commercial MOSFETs were selected; two power modules and five discrete N-channel SiC MOSFETs. A comparative analysis of these devices was carried out in a boost converter operating in continuous conduction mode (CCM) (see Figure 4).

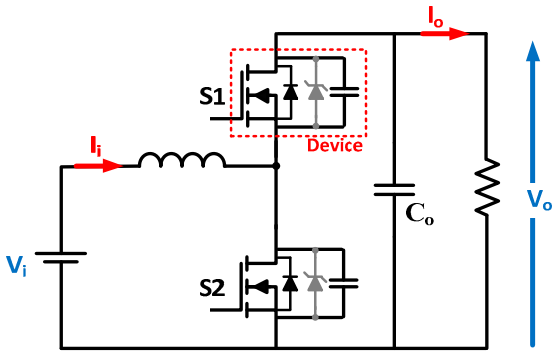


Figure 4. Boost converter test bench schematic.

The boost converter was chosen as a preliminary test bench due to its simplicity and rapid prototyping, but foremost, due to its similar operation to a DAB converter as it has two switching devices in a leg with an inductance connected to the middle point. However, the differences in operation between a CCM boost and a DAB are well understood and, therefore, perspective devices resulting from the first selection stage are then tested in a DAB converter prototype.

The test bench used commercial driver boards from CREE and a commercial FPGA-based controller platform (BASYS2). Tests in the boost converter were done at 2 kW 400/800 V for switching frequencies of 30, 50, and 100 kHz and a dead time of 500 ns. Table 2 summarizes the results. The efficiency is calculated using the input and output DC voltages and currents of the converter measured using digital multimeters. It is observed that all the devices show a high efficiency barely affected by the increase in switching frequency which was increased by a factor of more than three.

Table 2. SiC MOSFET comparative analysis in a boost converter.

Manufacturer	Reference	Package	Rated Current @100 °C (A)	R_{DS} (mΩ)	C_{out} (*p*F)	Efficiency (%)			Price per Bridge (€)
						30 kHz	50 kHz	100 kHz	
ST	SCT30N120	TO-247-3	34	80	130	97.77	98.16	97.81	100
ROHM	SCH2080KE + SBD		28	80	175	97.71	98.02	97.69	132
	SCT2080KE		28	80	77	97.82	98.17	97.93	80
CREE	C2M0040120D		40	40	150	97.76	98.10	97.84	128
	C2M0025120D		60	25	220	97.56	97.88	97.42	252
	CAS120M12BM2 + SBD	6-pack 45 mm	59	25	400	97.49	97.54	97.50	412
	CCS050M12CM2 + SBD	Half-bridge 62 mm	138	13	900	96.44	95.8	-	660

Since the performance of all seven MOSFETs is comparable, the selection of the adequate option was mainly based on the size and the price. The specifications for the DAB converter are shown in Table 1. Accordingly, the peak current handled by the devices can be calculated from Equation (1) [35], where T is half the switching period, d is the phase shift, L_{lk} is the leakage inductance, v_o is the output voltage, v_i is the input voltage and n is the HFT turns ratio:

$$I_{p\_lk} = \frac{T}{2L_{lk}}\left(2\frac{v_o}{n}d + v_i - \frac{v_o}{n}\right) \quad (1)$$

The current peak is calculated for the maximum phase-shift, this is selected to be 0.35 according to [35]. Based on Equation (1), this current is approximately equal to 11 A. The device current rating is selected to be twice the magnitude of the peak current handled by the devices to keep a safety margin. Therefore, the minimum required current rating is 22 A. This eliminates the two modules, and the CREE 60 A discrete, as the size and price are not justified in this case. The remaining four discrete devices are almost equally favored except for the ROHM SCH2080KE, as it includes a SiC Schottky barrier diode (SBD) co-packaged with the MOSFET.

4.2. Antiparallel SBD for a DAB Converter

Observing the efficiency of the boost converter using ROHM SCH2080KE versus for example ROHM SCT2080KE (without an additional SBD), it is consistently higher without SiC SBD. For the boost converter, this is logical as an additional antiparallel diode increases the output capacitance (see Table 2) and since hard-switching occurs, this increases the switching losses. Although, this makes sense and is simple to understand for the boost, for the DAB, it is more complicated as ZVS is implemented. That being the case, it is not valid to make a selection between both devices unless the additional diode behavior is studied for the DAB operation to identify if it improves or worsens its efficiency. This issue is addressed as follows, including: (1) understanding the potential effects introduced by a SiC antiparallel diode in a DAB converter, (2) developing a simple analytical loss model to estimate the possible efficiency improvement introduced by the SiC diode at a certain DAB operating point, and (3) validation of the proposed model using experimental results in a DAB prototype.

The two devices used in the analysis are the ROHM devices (i.e., SCH2080KE and SCT2080KE) as it is the same die but one packed with a SiC antiparallel SBD [22]. Characteristics of both devices are provided in Table 3. The diode forward voltage, $V_{F\text{-}diode}$, is obtained from the datasheet at the value of I_{p_lk} (see Equation (1)) where the employed phase shift is that corresponding to 5 kW.

Table 3. Specifications of the compared devices.

Characteristics		SCH2080KE +SBD	SCT2080KE
$R_{ON\text{-}MOSFET}$		125 mΩ	
E_{off} (R_g = 10 Ω)		110 µJ	120 µJ
E_{on} (R_g = 10 Ω)		330 µJ	275 µJ
Anti-parallel diode	Type	SiC SBD	Body diode
	R_D (Estimated)	45 mΩ	320 mΩ
	V_{knee}	0.85 V	1.4 V
	$V_{F\text{-}Diode}$ (@ I_{p_lk})	1.2 V	4.5 V

4.2.1. Advantages and Disadvantages of an Additional SBD

In order to provide a qualitative preliminary understanding of the possible effects of the SiC SBD on the DAB efficiency, the waveforms of the DAB are shown in Figure 5.

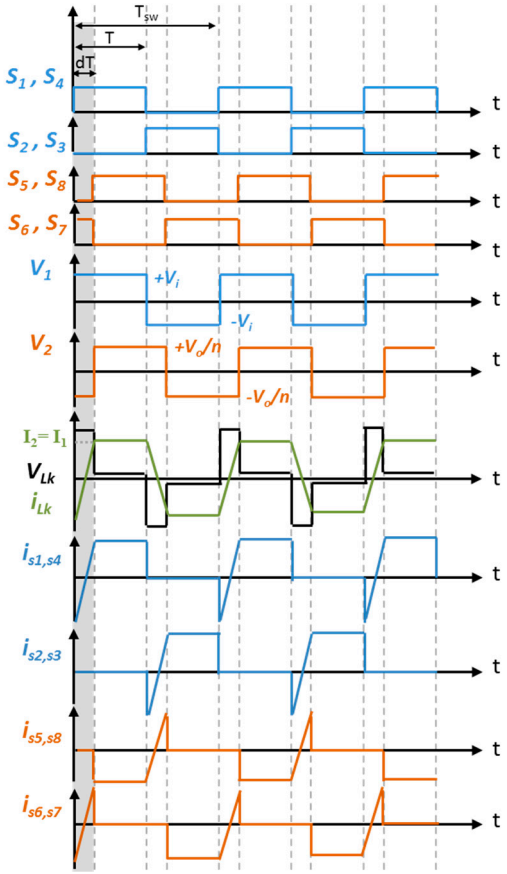


Figure 5. Dual Active Bridge (DAB) converter waveforms.

The potential advantages of using SCH2080KE +SBD in comparison to SCT2080KE are analyzed as follows:

- Since $V_{F\text{-}Diode}$ of the additional SiC SBD is more than three times lower than that of the body diode (see Table 3), the power losses due to diode conduction during the dead times are lower using SCH2080KE +SBD.
- The diode can enter into conduction while the MOSFET is ON. This can be seen from Figure 5, when the current through the MOSFET is negative (i.e., source to drain), a forward voltage drop,

$V_{F\text{-}MOSFET}$, is applied to the diode. If $V_{F\text{-}MOSFET}$ is higher than the diode knee voltage (V_{knee}), then the diode conducts. If this case is true, current is shared between the MOSFET and the diode and, therefore, conduction losses are reduced.

- Unlike boost converter operation, soft switching is adopted in DAB devices at turn ON and, therefore, the additional output capacitance introduced by the additional SiC diode, illustrated in Figure 4, does not significantly penalize the switching losses (see Table 2).

However, these advantages can be compromised by several situations resulting in almost no advantages of having a SiC SBD, these cases are summarized as follows:

- From Figure 6, diodes do not operate during the whole period of the dead time. During (A), the output parasitic capacitances of the MOSFETs (see Figure 4) in one leg are exchanging the voltage (i.e., one is discharging while the other is charging) and during (B), diodes conduct due to circulating currents. In some cases, (B) can tend to zero depending on the value of the current charging/discharging the parasitic capacitors and on the dead time.
- If the current through the MOSFETs is not high enough to produce a $V_{F\text{-}MOSFET} > V_{knee}$, then the diode will never conduct during MOSFET ON time.
- The turn OFF switching losses should be analyzed as the enhancement introduced by the SiC SBD in the conduction losses can, in some cases, be compromised by the increase in turn OFF switching losses (due to the extra capacitance).

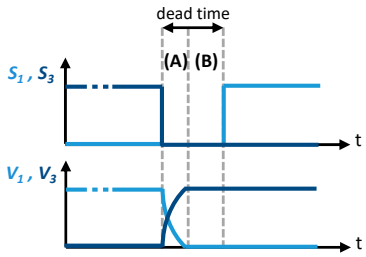


Figure 6. Waveforms of the gates and drain to source voltages of two MOSFETs in one leg during the dead time period.

As a conclusion to the previous discussion, it is important to develop a simple model to determine, for a certain DAB operation point, if an extra antiparallel SiC diode co-packed with the SiC MOSFET is worthy or avoiding it is better. This is introduced in the next section.

4.2.2. Model to Assess the Efficiency Improvement Using a SiC Diode

Diode Conduction Intervals

Regarding diode conduction interval during the dead time, in order to estimate the time duration (B) (see Figure 6), the capacitor charging time during (A) is estimated using Equation (2), where $C_{o(er)}$ is the MOSFET effective output capacitance given by the data sheet and $V_1 = V_i = V_o$. Accordingly, i_{lk} is considered flat ($I_1 = I_2$ in Figure 5) and, therefore, as an approximation, the peak current (I_{p_lk}) is considered to be equal during all the switching transitions.

$$t_{(A)} = 2\frac{V_1\, C_{o(er)}}{I_{p\_lk}} \tag{2}$$

Since $t_{(B)}$ = dead time − $t_{(A)}$, therefore diode operates for 570 ns for the case of the SiC SBD and 588 ns for the body diode. This time represents around 95% of the total dead time (600 ns) and, therefore, the reduction in conduction losses during diode operation is relevant to consider.

Regarding the diode conduction interval during MOSFET ON time, first, the diode characteristics are identified from the MOSFET datasheet (see Table 3). Figure 7 shows the forward voltage drop for both diodes ($V_{F\text{-}Diode}$) as a function of the current through the diode. Additionally, the voltage drop on the MOSFET due to its ON resistance ($V_{F\text{-}MOSFET}$) as a function of the current it is conducting is illustrated.

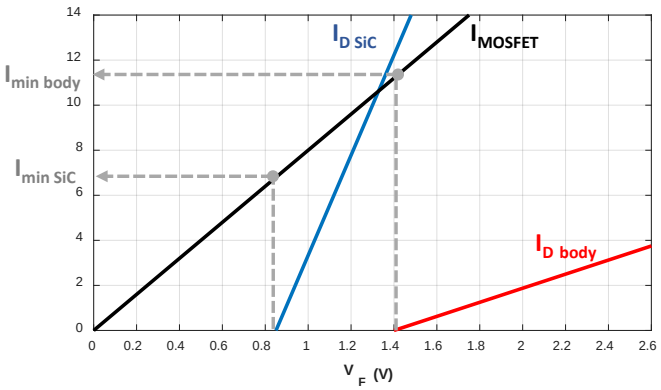


Figure 7. MOSFET voltage drop and diode characteristic curve for the SiC Schottky Barrier Diode (SBD) and the body diode.

It is possible to see that each diode conducts when the current through the MOSFET is above a certain minimum value. It is clearly lower in the case of the SiC SBD. This can be estimated from Equation (3), where $R_{ON\text{-}MOSFET}$ stands for ON-state drain-to-source MOSFET resistance:

$$I_{min} = \frac{V_{knee}}{R_{ON-MOSFET}} \tag{3}$$

Based on the data in Table 3, $I_{min\ SiC}$ is 6.8 A while I_{min} body is 11.2 A. Since the theoretical calculated I_{p_lk} = 9 A, therefore it is not possible that the body diode enters into conduction while the MOSFET is ON. On the other hand, the SiC diode would conduct when the current exceeds 6.8 A.

Estimation of the Power Losses

Power losses are estimated for both cases of the DAB using MOSFETs with a SiC antiparallel diode (SCH2080KE) and with only the body diode (SCT2080KE). Theoretical power loss estimation will be compared to the experimental efficiency results presented in the next section.

First, the periods where the diode can conduct (when it is forward biased) are identified as shown in Figure 8. It can be seen that, the diodes of all the ON MOSFETs can conduct during (1) and (4) as the current through all the devices is negative (see Figure 5), while during (3) and (6) only the diodes of the secondary bridge can conduct.

Accordingly, to simplify the power loss estimation the following assumptions are made:

- As $I_{min\ SiC}$ is around 75% of $I_{pk\text{-}lk}$, therefore, it is assumed that the diode operates only during period (3) and (6) when the peak current is passing through the devices (periods (1) and (4) are neglected).
- The power loss estimation is performed only during the periods with different operation for the case of the SiC SBD and the body diode. In other words, only the difference in losses between both cases is considered. These intervals are: (3), (6) and the dead times.

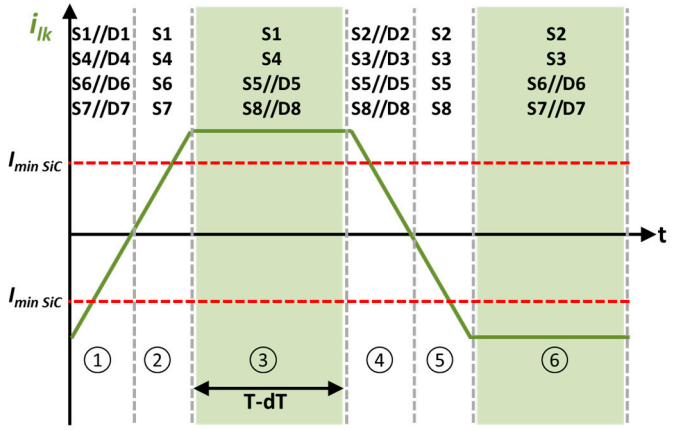


Figure 8. Current through the power transfer inductance of the Dual Active Bridge (DAB) showing periods where the antiparallel diode can enter into conduction mode during MOSFETs conduction.

During intervals (3) and (6), the conduction and switching losses of all the devices are estimated, while during the dead times, only the diodes conduction losses are estimated.

(a) Losses during dead time:

During one switching period (T_{sw}), four intervals of dead time take place. During each interval two diodes conduct. Accordingly, the diodes total conduction losses are estimated using Equation (4), where $V_{F\text{-}Diode}$ is the diode forward voltage at I_{p_lk} obtained from the diode characteristic curve given by the datasheet (linearized in Figure 7).

$$P_{deadtime} = 8 \cdot V_{F-Diode} \cdot I_{p\_lk} \cdot \frac{t_{(B)}}{T_{sw}} \tag{4}$$

(b) Losses during interval (3) and (6) (Figure 8):

Losses during these two intervals are divided into: (1) turn OFF switching losses (P_{sw}) and (2) MOSFET and diode conduction losses (P_{MOSFET} and P_{Diode}). The switching losses are straightforward, estimated from MOSFET E_{OFF} using Equation (5).

$$P_{sw} = 8 \cdot E_{OFF} \cdot f_{sw} \tag{5}$$

On the other hand, conduction losses are not straight forward. As noticed from Figure 8, in both (3) and (6) intervals, the primary bridge devices are different from the secondary ones. For example, during (3), for the primary, only the MOSFETs conduct (i.e., all the current flows through the MOSFETs, S1 & S4). In this case, four MOSFETs of the primary bridge conduct during (3) and (6) (two in each interval). Therefore, the total primary conduction losses can be easily estimated using Equation (6).

$$P_{MOSFET-prim} = 4 \cdot {I_{p\_lk}}^2 \cdot R_{ON-MOSFET} \cdot \frac{T - dT}{T_{sw}} \tag{6}$$

However, for the secondary, the current is shared between the diode and the MOSFET (S5, D5 and S8, D8). Accordingly, the current conducted by each element has to be estimated. Since the voltage drop on the MOSFET is equal to the diode $V_{F\text{-}Diode}$, then:

$$I_M \cdot R_{ON-MOSFET} = V_{knee} + I_D \cdot R_D \tag{7}$$

where I_M and I_D are the currents through the MOSFET and the diode respectively and R_D is the diode dynamic resistance.

Since the current is shared by both elements, then, I_M and I_D can be obtained from Equations (7) and (8):

$$I_M + I_D = I_{p\_lk} \tag{8}$$

Finally, the total conduction losses of the secondary bridge during T_{sw} can be calculated from Equations (9) and (10):

$$P_{MOSFET-sec} = 4 \cdot {I_M}^2 \cdot R_{ON-MOSFET} \cdot \frac{T - dT}{T_{sw}} \tag{9}$$

$$P_{Diode-sec} = 4 \cdot I_D \cdot V_{F-Diode}|_{I_D} \cdot \frac{T - dT}{T_{sw}} \tag{10}$$

The values of the power loss components estimated in this section are summarized in Table 4 where the enhancement to the DAB efficiency is estimated to be approximately 0.22% given the rated power is 5 kW.

Table 4. Theoretically-estimated power losses.

Interval	Losses		SCH2080KE +SBD	SCT2080KE
Dead time (600 ns)	Diode conduction ($P_{deadtime}$)		1.6 W	6.2 W
(3) & (6)	Switching (P_{sw})		26.4 W	28.8 W
	Conduction	$P_{MOSFET-prim}$	17.4 W	17.4 W
		$P_{MOSFET-sec}$	10.4 W	17.4 W
		$P_{Diode-sec}$	2.8 W	-
Total losses			58.6 W	69.8 W

4.2.3. Experimental Validation of the Proposed Loss Model

A DAB test bench was constructed and tests were performed at the nominal operation defined in Table 1 and the results are summarized in Table 5.

Table 5. Experimental results of the Dual Active Bridge (DAB) with and without SiC Schottky Barrier Diode (SBD).

Characteristics	SCH2080KE +SBD	SCT2080KE
Antiparallel diode	SiC SBD	Body diode
Efficiency (η)	98.1%	97.8%
Phase-shift (d)	0.29	
Dead time	600 ns	
I_{p_lk}	Calculated from Equation (1): 9 A Measured (experimental): 9.8 A	

It was observed that the measured efficiency of the DAB converter composed of MOSFETs with an additional SiC antiparallel SBD is higher than that with only the body diode. The enhancement observed from the experimental results is around 0.3%, which validates the calculation introduced previously resulting in 0.22%. These results validate the proposed hypothesis and approach.

5. Experimental Results of the PET Module

The developed full-scale PET module is shown in Figure 9. Its structure is that schematically shown in Figure 1b. Table 6 summarize the main components of the PET module.

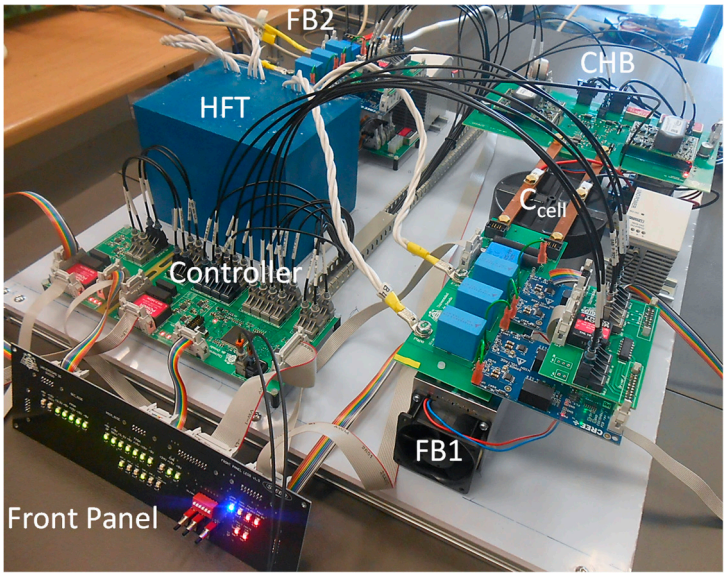


Figure 9. The developed Power Electronic Transformer (PET) module.

Table 6. Main Power Electronic Transformer (PET) module components.

Element	Characteristics	Reference
DAB	ROHM 1.2 kV, 28 A SiC MOSFET CREE 2-channel drivers	SCH2080KE CGD15HB62P1
CHB	Infineon 1.7 kV Si IGBT + SiC diode Infineon two-channel drivers	Not commercial 2ED300C17-S
Controller	Xilinx FPGA (Spartan 3E) custom board	XC3S250E-4TQG144I

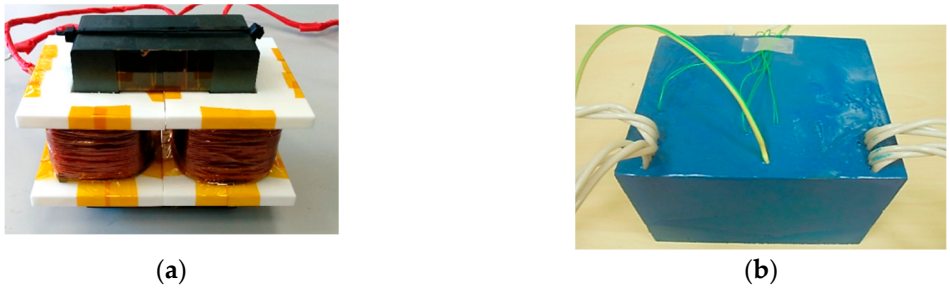
5.1. Developed HFT

One of the key aspects in the design of this HFT is the high galvanic isolation required between its primary and secondary sides, being 24 kV in this PET. This presents significant challenges compared to the ones considered in literature [43,44]. Moreover, the DAB power transfer inductance (L_{lk}) is magnetically integrated in the HFT by making use of its series leakage inductance [43]. This reduces size and cost but, on the other hand, imposes additional constrains on the HFT design due to the required accuracy of L_{lk}.

The HFT design is, therefore, a tradeoff between four variables: transferred power capability, temperature rise (i.e., losses), size and cost. Several design iterations are performed to achieve the required isolation with an acceptable tradeoff between these variables. The HFT design was previously presented in [45]. The main experimental validation tests are provided in this work for completeness.

Figure 10a shows laboratory developed HFT for test purposes and Figure 10b shows the final factory encapsulated HFT. A UU core structure is used typically selected in literature for separate winding [46,47]. The core ferrite material is selected to be Ferroxcube® 3C90 based on the DAB switching frequency [43]. An epoxy resin providing 15 kV/mm and exhibiting acceptable thermal conductance of 3 W/mK was used for encapsulation.

Figure 11 shows a schematic representation of the HFT design from ANSYS PEmag® software (Canonsburg, PA, USA).



(**a**) (**b**)

Figure 10. High Frequency Transformer (HFT) prototype. (**a**) Non-encapsulated laboratory developed using 3D printed bobbins. (**b**) Encapsulated final HFT.

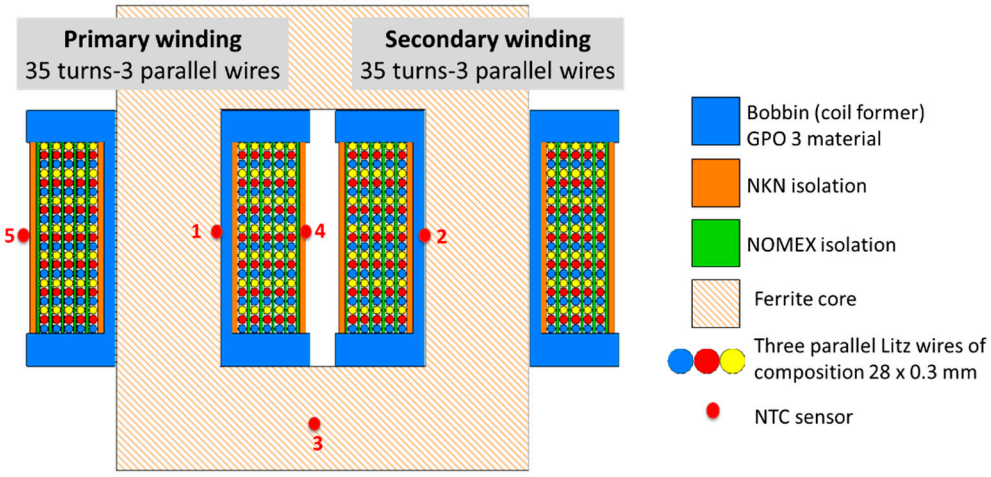


Figure 11. High Frequency Transformer (HFT) design taken from ANSYS PEmag®.

To verify the achieved isolation, a high potential test is done for both porotypes and results are compared. A Hipot tester is used to apply a voltage potential of up to 24 kV between both windings. The leakage current flowing from the winding with the higher potential, through air/resin, is recorded and shown in Figure 12. A significant diversion between both prototypes is clear at higher voltage potentials. Having lower leakage currents means that successive partial discharge due to high dv/dt is avoided which would lead to eventual insulation breakdown [48].

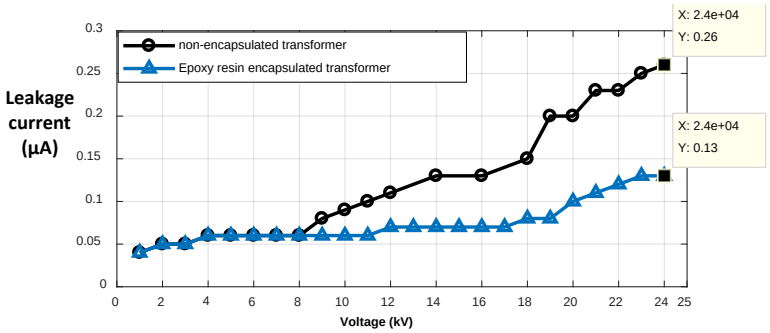


Figure 12. Experimental results. Leakage current measured between High Frequency Transformer (HFT) windings, as a function of the voltage difference between them.

To locate the hottest spot and verify its temperature rise, five NTC sensors were mounted inside the HFT (see Figure 11). The location of this spot differs in encapsulated (NTC 1) and non-encapsulated prototypes (NTC 4). The temperature profile of the encapsulated HFT hottest spot during a four-hour

DAB test at rated operation is shown in Figure 13. The steady state temperature, under natural convection, was recorded to be 60 °C.

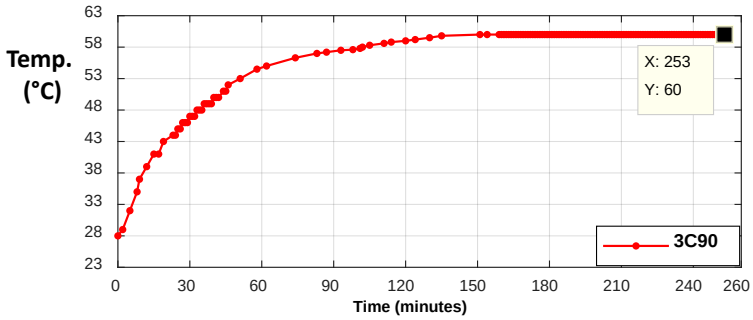


Figure 13. Experimental results. Hottest spot temperature profile for the encapsulated High Frequency Transformer (HFT) using 3C90 ferrite core measured using a Negative Temperature Coefficient (NTC) sensor.

A summary of the final HFT design is shown in Table 7.

Table 7. High Frequency Transformer (HFT) design summary.

Quantity	Value
Isolation	24 kV
Core structure	UU100/57/25
Ferrite material	Ferroxcube® 3C90
Encapsulation	Epoxy resin (15 kV/mm) (ROYAPOX 912 THC/2)
Bobbins	GPO-3 (20 kV/mm)
Number of turns (N)	35
Temperature rise at NTC 4	40 °C

5.2. Experimental Validation

Figure 14 shows the performed test connection diagram. A DC power supply is connected to the LVDC side to provide V_{dcLV} and the power is transferred from FB2 to FB1. The DAB current control regulates the transferred power using single phase shift (SPS) modulation while the CHB full bridge regulates the cell capacitor voltage (V_{cell}).

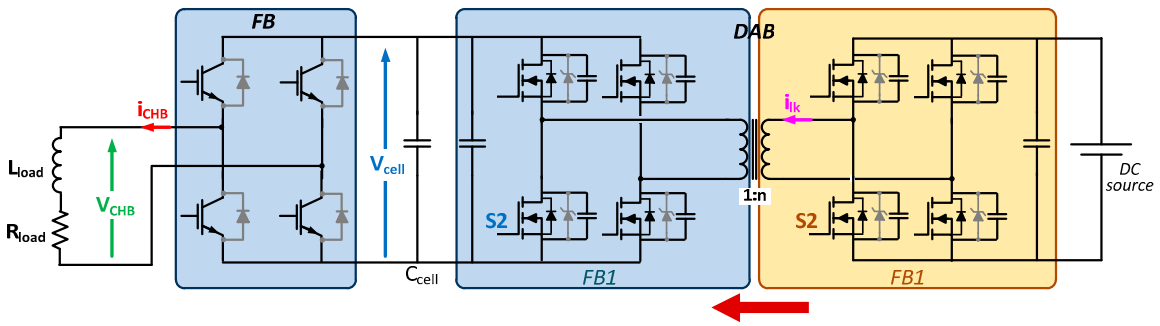
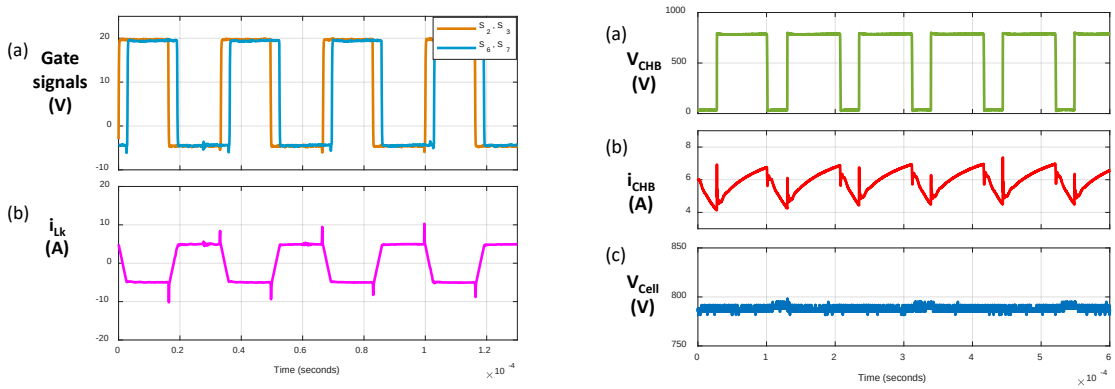


Figure 14. Schematic of the Power Electronic Transformer (PET) module during the performed experimental test.

Figure 15 shows the experimental results for the PET module nominal operation (described in Table 1). Figure 15a shows the DAB waveforms, where FB2 gates are leading FB1 gates and the phase shift between both controls the magnitude of the transferred power [35].



(**a**) (**b**)

Figure 15. Experimental results. (**a**) Dual Active Bridge (DAB) waveforms. Two gate signals of DAB FB1 and FB2 and leakage inductance current (i_{IK}). (**b**) Cascaded H-Bridge (CHB) full bridge waveforms. CHB full bridge output voltage (V_{CHB}), CHB full bridge output current (i_{CHB}), and the cell capacitor voltage (V_{cell}).

Figure 15b shows the CHB waveforms, where V_{CHB} and i_{CHB} are the CHB full-bridge output voltage and current respectively. V_{cell} is regulated at 800 V by the CHB voltage control.

6. Conclusions

This paper analyzes the use of SiC devices in three-stage modular PETs. It has been shown that SiC MOSFETs can be especially advantageous in the isolation stage, as they combine high blocking voltage and high switching frequencies, leading to higher efficiency, size reduction of the isolation transformer, and higher power density. On the other hand, limited merit is achieved using SiC in the front end AC/DC and the LV side DC/AC converters. However, this partially depends on the application of the PET and the selected topology.

The paper details the selection of SiC MOSFETs for the DAB DC/DC isolation stage experimentally comparing different commercial devices. The benefits of a SiC antiparallel SBD is investigated. It is concluded that the SiC diode improves the efficiency of the DAB as it reduces the total conduction losses of the device. However, this improvement strongly depends on two critical design aspects: the employed dead time interval and the time interval during which the current is driven by both the MOSFET and the diode at the same time (due to the voltage drop in the MOSFET on resistance directly biasing the diode). Generally, the efficiency improvement can be more relevant for a flatter inductor current shape and when the DAB is working around its nominal operation point. A loss model was presented to assess the introduced efficiency improvement and was experimentally validated.

Experimental results showing the operation of the full-scale DAB converter at rated conditions as part of the PET module are provided.

Author Contributions: Conceptualization, A.R., M.A. and F.B.; methodology, A.R., M.A. and F.B.; software, M.S.; validation, M.S. and M.R.R.; formal analysis, M.S. and M.R.R.; investigation, M.S. and M.R.R.; writing—review and editing, M.S., M.R.R., A.R., M.A. and F.B.; supervision, A.R., M.A. and F.B.; funding acquisition, A.R., M.A. and F.B. All authors have read and agreed to the published version of the manuscript.

Funding: This work was supported by the Spanish Government under projects MCIU-19-RTI2018-099682-A-I00, FC-GRUPIN-IDI/2018/000179, and PAPI-18-PF-10 and by the European Commission FP7 Large Project NMP3-LA-2013-604057, under grant UE-14-SPEED-604057.

Conflicts of Interest: The authors declare no conflict of interest.

Nomenclature

$\mathbf{V_{acHV}}$	HVAC grid voltage
$\mathbf{V_{acLV}}$	LVAC grid voltage
$\mathbf{V_{dcLV}}$	LVDC link voltage
$\mathbf{C_{dcLV}}$	LVDC link capacitor
$\mathbf{V_{cell}}$	Cell capacitor voltage
$\mathbf{C_{cell}}$	Cell capacitor
$\mathbf{f_{sw}}$	Switching frequency
T	Half the switching period of the DAB
d	Phase shift of the DAB represented as a ratio of T
$\mathbf{L_{lk}}$	DAB leakage inductance
$\mathbf{V_{knee}}$	Diode knee voltage
$\mathbf{V_{F\text{-}diode}}$	Diode forward voltage
$\mathbf{I_{pk\text{-}lk}}$	Peak current through the leakage inductance
$\mathbf{R_{ON\text{-}MOSFET}}$	MOSFET ON resistance
$\mathbf{C_{o(er)}}$	MOSFET effective output capacitance

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