

Design of a Cooperative Voltage Harmonic Compensation Strategy for Islanded Microgrids Combining Virtual Admittance and Repetitive Controller

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Abstract—Non-linear loads (NLLs) in three-phase systems are known to produce current harmonics at -5, 7, -11, 13... times the fundamental frequency; harmonics of the same frequencies are induced in microgrid voltage, reducing therefore the power quality. Dedicated equipment like active power filters can be used to compensate the microgrid harmonics; alternatively, each distributed generation (DG) unit present in the microgrid can be potentially used to compensate for those harmonics. The use of the virtual admittance concept combined with a PI-RES control structure has been recently proposed as a harmonic compensation sharing strategy when multiple DGs operate in parallel. The drawback of this methodology is that a large number of RES controllers might be required to compensate for all harmonic components induced by NLLs. This paper proposes the combined use of virtual admittance control loop and repetitive controller (RC) for harmonic compensation. The main advantage of the proposed method is that only one RC is required to compensate for all the harmonic components, significantly reducing the computational burden and the design complexity.

Keywords—central controller, harmonic compensation, nonlinear loads, repetitive controller, resonant controller, virtual admittance

I. INTRODUCTION

During the last decades, the power generation strategy has been shifted from a centralized to a distributed scenario [1]. In a centralized scenario the power is generated in large centralized power plants that transmit the electric power over long distances. Opposite to this, in the distributed generation (DG) scenario the generators typically have a smaller size and are connected to the utility grid near where the electric power is used. This reduces the transmission losses as well as the size and number of power lines needed [2]. DG scenarios can be islanded or grid connected [3]-[4]. Both scenarios can combine linear loads (LL) and non-linear loads (NLL). NLLs in three-phase systems are known to produce current harmonics typically at -5, 7, -11, 13...

times the fundamental frequency (i.e. 50/60 Hz). As a consequence, harmonic components of the same frequencies are induced at the point of common coupling (PCC) voltage [5]-[7], adversely impacting the power quality. To overcome these problems, dedicated equipment like active power filters (APFs) designed to compensate harmonic current components can be used [8]. However, these solution brings an increase of cost. An alternative to the use of APFs is to use the DG units as APF, to improve the microgrid's power quality. DGs are required to inject high frequency currents to the PCC to compensate for harmonic components due to e.g. NLLs. A relevant issue in this case is to determine how much harmonic current must be injected by each DG unit participating in the strategy. It is desired in this case that DG units closer to where the disturbance is produced inject a larger share of the harmonic current, as this will reduce the associated losses. Centralized and distributed control strategies have been already proposed to address this issue [9]-[10].

A simple solution to select the amount of harmonic current injected by each DG is to use an agent that statically assigns the harmonic current command for each DG [11]. However, this solution typically does not take into account the microgrid topology, meaning that this strategy might not minimize the transmission losses due to the harmonic current injection. An alternative solution is the use of the virtual admittance concept [10]. This method dynamically adapts the mode of operation of the inverter to the microgrid condition, such that inverters located nearer the PCC contribute in a greater degree to the compensation task. Very important, this is achieved without previous knowledge of the grid topology.

Nonetheless, the virtual admittance concept [10] requires the use of a PI-RES control structure to inject the inverter's current harmonics. A resonant controller (RES) is used for each pair of harmonic components to be compensated for (a positive sequence harmonic and a negative sequence), therefore a large number of RES controllers might be required to compensate for all harmonic components induced by NLLs, which might result in a significant increase of the computational burden and tuning difficulties.

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To overcome this limitation, this paper proposes a virtual admittance control loop based on a repetitive controller (RC). The advantage of using a RC is that it can compensate all harmonic components with reduced computational burden and design and tuning complexity.

The paper is organized as follows: Section II presents the basics of the proposed harmonic compensation strategy. The repetitive controller design is analyzed in Section III. Simulation and experimental results validating the proposed methodology are presented in Sections IV and V respectively. Finally, the conclusions are presented in Section VI.

II. COOPERATIVE VOLTAGE HARMONIC COMPENSATION STRATEGY FOR ISLANDED MICROGRIDS

Fig. 1 shows a simplified microgrid configuration that will be used for analysis purposes. It includes two voltage source inverters (VSI) connected in parallel, the microgrid always working in island mode. Both inverters are physically connected by a static switch (S), a transmission line (TL) being placed between each inverter and the PCC. Linear (LL) and nonlinear (NLL) loads are connected to the PCC. All the variables in the following block diagrams are referred to a reference synchronous with the harmonic h being controlled (inv : inverter-side or out : LCL output). The cooperative harmonic compensation strategies, including using a central controller and local controllers and the virtual admittance concept are described following.

A. Central Controller

The objective of a cooperative harmonic compensation strategy is to make use of all inverters connected to the PCC to inject harmonic currents consumed by NLLs. The central controller shown in Fig. 1 receives the information of the PCC voltage harmonic components, a communication channel (industrial bus, WiFi, ZigBee, mobile communications ...) being used for this purpose. The central controller implements

a PI regulator for each harmonic component to be compensated for, its reference $u_{out\ dqh}^{h*}$ being typically set to zero, as PCC voltage harmonic components are normally desired to be fully compensated. The output of each harmonic PI controller, i_{dqh}^{h*} , is then transmitted, the reference being common to all inverters.

B. Local Controller with virtual admittance

The harmonic current sharing being implemented uses the virtual admittance concept [10]. A virtual admittance is connected in parallel with the inverter output and the LCL filter input, Y_{v1}^h and Y_{v2}^h in Fig. 1. The virtual current that this virtual admittance consumes depends on the inverter output voltage and the virtual admittance value, meaning that, for the same harmonic voltage, the higher the value of the inverter virtual admittance is, the lower the current that the inverter injects to the PCC is.

The current injected by each inverter consist of a fundamental current and harmonic current components. A synchronous PI current regulator is typically used to control the fundamental current. Resonant controllers were proposed in [10] to control the harmonic currents. Use of repetitive current controller (RC) [12]-[14] for this purpose is proposed in the next section. Advantages of RCs include simultaneous control of multiple harmonic components and easiness of its design and tuning.

III. REPETITIVE CONTROLLER DESIGN

A. Repetitive Controller Background

The concept of repetitive control was originally developed in 1980 by Inoue et al. for a single input single output (SISO) plant in the continuous time domain to track a periodic repetitive signal with defined period, and was applied successfully to control a proton synchrotron magnet power supply in 1981 [24]. The concept was then further investigated by Hara et al. [12]. Based on the internal model principle proposed by Francis and Wonham in 1975, any periodic reference (disturbance) signal with known period can be tracked (rejected) by including their

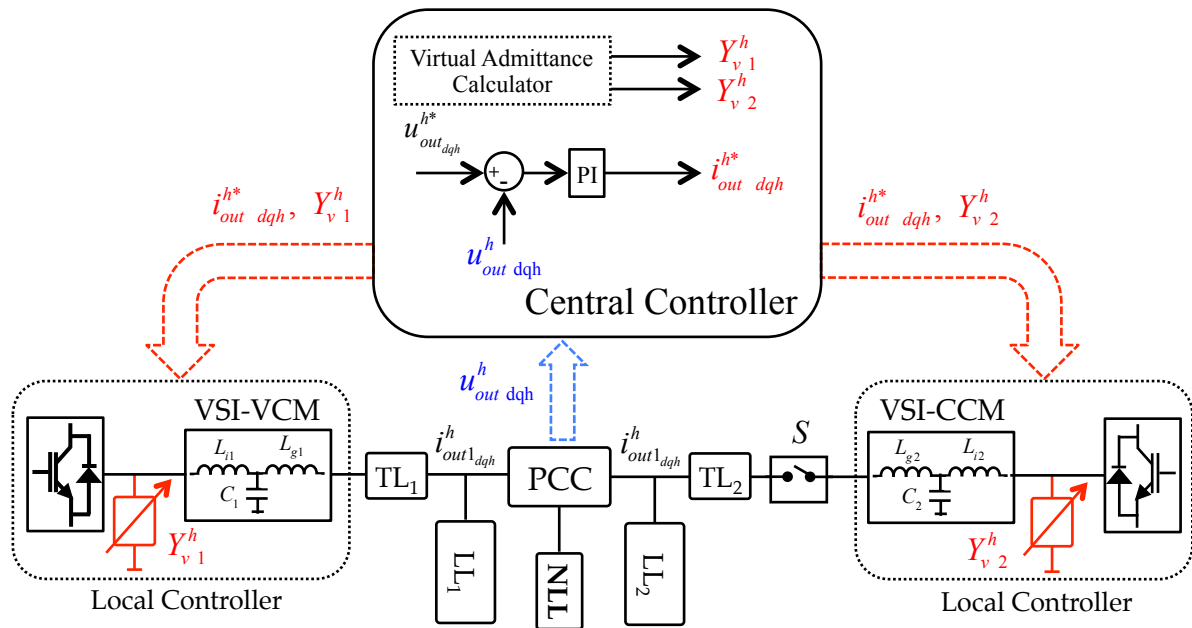


Fig. 1. Islanded scenario with two parallel-connected inverters. NLL stands for a non-linear load, the rest of loads in the figure being linear (LL). Subindex out stands for LCL output.

generator in the stable closed loop [25]. Therefore, RC is based on the idea of introducing the disturbance (signal) model in the system to track or reject it. Repetitive controllers have been widely used in applications including PWM inverters [26-29], PWM rectifiers [30], matrix converters [15], robotic manipulators [31], disk drive systems [32], four legs VSI [33]. The repetitive controller (RC), is a well know alternative to the use of a set of resonant controllers. The intrinsic characteristic of the RCs allows the automatic compensation of a defined set of multiple frequencies. The model can be introduced in both the continuous (Fig. 2) and discrete domain (Fig. 3), but the latter implementation, in digital system, has a more straightforward implementation by using (1). This results in a slow control action capable of cancelling the system steady state error to a periodic reference cycle by cycle (or rejecting periodic disturbances in the same way). RC can be used on its own only on an intrinsically stable system; for more general applications, it needs therefore to be used in conjunction with another controller (for example P or PI) which is designed with the aim of system stabilization and transient response performance.

$$G_{REP} = \frac{z^N}{1 - z^{-N}}; N = \frac{f_s}{f_{comp}} \quad (1)$$

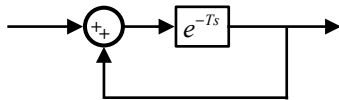


Fig. 2.- Continuous periodic model

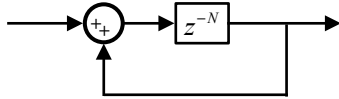


Fig. 3. - Discrete periodic model

The delay N is an integer value that, which together with the sampling frequency f_s , and f_{comp} being the first target frequency to be compensated. Three different schemes of combined plant compensator and RC controllers have been proposed in the literature [13]: parallel, series and the plug-in. The plug-in structure (Fig. 4) is used in this work as it shows several advantages including the possibility to design separately the RC and the plant compensator. The plant compensator G_C is firstly design to stabilize the plant and later the parameters of the RC are chosen to achieve the target signal tracking. To ensure the stability of the overall system, the basic scheme has to be modified to obtain the RC shown in Fig. 5.

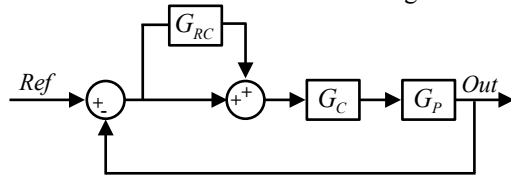


Fig. 4.- Plug-in repetitive Control loop.

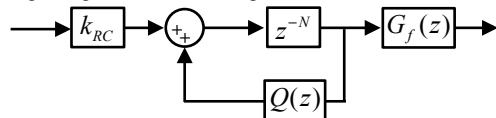


Fig. 5- Repetitive controller structure

The structure of the RC is characterized by a learning gain k_{RC} , a robustness filter $Q(z)$ and a stability filter $G_f(z)$. The robustness filter is designed to increase the stability margin of the system while the learning gain together with the stability filter is used to stabilize the entire loop. As summarized in [18], if the two following conditions are satisfied, the stability of the system is ensured:

1. All the poles of the close loop without the RC must be within the unity circle.
2. The absolute value of the function $S(z)$ (2) is less than the unity for all the frequency below the Nyquist frequency.

$$S(e^{j T_s}) = Q(e^{j T_s}) \frac{k_{RC} G_f(e^{j T_s}) G_c(e^{j T_s}) G_p(e^{j T_s})}{1 + G_c(e^{j T_s}) G_p(e^{j T_s})} \quad (2)$$

NYQ

The second condition is obtained applying the small gain theorem [16] to the error transfer function of the control loop shown in Fig. 3. Several choices exist to define the RC controller. First of all the robustness filter $Q(z)$ can be either a close-to-unity gain constant [18] or a moving average filter [21]. Both solutions enhance the stability margin of the model; the close-to-unity choice is the simplest solution in terms of implementation, but it compensates all the poles in the same manner. This means poorer tracking/rejection at lower frequencies. The second solution considers the use of a low pass filter that moves the high frequency poles inside the unity circle, resulting in poorer performances only for the high frequency poles. This solution is an acceptable trade-off between reasonable stability margins and accurate tracking/rejection at lower frequencies. For what concerns the stability filter $G_f(z)$ two different solutions can be adopted, as discussed in [15]. The first solution is a zero-phase-error-tracking-compensator [20]; however, the design is quite complicated and an accurate plant model is required. An alternative solution is the time-advanced-compensator that has the effect of balancing the phase shift introduced by the RC. The time-advanced compensator assumes the expression (3), where T_A is the time advanced step. The k_{RC} gain is adjusted to achieve the condition of the small gain theorem. In general the range of feasible values for the repetitive controller is $0 < k_{RC} < 2$.

$$G_f(z) = z^{T_A} \quad (3)$$

B. Repetitive Controller Design

The proposed control is based on the plug-in configuration of the repetitive controller. The number of necessary finite delays N is selected according with (1). The low pass filter has been selected as a moving average filter whose transfer function is (4).

$$Q(z) = \frac{0.0625z^4 + 0.25z^3 + 0.375z^2 + 0.025z + 0.0625}{z^2} \quad (4)$$

The stability filter $G_f(z)$ has been selected as a time-advanced compensator (3). The proposed design uses a sampling frequency of 9.9 kHz and number of finite delays N equal to 33 (1). The learning gain k_{RC} has been adapted for the different network topologies; for doing so an initial learning gain $k_{RC\text{ init}}$ has been defined to stabilize the system when the VSI-CCM inverter is not connected to the PCC (Fig. 1). The design parameters are summarized in Table I.

Table I – Setup Parameters		
	VSI-VCM Inverter	VSI-CCM Inverter
Rated power	50kW	50kW
Rated voltage	380V	380V
Capacitor ESR	0.052 Ω	0.052 Ω
Inductor ESR	0.05 Ω	0.05 Ω
Inverter-side inductor	2.4 mH	2.196 mH
Capacitor filter	10 μF	10 μF
Grid-side inductor	1.6 mF	2.19 mF

Centralized controller			
Kp_{-5}	0.07	Ki_{-5}	0.9
Kp_7	0.3	Ki_7	0.9
Local PI-RES			
Kp	8	Ki	3000
Kp_{RES}	1	C	300
N	6	f_s	9.9 kHz
Local PI-RC VSI-VCM Inverter			
$k_{RC\text{ init}}$	0.5	N	33
k_{RC}	1	f_s	9.9 kHz
TA	2	f_{comp}	300Hz
Local PI-RC VSI-CCM Inverter			
$k_{RC\text{ init}}$	0.1	N	33
k_{RC}	1.2	f_s	9.9 kHz
TA	2	f_{comp}	300Hz

IV. SIMULATION RESULTS

Fig. 1 and Table I show the simulation scenario and the simulation parameters respectively. Fig. 6 shows the local controller block diagram that is implemented in each inverter (VSI-VCM and VSI-CCM, see Fig. 1); it includes the virtual

admittance control loop (shown in red color, see Fig. 6; more details can be found in [10]) and the plug-in RC.

Fig. 7 shows the simulation results using both the proposed control strategy with a RC, and with RES controllers [10]. The implementation using RES controllers is configured to compensate only for -5^{th} and 7^{th} harmonic components [10].

The THD before harmonic compensation is enabled is 8.7 %, the cooperative harmonic compensation starting at $t=0.6$ s. It is observed from Fig. 7b that the voltage THD reduces to 0.07% using the proposed PI-RC implementation, and 3.12% when using the PI-RES implementation. This is due to the fact that the PI-RES implementation only compensates for the -5^{th} and 7^{th} PCC voltage harmonic while the RC compensates all higher order harmonics (-5^{th} , 7^{th} , -11^{th} , 13^{th} ...).

Fig. 7b-7e show the magnitude of the current harmonic injected by each inverter for the PI-RC and PI-RES implementations. Independent of the method being used, the higher the virtual admittance is, the lower is the current being injected: while $t < 2$ s, the virtual admittance of both inverters is set to zero, both VSI-VCM and VSI-CCM injecting the same amount of current for all of the controlled harmonics, see Fig. 7b-7e). At $t=2$ s, the VSI-VCM virtual admittance is set to $0.05 \Omega^{-1}$ while the VSI-CCM virtual admittance is set to $0.01 \Omega^{-1}$, the VSI-VCM injects therefore less harmonic current than the VSI-CCM (see Fig. 7b-7e). At $t=3$ s the virtual admittances of both inverters are swapped; the VSI-CCM injecting therefore less current than the VSI-VCM. For $t > 4$ s, the virtual admittance of VSI-VCM is set to infinite (see Fig. 7a), therefore it stops injecting harmonic current (see Fig. 7b-7e), i.e. all the harmonic current is consumed by the virtual admittance. It is finally noted that the -11^{th} and 13^{th} harmonic currents are not controlled when using the PI-RES implementation, see Fig. 7d and 7e, no RES controller being implemented to compensate for those harmonic components.

Finally, Fig. 8a and 8b shows the PCC voltages before and after the compensation respectively.

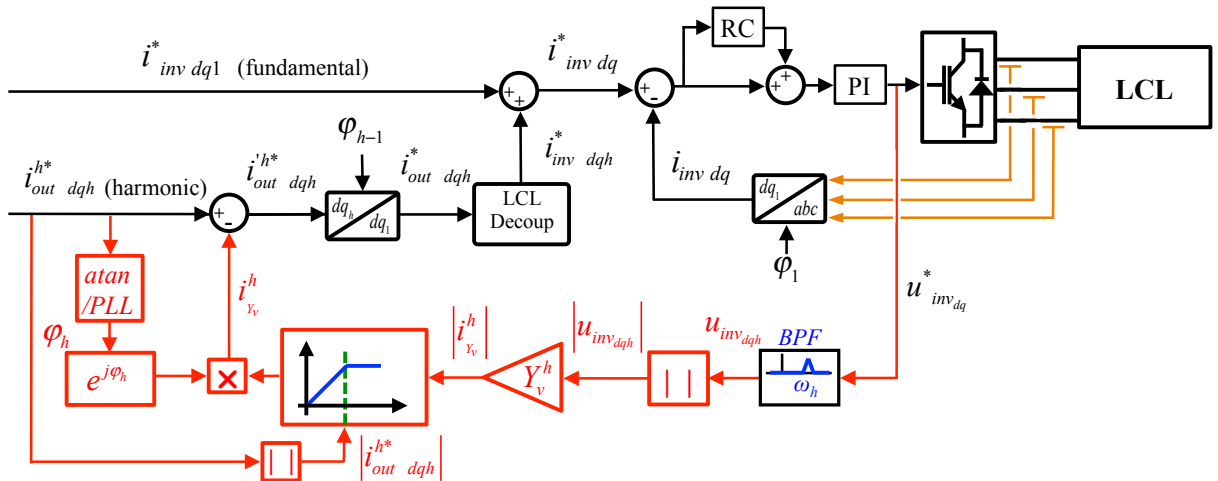


Fig. 6. Local controller block diagram including the virtual admittance and the RC.

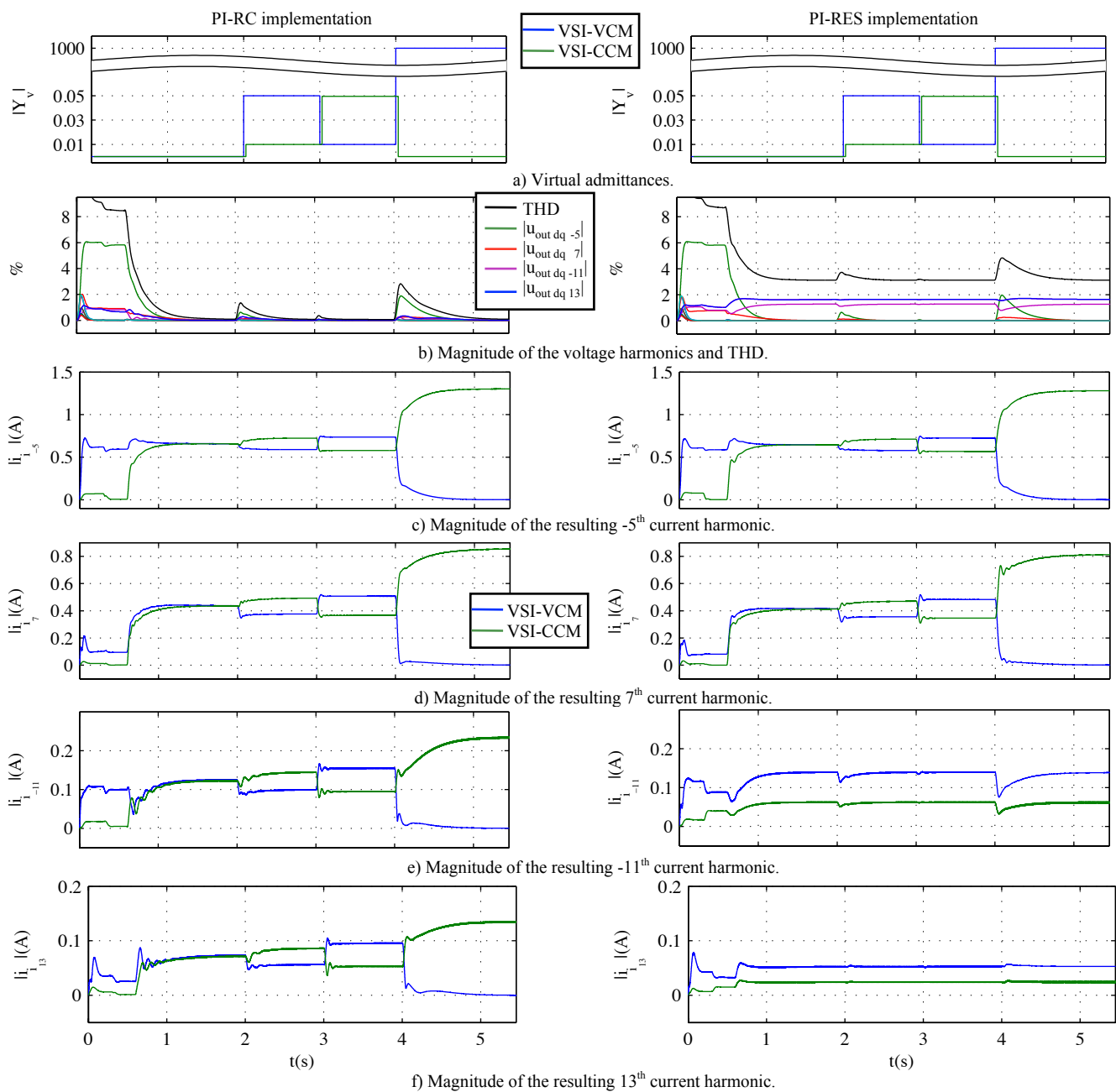


Fig. 7.- Simulation results. Coordinated voltage harmonic compensation for different values of the virtual admittance. PI-RC & PI-RES comparative.

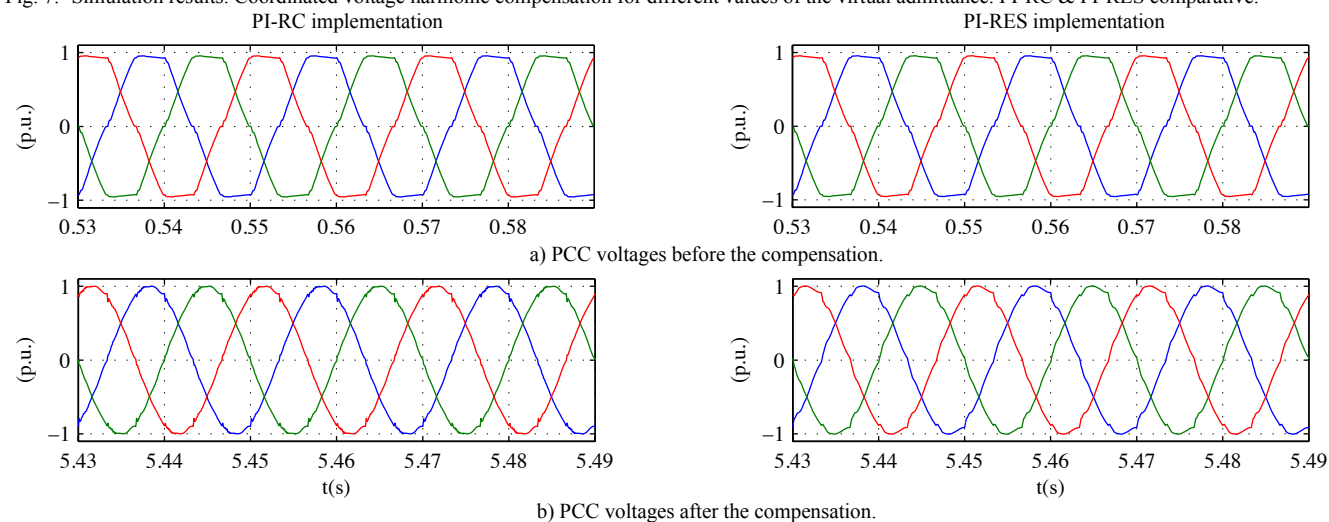


Fig. 8.- Simulation results showing the PCC voltages in *abc* quantities before and after the compensation strategy is enabled.

V. EXPERIMENTAL RESULTS

This section shows the experimental verification of the control strategy proposed in this paper. The experimental setup is the same as in simulation, see Fig. 1. Parameters of the experimental setup are shown in Table II. For the experimental results, a *WiFi* link has been used to transfer measurements, current references and virtual admittances among the inverters and the central controller. The central controller is implemented in a computer. It receives the PCC voltages and sends the current references required to compensate the voltage harmonic content at the PCC. Simultaneously, the central controller sends the virtual admittances to the VSI-VCM and VSI-CCM which determines the current sharing strategy. The sampling frequency of the central controller is 5 Hz.

Table II – Experimental Setup Parameters

	VSI-VCM Inverter	VSI-CCM Inverter
Rated power	50kW	50kW
Rated voltage	380V	380V
Capacitor ESR	0.052 Ω	0.052 Ω
Inductor ESR	0.05 Ω	0.05 Ω
Inverter-side inductor	2.196 mH	2.4 mH
Capacitor filter	10 μ F	10 μ F
Grid-side inductor	0.5 mF	2.196 mF

Fig. 9 shows experimental results of the proposed strategy, using a PI-RC controller (Fig. 6) and the control strategy proposed in [10] using a PI-RES. Fig. 9a shows the virtual admittances that will be used, they are the same. Compensation is enabled at $t=6$ s. Both inverters are connected to the PCC while the microgrid is disconnected from the main grid. The same harmonics as in simulation (see Fig. 7), are to be compensated.

Fig. 9b shows the THDs for the PI-RC and PI-RES strategies. Harmonics not being controlled were removed from the figures for the sake of legibility. For the proposed PI-RC strategy, the THD reduces from 10.6% to 1% while for the PI-RES strategy, it reduces to 3%. These results are in good agreement with the simulation results and confirm the improved performance of PI-RC control strategies.

Figs 9c-9f show the -5^{th} , 7^{th} , -11^{th} and 13^{th} harmonic currents injected by the VSI-VCM and VSI-CCM respectively. When the PI-RC strategy is used (see Fig. 9c-9f) all of the PCC voltage harmonics controlled by the central controller are compensated. Conversely, when the PI-RES strategy is implemented, only the -5^{th} and 7^{th} harmonics are compensated, the -11^{th} and 13^{th} PCC voltage harmonics remaining unchanged. This is due to the fact that each RES only controls two harmonic components (-5^{th} and 7^{th} in this work).

For $0 < t < 12$ s, the virtual admittances of the VSI-VCM and VSI-CCM inverters are set to zero (Fig. 9a). Thus, for the case of the PI-RC strategy, both inverters inject the same amount of current (-5^{th} , 7^{th} , -11^{th} , 13^{th} harmonics), see Fig. 9c-f. This also occurs for the -5^{th} and 7^{th} harmonics in the PI-RES strategy (Fig. 9c and 9d), but not for the -11^{th} and 13^{th} components that remain unchanged (Fig. 9e, 9f).

At $t=12$ s, the VSI-VCM virtual admittance value is set to $0.05 \Omega^{-1}$ while the VSI-CCM virtual admittance value is set to $0.01 \Omega^{-1}$ (Fig. 9a). These values are swapped at $t=18$ s. Finally, at $t=24$ s the VSI-VCM virtual admittance value is set to 1000, the VSI-CCM virtual admittance being set to 0.

For the period between 12s and 24s, the inverter with the lowest virtual admittance injects more harmonic current. This is valid for all of the harmonics controlled in the proposed PI-RC scenario (-5^{th} Fig. 9c, 7^{th} Fig. 9d, -11^{th} Fig. 9e, and 13^{th} Fig. 9f), and for the -5^{th} and 7^{th} harmonics in the PI-RES scenario (Figs. 9c, 9d), -11^{th} and 13^{th} harmonics not being controlled in the PI-RES scenario (Fig. 9e and 9f).

Note that using the same virtual admittance does not guarantee that different inverters inject the same amount of current. E.g. for $12 \text{ s} < t < 18 \text{ s}$, the VSI-CCM inverter injects 0.38 A of -5^{th} harmonic (Fig. 9c) when a virtual admittance of $0.01 \Omega^{-1}$ is set (Fig. 9a). If the same virtual admittance is used for the VSI-VCM inverter, $18 \text{ s} < t < 24 \text{ s}$, VSI-VCM inverter injects 0.48 A of -5^{th} harmonic. This is due to the fact that the virtual admittance magnitude is multiplied by the LCL input voltage (u_{inv_dq} in Fig. 6). In this case, VSI-VCM inverter output LCL filter inductances (see Table II) are smaller, meaning that it requires less voltage to provide the same amount of current, more details on this issue can be found in [10].

Finally, for $24 \text{ s} < t < 30 \text{ s}$ the harmonic injection of the VSI-VCM is discontinued by setting the virtual admittance to a very large value ($1000 \Omega^{-1}$, see Fig. 9a). In this case, the VSI-CCM is required to inject all necessary current to compensate the harmonics being controlled, see Fig. 9c-f.

Fig. 10a shows the PCC voltages when the harmonic compensation strategy is disabled, while Figs. 10b shows the PCC voltages when both strategies, PI-RC and PI-RES, are used.

It is finally noted that the experimental results shown in Figs. 9-10 are in good agreement with the simulations shown in Fig. 7-8, the differences coming from the accuracy of the current sensors, non-linear behavior of the inverters and the communications bandwidth (communications have been modeled as a deterministic delay in simulation). Adding more harmonics to be compensated will be straightforward in the case of the PI-RC implementation since there is no need to modify the local controller. In this case, the central controller must receive the PCC harmonics to compensate and it will send current references. This issue has not tested experimentally due to of the limited *WiFi* bandwidth.

VI. CONCLUSIONS

In this paper, a cooperative voltage harmonic compensation strategy based on a centralized controller, the virtual admittance concept and a PI-RC controller has been presented. The advantage of the proposed implementation is that a single RC can compensate for all harmonic components typically produced by NLLs, which decreases the design complexity compared with previous implementations based on PI-RES structures.

The design and implementation of the central controller, the virtual admittance and the RC has been developed. Simulation and experimental tests have been provided to demonstrate the

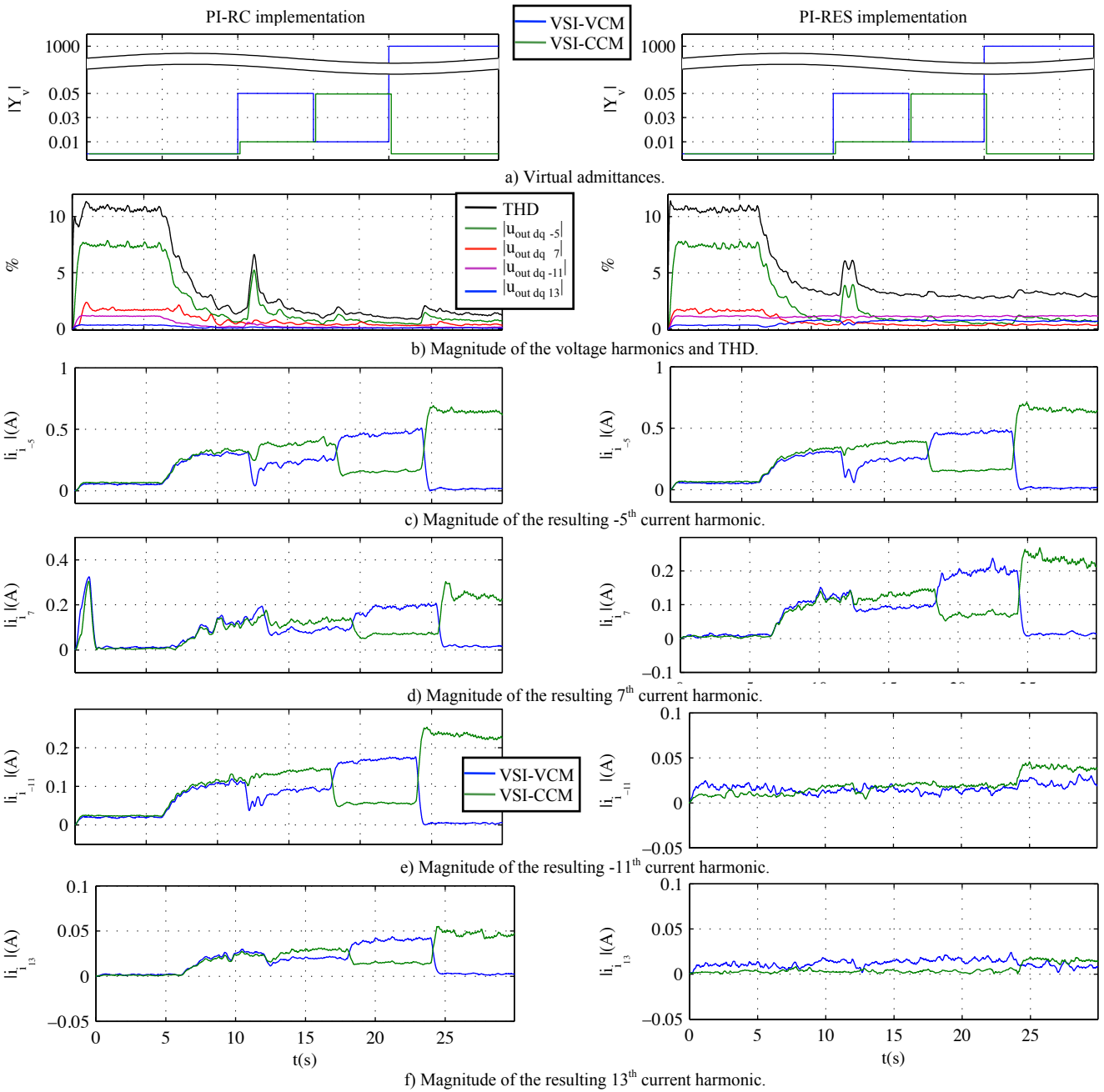


Fig. 9.- Experimental results. Coordinated voltage harmonic compensation for different values of the virtual admittance. PI-RC & PI-RES comparative

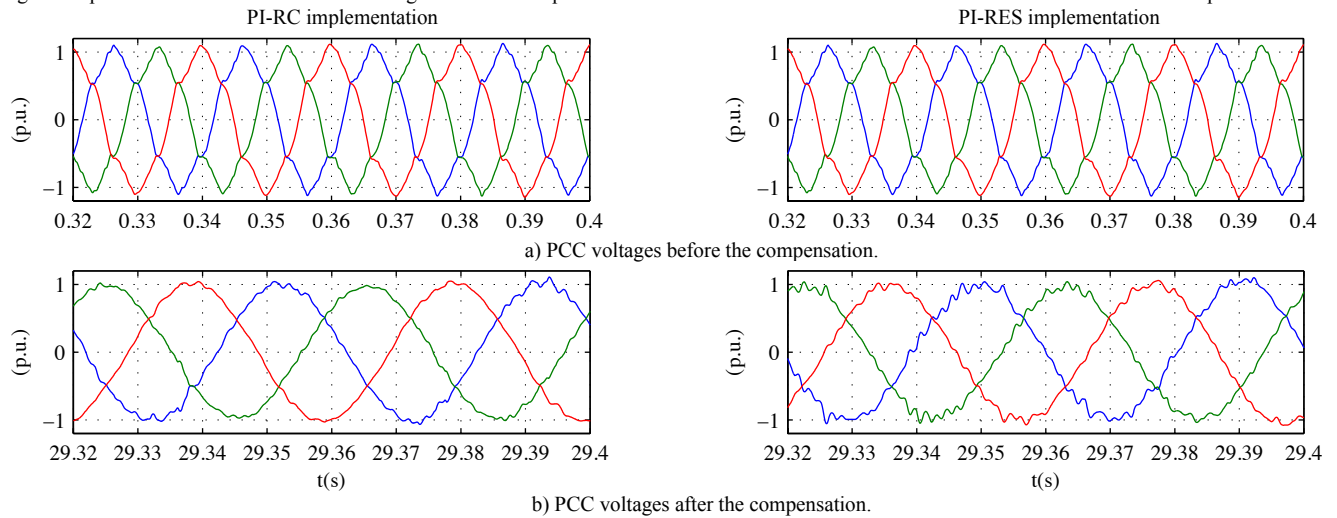


Fig. 10.- Experimental results showing the PCC voltages in abc quantities before and after the compensation strategy is enabled.

viability of the proposed method. From the obtained results, it has been proved that by just changing the controller from a resonant to a repetitive controller, the PCC voltage THD can be reduced from $\approx 3\%$ to $\approx 1\%$.

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