Efficiency evaluation of a SiC-based bidirectional boost converter using TCM-ZVS with different voltage conversion ratios

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***Abstract* -- This paper focuses on the design of a high-voltage (800V) bidirectional boost converter with high efficiency at medium-low power levels. Triangular Current Mode (TCM) enhances the efficiency of the converter at low power thanks to soft-switching operation, but it requires a variable switching frequency and a large current ripple through the inductor. The former can be implemented using SiC MOSFETs, while the latter can be minimized using interleaved modules.**

At low power, TCM requires a high switching frequency and specific pair of values of negative inductor current and dead-time to obtain ZVS. These values vary for different input/output voltage ratios and must be suitably selected to reduce dead-time losses, an issue normally neglected in the literature as it is assumed that they have low impact. However, it can be important at high frequencies (especially for devices with high reverse conduction voltage drop, such as SiC MOSFETs). In this paper, dead-time losses are included in the proposed power loss models. Furthermore, the selection of the optimum values of dead-time and minimum inductor current to minimize these dead-time losses are analytically evaluated and experimentally validated.

***Index Terms*--Boost, efficiency, modularity, QSW, SiC, TCM.**

I. INTRODUCTION

Some examples of established topics in current issues related to power electronics are: energy recovery systems, energy storage systems, renewable energies, dc distribution grids, smart grids and power electronic transformers [1]-[6]. Most of these applications require energy storage systems and bidirectional dc–dc power converters. Besides, the battery charging process is usually carried out in three stages [7], with a final stage in which the charging current is very low. Therefore, the aforementioned power converters interconnecting the storage system must achieve high efficiency over a wide power range.

An interesting topic related to these applications is the integration of distributed energy resources in multilevel converters. By means of the adequate design of the cells of multilevel converters (with a cell voltage usually around 1 kV), it is possible to integrate low voltage DC or AC power sources (such as photovoltaic (PV) panels or wind turbines), loads or energy storage devices at the cell level [8]-[10].

Hence, a power converter designed to integrate battery systems in a multilevel converter at the cell level must withstand high voltage while at the same time providing high efficiency. The use of Wide Band Gap (WBG) semiconductors, especially Silicon Carbide (SiC) MOSFETs, allows power converters to operate at high voltage and high switching frequency with high efficiency [11]. SiC MOSFETs and a variable switching frequency control technique providing Zero Voltage Switching (ZVS) have been used to improve efficiency in a synchronous boost converter, especially at medium and low load operating at high voltage and high frequency [12], [13].

When the converter is working at low load, triangular conduction mode (TCM) requires, on the one hand, a high switching frequency and, on the other, a minimum negative inductor current and a minimum dead-time to achieve ZVS. Given that switching losses are predominant at low load (which corresponds to higher switching frequencies), these extra losses need to be considered in an appropriate loss power model to predict their impact if TCM is used. In this paper, dead-time losses are included in the proposed power loss models and the selection of the optimal values of dead-time and minimum inductor current to minimize these dead-time losses are analytically evaluated and experimentally validated.

It should be noted that the specifications of the bidirectional boost converter analysed in this paper are oriented towards providing battery systems to a multilevel converter at the cell level (Fig. 1). However, the conclusions can be applied to different applications in which a non-isolated bidirectional converter with high efficiency for light loads and high-voltage operation is needed (e.g. wind energy generation with storage capability [10] or electric vehicle battery chargers [14], [15]).

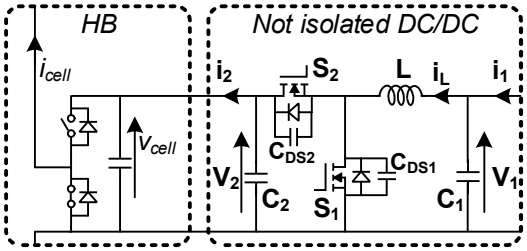

Fig. 1 Cell structure composed of a non-isolated bidirectional boost converter and a Half-Bridge (HB).

The advantages and drawbacks of different conduction modes and a preliminary power loss model will be reviewed and discussed in Section II. Furthermore, more analytical insight into the resonant period, which is commonly neglected in the literature, and the trade-off between negative current and dead-time when the converter works under different input/output voltage ratios are presented in Section III, constituting the main contribution of this paper. Section IV shows the experimental results and efficiencies for different conditions. Finally, conclusions are drawn in Section V.

II. CONTROL STRATEGIES TO OBTAIN HIGH, FLAT EFFICIENCY OVER A WIDE POWER RANGE

In order to achieve and maintain high efficiency over a wide power range, different strategies may be followed, such as modifying the conduction mode for different load levels. To be able to select the appropriate operating mode of the bidirectional boost converter, a comprehensive power loss model considering any possible source of losses is needed.

A. Conduction Modes

The main characteristics of the two continuous conduction modes (CCM) providing the best performance from the efficiency point of view are presented below (their main waveforms are shown in Fig. 2):

1) CCM Hard Switching (CCM-HS). Reduced current ripple and constant switching frequency (f). The key advantage of this conduction mode is low current ripple (suitable for charging and discharging energy storage systems), achieving low conduction losses. High-switching losses constitute the main drawback, however. At light loads, this mode can achieve ZVS (i.e. TCM at constant switching frequency).

2) TCM with minimum negative current to obtain ZVS (TCM-ZVS). Large current ripple (the inductance current is negative at the turn-on of S_1) and variable switching frequency comprise its main characteristics. Full ZVS can be achieved by the suitable selection of the negative inductance current and dead-time for different input and output voltages relationships [16], thereby reducing switching power losses. This conduction mode is also known as pure QSW-ZVS [16] - [19] when the output voltage is twice the input voltage (ZVS is obtained more easily).

B. Power loss models

The use of the aforementioned conduction modes depending on the load demand and the distribution of losses related to them are characterized in detail in [20] and [21], respectively. An efficiency comparison between the analysed conduction modes is thus possible for a wide power range (Fig. 3). To obtain these power loss models, the specifications of the prototype (defined, in this paper, in Section IV) need to be taken into account.

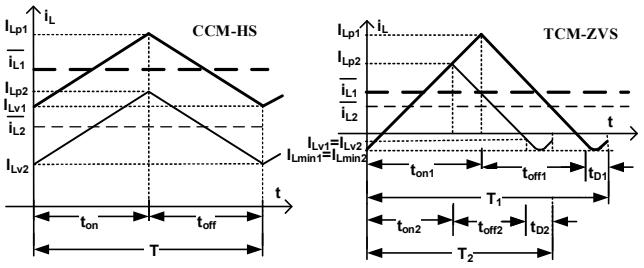

Fig. 2 Current through the inductor, $i_L(t)$, for CCM-HS and TCM-ZVS, showing the peak value ($I_{Lp\,x}$), average value ($\overline{i_{L\,x}}$), valley value ($I_{Lv\,x}$) and minimum value ($I_{Lmin\,x}$) for two power demands (1 or 2). t_{onx} represents the time S_1 is ON and S_2 is OFF, t_{offx} represents S_1 OFF and S_2 ON and t_{Dx} represents a certain dead-time.

The sources of losses taken into consideration in this paper are conduction, gate, switching and inductor losses, placing special emphasis on the differences among switching losses during turn-ons turn-offs depending on the conduction mode.

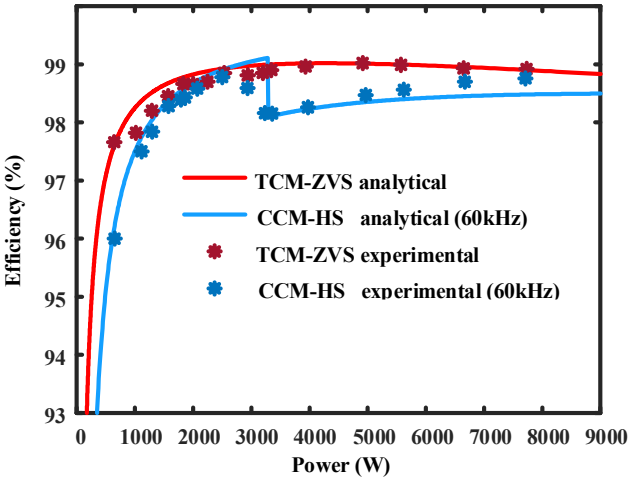

Fig. 3 Experimental and analytical efficiency comparison for different conduction modes [21].

In CCM-HS, the converter works at a fixed frequency of 60kHz and the current through the inductor is always positive for load levels higher than 3000W. A dip in efficiency at 3000W takes place because, as the current ripple is fixed, the converter enters into TCM for load demands lower than 3000W (i_{Lv} is negative and ZVS is achieved). As the load demand decreases, the current through the inductor takes a more negative value, causing losses due to reactive current in the converter, which results in a faster decrease in efficiency.

Taking into account the current ripple level through the inductors and as the efficiencies between modes are close, it is proposed to use CCM-HS for power levels higher than 3000W and TCM-ZVS for lower power levels.

It should be noted that both the analytical and experimental results are obtained under the condition $V_2=2\cdot V_1$, where V_1 is 400V and V_2 is 800V, and therefore pure QSW-ZVS is achieved.

For different input/output voltage ratios, however, QSW-ZVS becomes TCM-ZVS with variable switching frequency

and some changes in the power loss model need to be included in order to take into account the minimum negative inductor current and the minimum dead-time needed to achieve ZVS, as will be further explained in Section III.

III. DEAD-TIME VS. NEGATIVE CURRENT

As stated in Section II, the efficiencies obtained in Fig. 3 are only valid if the condition $V_1=V_2/2$ is met and pure QSW-ZVS is achieved.

When the bidirectional boost converter under analysis is used to integrate batteries at the cell level in a multilevel converter, the voltage conversion ratio varies due to the voltage fluctuation of the batteries. If V_2 is not twice V_1, the efficiencies presented in Fig. 3 are not valid, because the inductance current could be different to ensure ZVS. In the case presented here, there are certain variables that must be properly selected, such as the valley inductance current when S_2 is turned off (i_{Lv} in Fig. 4) and the appropriate dead-time (t_D in Fig. 4). The dead-time is defined as the time from the negative edge of V_{GS2} (green waveform) to the positive edge of V_{GS1} (purple waveform). During this dead-time, the output parasitic capacitance of S_1 is discharged, a requirement to achieve ZVS and the best attainable efficiency.

A. Resonant interval in TCM-ZVS

QSW-ZVS can be seen as a particular case of TCM-ZVS where i_{Lv} is equal to 0 (due to $V_2 = 2 \cdot V_1$). To fully understand the differences between these two conduction modes and the advantage of TCM under different V_1/V_2 ratios, it is important to analyse the resonant interval, generally neglected in the literature as it is assumed that it has low impact in comparison to linear intervals.

The voltage in the switching MOSFET ($V_c(t)$) and the current through the inductor ($i_L(t)$) during the resonant interval can be obtained using (1)-(3) for boost behaviour and (2)-(4) for buck behaviour (see Table I).

In this paper, boost behaviour is considered when the power flows from V_1 to V_2. In contrast, buck behaviour is considered when the power flows from V_2 to V_1. In line with the specifications of the prototype presented in Section V, $V_c(t)$ and $i_L(t)$ are shown in Fig. 5 for different voltage ratios by plotting Equations (1) and (3) for diverse values of $|i_{Lv}|$.

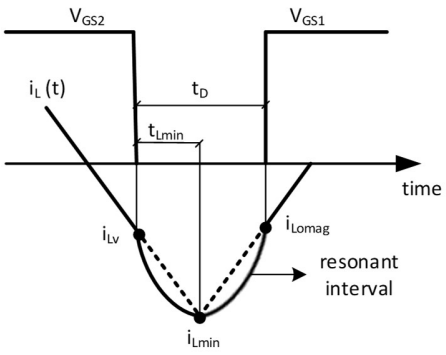

Fig. 4 Detail of $i_L(t)$ during the resonant interval.

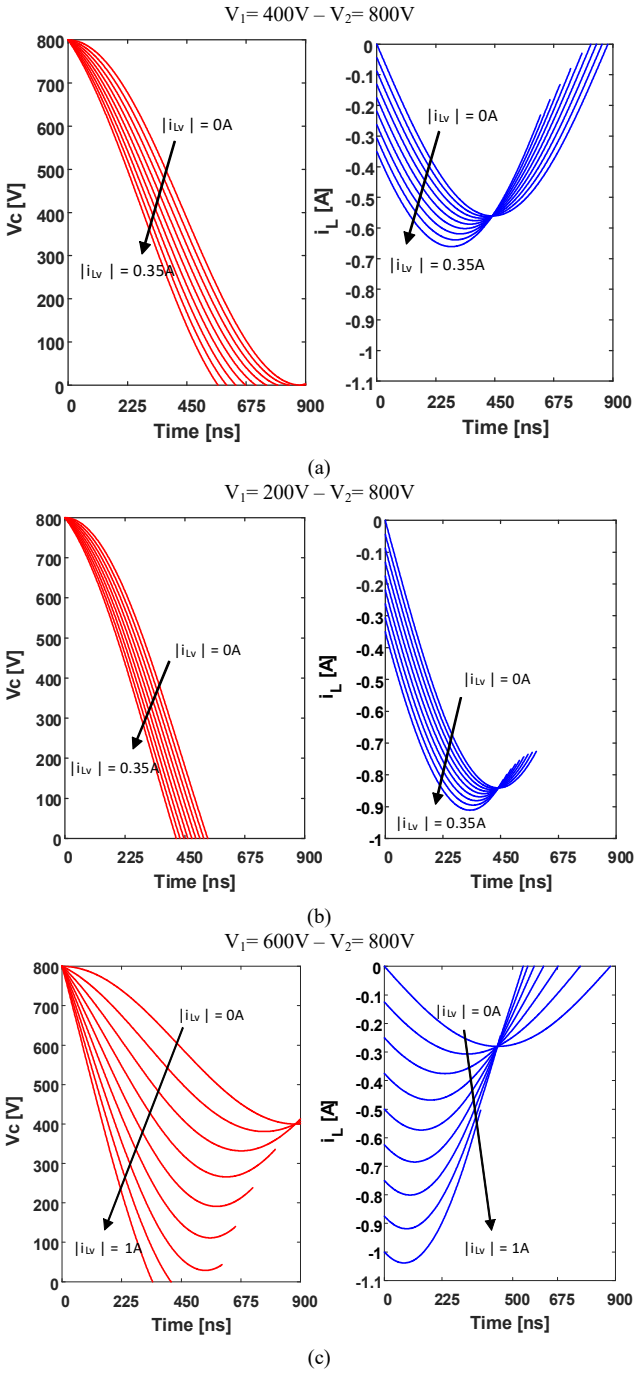

Fig. 5 Vc(t) in red and iL(t) in blue for different V1/V2 voltage ratios. (a) 400V/800V (b) 200V/800V and (c) 600V/800V when the power is flowing, defining boost behaviour.

A voltage ratio $V_1=V_2/2$ is applied in Fig. 5 (a). This working condition corresponds to the well-known case of pure QSW-ZVS. In this case, ZVS can be achieved for any i_{LV} value below or equal to 0A provided there is a specific minimum t_D. It can be seen that the lower the value of i_{LV} (the inductance current at the beginning of the resonant interval), the shorter the t_D needed to achieve $V_c(t)$ equal to 0V.

TABLE I EQUATIONS DURING THE RESONANT INTERVAL FOR BOOST AND BUCK BEHAVIOUR.

BOOST		BUCK	
$V_C(t) = (V_2 - V_1) \cdot cos(w_0 t) + \left({}^{i_{Lv}}/_{C_{sw} \cdot w_0}\right) \cdot sin(w_0 t) + V_1$	(1)	$V_C(t) = V_2 \cdot \cos(w_0 t) + \left({}^{i_{Lv}}/_{C_{sw} \cdot w_0}\right) \cdot \sin(w_0 t) + V_1 - V_2$	(2)
$i_L(t) = i_{Lv} \cdot \cos(w_0 t) - C_{sw} \cdot w_0 \cdot (V_2 - V_1) \cdot \sin(w_0 t)$	(3)	$i_L(t) = i_{Lv} \cdot \cos(w_0 t) + C_{sw} \cdot w_0 \cdot V_2 \cdot \sin(w_0 t)$	(4)
$i_{Lv} = C_{sw} \cdot w_0 \cdot \sqrt{2 \cdot V_2 \cdot V_1 - V_2^2}$	(5)	$i_{Lv} = C_{sw} \cdot w_0 \cdot \sqrt{V_1^2 - 2 \cdot V_2 \cdot V_1}$	(6)
$t_D = {}^1/_{w_0} \cdot \left[\sin^{-1}\left(-\frac{V_1}{\sqrt{(V_2 - V_1)^2 + \left({}^{i_{Lv}}/_{C_{sw} \cdot w_0}\right)^2}} \right) - \tan^{-1}\left(\frac{C_{sw} \cdot w_0}{i_{Lv}} \cdot (V_2 - V_1) \right) \right]$	(7)	$t_D = {}^1/_{w_0} \cdot \left[\sin^{-1}\left(-\frac{(V_2 - V_1)}{\sqrt{{V_2}^2 + \left({}^{i_{Lv}}/_{C_{sw} \cdot w_0}\right)^2}} \right) - \tan^{-1}\left(\frac{C_{sw} \cdot w_0}{i_{Lv}} \cdot V_2 \right) \right]$	(8)
$i_{Lmin} = i_{Lv} \cdot \cos(w_0 t_{iLmin}) - C_{sw} \cdot w_0 \cdot (V_2 - V_1) \cdot \sin(w_0 t_{iLmin}) + V_1$	(9)	$i_{Lmin} = i_{Lv} \cdot \cos(w_0 t_{iLmin}) + C_{sw} \cdot w_0 \cdot V_2 \cdot \sin(w_0 t_{iLmin}) + V_1 - V_o$	(10)
$t_{iLmin} = {}^1/_{w_0} \cdot \cos^{-1}\left(\sqrt{\frac{1}{1 + \left(\left(\frac{C_{sw} \cdot w_0}{i_{Lv}} \right) \cdot (V_2 - V_1) \right)^2}} \right)$	(11)	$t_{iLmin} = {}^1/_{w_0} \cdot \cos^{-1}\left(\sqrt{\frac{1}{1 + \left(\left(\frac{C_{sw} \cdot w_0}{i_{Lv}} \right) \cdot V_2 \right)^2}} \right)$	(12)

Similarly, a voltage ratio $V_1<V_2/2$ is employed in Fig. 5 (b). Under these voltage conditions, ZVS is achieved using boost behaviour for any negative value of i_{LV} provided a certain t_D. The t_D value is lower in this case than in the boundary case (where $V_1=V_2/2$).

In the case of Fig. 5 (c), the voltage ratio used corresponds to $V_1>V_2/2$. In this situation, not all the values for the i_{LV}-t_D pair are valid for boost behaviour, according to (5) and (7). A minimum i_{LV} below 0A must be ensured to fully discharge the output capacitance of the device and achieve ZVS.

It should be mentioned that the curves obtained in Fig. 5 , following (1) and (3) and complying with (5) and (7) for boost behaviour, are analogous to but the inverse of those following (2), (4), (6) and (8) for buck behaviour. Therefore, in the case of buck behaviour, the most suitable working situation corresponds to $V_1>V_2/2$, while in the case of $V_1<V_2/2$, only some pairs of i_{LV}-t_D values (with i_{LV} sufficiently low) are suitable to achieve ZVS.

B. Optimal pair of values i_{LV}-t_D

As already stated, depending on the operation point with respect to the input/output voltage ratios, certain values for i_{LV} and t_D need to be calculated.

Furthermore, following the currents through the inductor expressions, $i_L(t)$, (3) and (4), it is possible to calculate the minimum value of the current during this resonant period. i_{Lmin}, (9)-(10) and the time needed to reach it, t_{iLmin}, (11)-(12), These calculations are especially useful to obtain practical approximations of the current values needed to calculate the extra power losses during the negative part of $I_L(t)$ defined in (13).

In the modified power loss model, the extra dead-time losses due to the negative current passing through the antiparallel diode of the MOSFET are considered by means of its characteristic I-V curve [25].

$$P_{dT} = V_d \cdot \bar{I}_{L\_tD} + {I_{L\,rms\_tD}}^2 \cdot R_d \quad (13)$$

where V_d and R_d are the knee voltage and conduction resistance of the diode, respectively, and $\bar{I}_{L\_tD}$ and $I_{L\,rms\_tD}$, the average and rms current through the inductor during dead-time (times defined in Fig. 5 and given by (7) and (8)).

Applying the new power loss model in the case of boost converter behaviour, where the voltage ratio is $V_1<V_2/2$ ($V_1>V_2/2$ for buck behaviour), the best option to achieve the highest theoretical efficiency is to try to find an optimal value for t_D (t_{D_OPT}) while always maintaining i_{Lv_OPT} equal to 0A. Under this condition, no extra dead-time power losses appear.

Conversely, when $V_1>V_2/2$, a certain pair of i_{LV}-t_D values needs to be determined. In this paper, these values are calculated for the best theoretical efficiency (based on the modified power loss model) for a voltage ratio, V_1/V_2, equal to 600V/800V, although the expressions are valid for any other voltage ratio. As can be observed in Table II and deduced from (5)-(8), the expressions are independent of the power load. They are only circumscribed to the voltage ratio and some other characteristic variables, such as w_o (which is defined as $\frac{1}{\sqrt{L \cdot C_{sw}}}$) and the effective output parasitic capacitance, C_{sw}, which is dependent on the device or the MOSFET module selected by the designer. In this particular case, the conditions needed to satisfy ZVS with the best possible theoretical efficiency are i_{Lv_OPT} equal to 0.795A and t_{D_OPT} equal to 533ns.

The practical values needed during the experimental measurements (Fig. 12) are also included (Table II) as an example of the real error during the tests. There is a certain amount of deviation from the theoretically optimal values, as the resolution of the digital control only allows 10 ns steps

for the t_D. Besides, an exact match of the analytical switching frequency and the optimal value is not always possible.

More pairs of values for i_{Lv} and t_D have been explored by increasing the minimum current at the beginning of the resonant period and correspondingly decreasing the dead-time needed. Nonetheless, all of them result in poorer analytical efficiencies. This demonstrates the validity of the study, as values of $|i_{Lv}|$ or t_D different from $i_{Lv\ OPT}$ or $t_{D\ OPT}$ do not provide better results from an efficiency point of view.

TABLE II I_{Lv} AND T_D VALUES FOR THE BEST THEORETICAL EFFICIENCY AND EXPERIMENTAL EFFICIENCY UNDER A 600V/800V VOLTAGE RATIO.

Power (W)	$i_{LV\ OPT}$ (A)	$t_{D\ OPT}$ (ns)	$i_{LV\ PRACT}$ (A)	$t_{D\ PRACT}$ (ns)
500	-0.795	533	-0.8	520
1000	-0.795	533	-0.79	550
2000	-0.795	533	-0.8	530
3000	-0.795	533	-0.85	510
4000	-0.795	533	-0.9	510

IV. EXPERIMENTAL RESULTS AND EFFICIENCIES

A. *Prototype and Set-up*

A SiC-based synchronous DC/DC boost converter was built in the laboratory (Fig. 6 and Fig. 7) to test and compare the analytical and experimental efficiencies.

The total output power is set up to 10 kW. The chosen output voltage, V_2, is 800V, considering boost behaviour, while the input voltage (V_1) varies between 200V and 600V. In addition, the SiC MOSFET module CCS050M12CM2 (three half-bridge six-pack module) by Wolfspeed® constitutes the selected power transistor. It should be noted that no modularization technique is applied in these experimental results (i_{Lv} vs t_D analysis) and the three HB receive the same control signals. Therefore, they support the same voltages, currents and power (which is the same as having a single converter with the inductance and MOSFETs formed by three in parallel). The commercial driver is a CGD15FB45P1, also manufactured by Wolfspeed®.

The maximum switching frequency is 200 kHz and the inductors are constructed using Litz wire and an ETD59-3F3 ferrite core for each module.

B. *Efficiency results*

Some considerations regarding the design of the converter for TCM-ZVS are worth highlighting next.

Initially, for a voltage ratio where V_1=400V and V_2=800V, the prototype was designed for a minimum switching frequency of 20kHz at maximum load, keeping it above the audible frequencies. Likewise, the maximum switching frequency, limited by the driver, was set at 200kHz for a very low load.

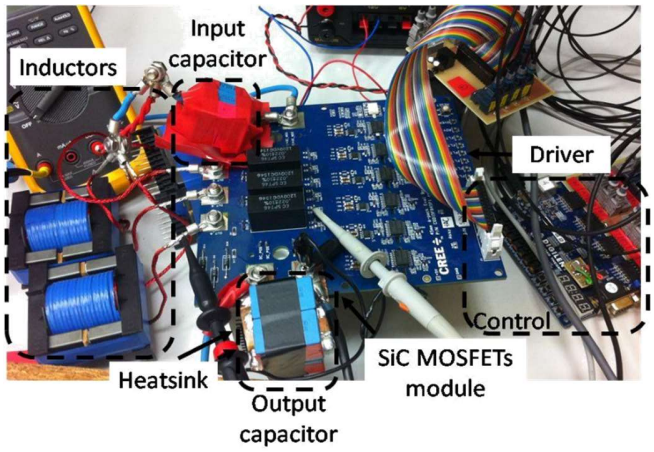

Fig. 6 Experimental prototype.

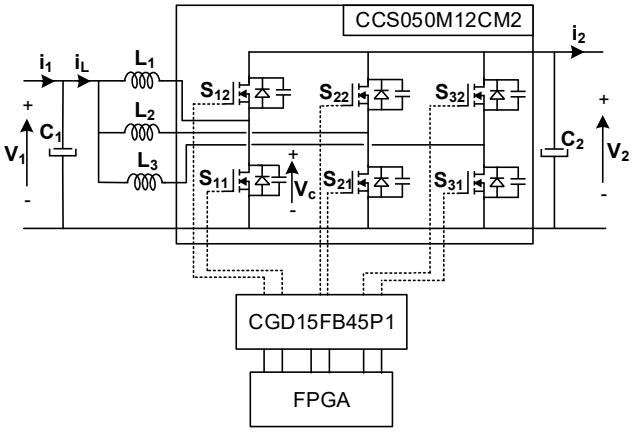

Fig. 7 Diagram of the prototype.

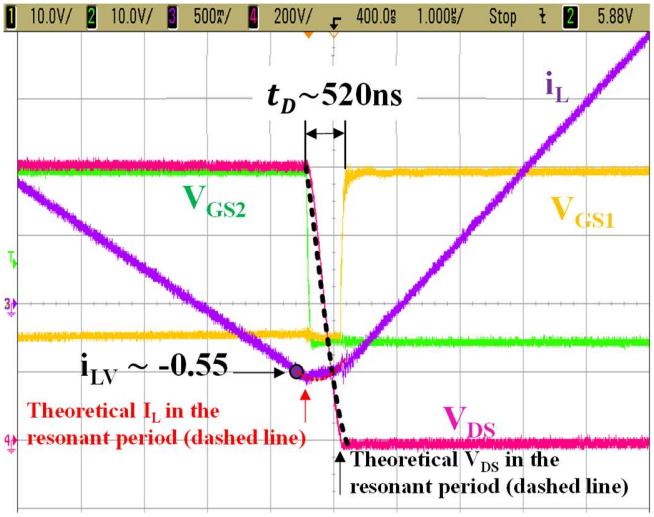

Fig. 8 Experimental waveforms of V_{GS1} (in yellow), V_{GS2} (in green), i_L (in purple), V_{DS} (in pink), theoretical I_L (red dashed line) and V_{DS} (black dashed line) during the resonant period under a voltage ratio V_1/V_2 = 500V/800V.

As an example, some experimental waveforms of the most significant voltages and currents during the resonant period are shown in Fig. 8 for a voltage ratio V_1/V_2 equal to

500V/800V, where i_{LV_OPT}=-0.525A and t_{D_OPT}=500ns. The theoretical V_{DS} and I_L waveforms during the resonant period are included for the sake of comparison, showing a good match with the corresponding experimental waveform.

In Fig. 9, analytical and experimental efficiency results are compared for a particular voltage ratio condition, $V_1<V_2/2$, where V_1=200V and V_2=800V. It should be noted that two different experimental measurements are provided in the graph: those results where an optimal value for i_{Lv} is set (i_{L_OPT}) match the estimated expected theoretical values to a great extent; and those where the i_{Lv} value is different to the optimal. In the latter case, the trend in efficiency is similar to the previous ones, though the efficiencies are slightly lower.

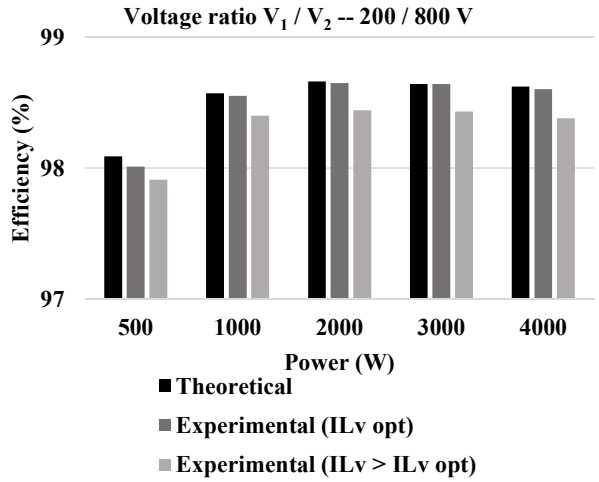

Fig. 9 Theoretical and experimental efficiencies under a 200/800V ratio.

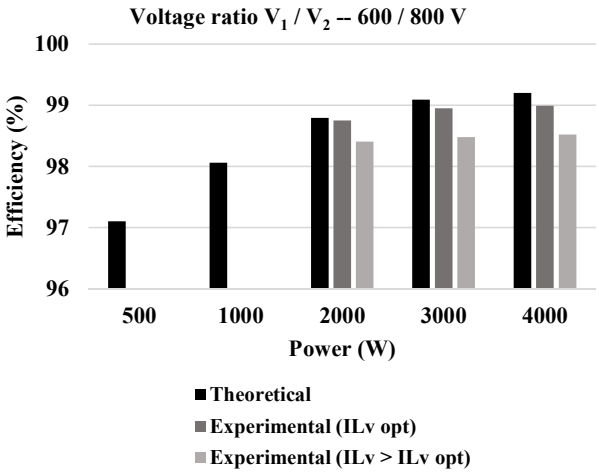

Fig. 10 Theoretical and experimental efficiencies under a 600/800V ratio.

Note that the efficiencies are quantitatively quite close to those corresponding to the initial conditions presented in the paper, where pure QSW-ZVS was possible, as V_1=400V and V_2=800V.

Equivalent efficiency results are presented in Fig. 10 for the case in which $V_1>V_2/2$, where V_1=600V and V_2=800V. Once again, the analytical values show a good match with the experimental results measured under the condition $i_{Lv}=i_{LvOPT}$, whereas the efficiencies with i_{Lv} different to the optimal value are slightly lower.

Only the results for low and medium power are provided in Fig. 9 and Fig. 10. This power range is the most interesting, as higher switching frequencies are needed for lower loads and hence more switching losses (including extra dead-times losses) will appear, making the study of i_{Lv} and t_D especially important in order to obtain an accurate power loss model.

Moreover, even if the differences between efficiencies may not seem very significant, the corresponding power loss that they cause within certain power ranges can jeopardize the design and performance of the system as a whole.

V. CONCLUSIONS

Different conduction modes in a SiC-based synchronous boost converter, in which a good match is obtained between theoretical and experimental efficiency results, have been reviewed. An accurate power loss model allows for the suitable selection of the conduction mode to improve the performance of the converter over a wide power range.

A study of the resonant period in a ZVS transition has been carried out to provide knowledge about the voltage and current waveforms in the device corresponding to the switching point during this period, an issue that is normally neglected in the literature, and the dead-time losses associated with it. Based on this study, by controlling the minimum negative current and the corresponding dead-time for different voltage ratios, ZVS can be achieved for this topology without losing high flat efficiency over a wide power range.

Using the new analytical power loss model, in which these extra dead-time losses are considered and a good match is achieved between theoretical and experimentally obtained results, the optimal values of i_{Lv} and dead-times can be obtained.

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