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An Analog Magnetic Isolator for Space Power Applications

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Abstract: In power electronic applications, often a galvanic isolation barrier has to be passed. An example of this is the feedback control of isolated DC/DC converters where the secondary voltage has to be passed to the primary side where the control circuitry lies. For these applications, the use of optocouplers is well known in terrestrial applications. However, optocouplers tend to suffer degradation from the radiation damage induced by the space environment. For this reason, some space grade DC/DC converters use some form of magnetic feedback. In this paper, a magnetic analog isolator is presented. It will allow for passing an analog voltage through an isolation barrier by means of a magnetic transformer based circuit. It will be based on an LLC DC/DC converter so the gain between both sides of the isolator can be tuned. Design methodology will be presented so the circuit can be tailored for any foreseen application. In this paper, a simulation of its application in a Latching Current Limiter is presented. All the components will be discrete components which have a rad-hard version. A design example having a bandwidth around 20 kHz and a gain of 4.6 dB is shown in the Experimental Results sections to support the analysis.

Keywords: analog isolator; resonant DC/DC converter; isolated DC/DC converter; optocoupler replacement

1. Introduction

Space electronics have to work in a very harsh environment facing extreme temperatures and high radiation doses. Furthermore, space equipment must work for many years in such a extreme environment without maintenance. For this reason, the design has to be very hardened and sometimes deviates from common designs in small details. One of such details is how to pass a galvanic isolation barrier. For example, to pass to the PWM modulator, controlling the switches of an isolated converter, the duty cycle information if the controller lies in the secondary part of the transformer. In terrestrial applications, optocouplers are usually the first choice. However, optocouplers have many limitations. Some are well known in terrestrial applications such as Current Transfer Ratio (CTR) variation, noise, and low bandwidth. However, others are more specific to space and radiation applications. With the radiation induced degradation, the CTR diminishes a lot [1,2], so the converter control loop has to compensate for that. In order to compensate for these effects, transformer-based magnetic feedback have been proposed and implemented. For example, Rad-Hard DC/DC converters from Microsemi [3] have this feature. Magnetic feedback has also been used in terrestrial DC/DC converter applications and there are integrated circuits that are used for this purpose [4]. However, to the best knowledge of the authors, besides [5,6], no specific designs have been proposed. In this paper, an analog isolator design based on a resonant DC/DC converters is proposed. The bandwidth achieved is in the range of the tens of kHz and they can offer a voltage gain wide enough to be adapted

to many requirements. Furthermore, design guides to achieve a flexible design will be provided. This isolator will be capable of driving the gate of a power MOSFET operating as a current source. All the components are discrete ones and almost all of them belong to the European preferred parts list [7].

The paper is organized as follows: Section 2 shows the background and design of the analog isolator, Section 2.3 shows one application driving the requirements or the design. The design of the circuitry is described in Section 3, and special care has been taken for the analysis of the resonant network in Section 3.1.2. A design procedure, verified by simulation, is shown in Section 4.1, and the results can be found in Section 4.2. Finally, conclusions are addressed in Section 5.

2. Design of the Analog Isolator

2.1. Concept and Reference Designs

The overall design of the analog isolator is depicted in Figure 1. The signal to be transferred is called V_{in}. Let us call the primary side of the analog isolator where V_{in} drives an amplitude modulator generating an AM modulated carrier. This AM modulated carrier is transferred through a magnetic transformer, being the primary of the magnetic transformer connected to the primary side of the isolator and the secondary of the transformer to the secondary side of the isolator. The AM modulated carrier will be demodulated with a rectifier, obtaining V_{out} which would be a scaled version of V_{in}, thus the information contained in V_{in} (e.g., the output voltage of an isolated converter to be controlled, the control action to be performed, a measurement, ...) is recovered at the secondary side of the isolator.

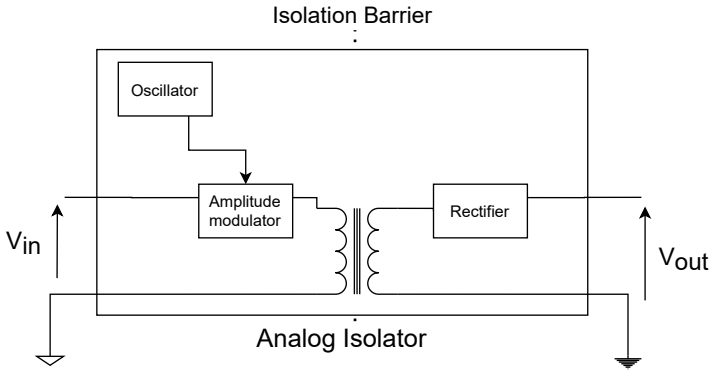


Figure 1. Analog Isolator concept.

The same concept is implemented in [5,6]. In both cases, the modulation stage derives from a DC/DC converter. In [6], the isolator is based on a forward converter operating at fixed frequency and duty ratio. The input voltage of this Forward converter is the signal to be transferred V_{in}, therefore the audio-susceptibility of the Forward converter is used to transfer V_{in}.

In [5], the AM modulator concept is also used, but it is performed in a different way. The isolation is performed by a Flyback transformer driven by a pulsed current source. To be consistent with the primary and secondary terminology, let us call the side of the transformer driven by the current source the secondary, but in a typical Flyback converter it would be the primary. This current source operates with a fixed frequency and duty ratio, and it is constant in amplitude. The voltage modulation is performed by fixing with V_{in} the Flyback rectifier output, which in this case should be called the primary. Thus, when the transformer has to be demagnetized, it will do so with voltage V_{in} which appears at the other side where it is sampled obtaining V_{out}.

It is important to note that the magnetic isolation concept have been incorporated to integrated circuits such as the UC1901 [8], in which the transformer is external. Another example with an internal transformer is Analog Devices ADUM3190S [9]. Both devices are available as space grade options. However, for certain applications, they might be a little limited. For example, ADUM3190S requires

an isolated power supply for the secondary side and the output voltage range of UC1901 can be very small for certain applications. For these reasons, a fully discrete and custom circuit that can be adapted to many input–output voltage ranges is presented here. However, for the target applications of the aforementioned ICs, they excel and surpass the capabilities of the approach presented in this paper.

This paper uses a similar approach as [6], thus no power supply is needed for the secondary of the isolator. A DC/DC converter will be used with a fixed switching frequency and duty ratio. The input voltage will be V_{in}. However, in this case, it will be based on a resonant DC/DC converter very similar to the well-known LLC converter. This topology will be described in Section 3. It uses a half-bridge for driving a resonant circuit which includes a magnetic transformer that provides the isolation. The advantages of using a resonant converter are various. First, the transformer is AC driven since C_{tank} blocks any DC voltage applied, so its magnetic material cannot saturate avoiding all the process described in [5] to avoid transformer saturation. Second, Zero Voltage and Zero Current switching can be achieved, thus a high frequency switching can be used maximizing the small-signal bandwidth of the V_{in} to V_{out} transfer functions. For the proposed design, switching frequencies in the MHz range will be preferred. Third, as the currents through most of the devices are sinusoidal, the EMI problems should be small so the spectral content will be minimized. However, the use of a resonant DC/DC converter topology is not without problems. All the elements of the resonant network and the transformer have to be carefully selected and designed. The inductor and capacitor values forming the resonant network have an impact in the V_{out}/V_{in} ratio so it can be adjusted at the designer's will. These issues will be addressed in Section 3.1.2.

2.2. Space Qualified Components' Restrictions

The use of discrete components from the European Preferred Parts List [7] imposes several challenges. Primarily, the MOSFETs that appear are high power devices not suitable for high frequency switching. Thus, all the transistors used will be bipolar junction transistors. Therefore, bipolar anti-saturation techniques will have to be implemented to enable switching at the MHz range. These techniques are described in Section 3.1.1.

2.3. Application: Latching Current Limiters

One of the design drivers of these analog isolator is its integration in a Latching Current Limiter (LCL). LCLs are a protection device used by the European Space Agency (ESA) spacecrafts. They are designed to limit the current demanded by a load to a fixed value for a certain time, thus protecting the bus from an overload. If the time is elapsed the LCL deems that there was a failure and disconnects the load. They are also used as switches. Normally, the device that limits the current is a P channel MOSFET because the source will be connected to the bus side, and it is easily driven by the current control loop, which is referred to the ground of the spacecraft. Figure 2a shows a conceptual schematic of such device. A full description of LCLs requirements are recorded in [10] and a complete set of explanations can be found in [11].

However, N channel MOSFETs usually exhibit a lower on-state resistance so the ohmic losses in the device when it is not limiting the current would be lower than in a P channel device. However, the source of the N Channel device shall be connected to the load side and thus the control loop information has to be referred to the source of the MOSFET. Here is where the analog isolator comes into play, translating the control loop voltage, referenced to the ground of the spacecraft to the gate to source voltage of the MOSFET referenced to the source. Figure 2b shows a conceptual driving of an N channel MOSFET LCL with an analog isolator. For this application, ideally the secondary side of the analog isolator (see Figure 1) does not need a power supply. This rules out the use of the Analog Devices ADUM31190S. In order to minimize the on-state resistance of the MOSFET, the maximum output voltage provided shall be close to the maximum required gate-source voltage of a MOSFET with the derating provisions [12]. This means a gate-source voltage around 15 V. This is way above the capabilities of UC1901.

As the dynamic requirements of the LCLs are very stringent regarding speed response and loop stability, the frequency response of the analog isolator shall be carefully verified. However, the design of the analog isolator shall be flexible enough to be used in other applications such as the feedback loop of an isolated DC/DC converter or in a isolated sensor.

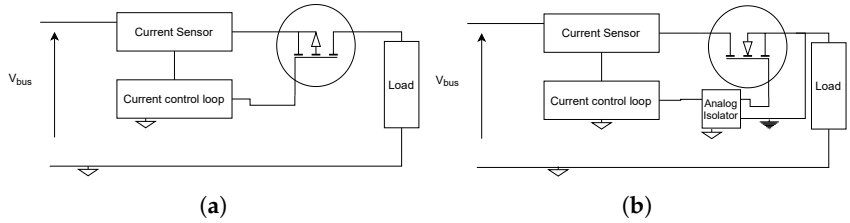


Figure 2. Latching Current Limiters: (**a**) P Channel based; (**b**) N Channel based.

3. Proposed Design

3.1. Isolator Design Description

The design of the analog isolator is depicted in Figure 3. A square wave oscillator, described in Section 3.1.1, drives a half bridge. This generates a square voltage waveform, V_{bridge}, at the input of a *LC* resonant circuit formed by C_{tank} and the leakage inductance of the transformer. The current at the switching frequency is coupled to the secondary by means of the transformer, where it is rectified and low pass filtered. The whole design of the resonant network is explained in Section 3.1.2. The amplitude of V_{bridge} is controlled by means of its supply voltage V_{sup_bridge}, which is provided by the complementary linear stage; this is the amplitude modulator. Therefore, the information contained in V_{in} modulates the amplitude of V_{bridge} and after the rectification and the filtering in the secondary is recovered as V_{out}. Therefore, V_{out} is a scaled version of V_{in}. As described in Section 3.1.2, the scaling is achieved by the design of the resonant network. Figure 4 shows different configurations for the same principle. By placing an additional op-amp with the feedback for the amplifier at the V_{sup_bridge} the base-emitter junction voltage drop is compensated. Thus, V_{sup_bridge} follows V_{in}. If the analog isolator was going to be integrated in a control loop, the operational amplifier could be used for implementing the regulator transfer function. This is represented in Figure 4b. The output of the analog isolator is the control input to the plant (e.g., in an isolated DC/DC converter, it could be the duty cycle command). The control action will be implemented by the op-amp that sets V_{in}. It will sense the output of the plant, compare it against the reference V_{ref}, and decide which control action is needed to have the output of the plant following V_{ref} (e.g., in a isolated DC/DC converter, the controlled variable is often the output voltage.) Please note how the input and output of the analog isolator are referenced with respect to the plant to be controlled. If the plant was an isolated DC/DC converter, the control and the analog isolator input would be placed at the DC/DC converter secondary and the output of the analog isolator will be referenced to the DC/DC converter primary.

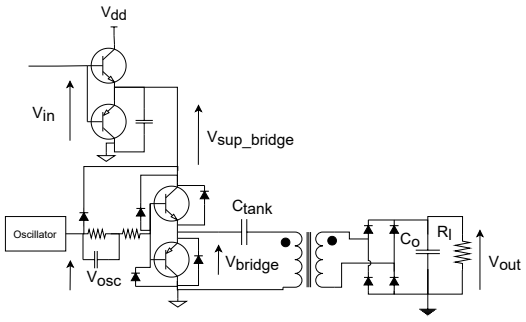


Figure 3. Analog Isolator Schematic.

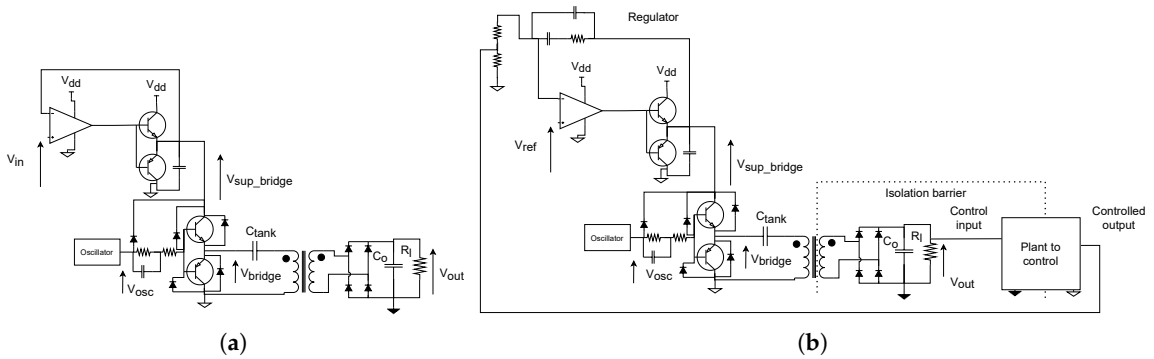


Figure 4. Analog Isolator options: (**a**) Implementation with op-amp; (**b**) Integration with control loop.

3.1.1. Oscillator and Transformer Driver

The design of the oscillator is depicted in Figure 5. A square waveform is generated by a NAND gate with Schimidt–Trigger input and a feedback network formed by R_{osc} and C_{osc}. The remaining input can be tied to positive as in the figure or to a control signal to turn on and off the oscillator. When this input is high, the NAND gate behaves as an inverter so when the voltage at C_{osc} is high, its output becomes low discharging C_{osc}, and, when it is low, the output becomes high charging C_{osc}. Therefore, R_{osc} and C_{osc} control the frequency of the oscillator. Additional gates configured as inverters provide more current to drive the half-bridge. They are implemented as NAND gates so a single chip with several gates could be used, in order to achieve a frequency in the MHz range provisions to avoid the deep saturation of the BJTs and to enhance the minority carrier extraction from the base. The latter is achieved by the presence of the capacitor connected in parallel to one of the base resistors that are needed. When V_{osc} is high, this capacitor gets charged. When V_{osc} is low, this capacitor imposes a small negative voltage in the base of the transistors.

Ideally, V_{osc} will have a maximum value of V_{dd}. If by means of tracking V_{in}, V_{sup_brige} falls below V_{dd}, the BJT collector–emitter voltage will be forward biased with a relatively high voltage, in order to prevent diode D_1 from clamping V_{osc} to V_{sup_bridge}. Diodes D_{S1} and D_{S2} further avoid the deep saturation of the BJTs. Finally, diodes D_{fw1} and D_{fw2} allow the reverse flow of the current through the bridge.

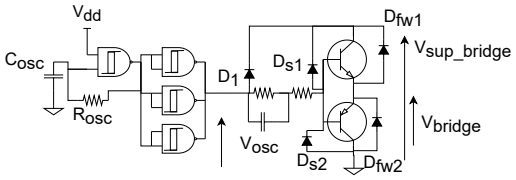


Figure 5. Oscillator and transformer driver.

3.1.2. Resonant Network Design

The resonant network design plays a fundamental role in the static gain between V_{out} and V_{in}. The procedure used to analyze and design is based on the First Harmonic Analysis (FHA), which is well referenced. The design of the LLC converter using FHA can be found in [13] or in the form of design guides in [14,15]. Basically, it will assume that, thanks to the resonant circuit formed by C_{tank} and the primary leakage inductance L_{lk1}, the only current that will circulate through the resonant tank, i_{res}, will be due to the first harmonic, at the switching frequency f_s, of the square voltage applied. The higher harmonics will generate no power at the output. In order to obtain this current, only the impedance of the reactive elements at f_s has to be taken into account. However, most of the literature neglects the effect of the secondary leakage inductance, since in most transformers this value is very low in comparison to the magnetizing inductance L_m. One of the exceptions is [16] in which it is

taken into account since it is operating at very high frequency. In this paper, the analysis will include it, since the transformer is designed to have a big leakage inductance to use it in resonance with C_{tank}. In addition, the parasitic resistances will be taken into account. Figure 6 shows the equivalent circuit for the FHA analysis. It can be seen how the bridge has been replaced by a square waveform voltage source that acts over a resonant network. The output voltage will be considered to be DC with negligible ripple thanks to capacitor C_o. Then, the full wave rectifier makes the output capacitor and load behave as a resistor of value R_{eq} with value [17]

$$R_{eq} = \frac{8}{\pi^2} R_l \tag{1}$$

The fraction of the resonant current i_{res} that circulates through this equivalent resistor R_{eq} will be called i_{res_load}. It generates a sinusoidal voltage of amplitude V_{out_1st}. This current will dissipate the same power at R_{eq} as the DC current source of value I_o over R_l. Thus, by calculating i_{res_load}, the DC output voltage V_{out} can be inferred:

$$I_o = \frac{2}{\pi} \cdot i_{res\_load} \tag{2}$$

$$V_{out} = \frac{2}{\pi} \cdot i_{res\_load} \cdot R_l \tag{3}$$

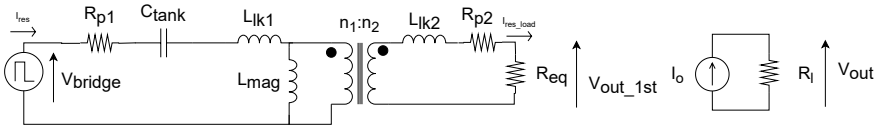


Figure 6. Network for first harmonic analysis.

The circuit in Figure 6 can be further simplified referring all the elements to the primary of the transformer, which can be done scaling it with the turns ratio $n = n1/n2$, with $n1$ being the number of turns in the primary and $n2$ the number of turns in the secondary. The result of the transformation can be seen in Figure 7.

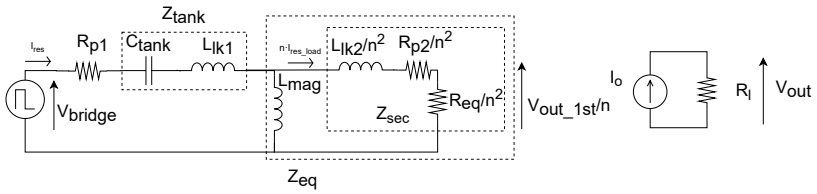


Figure 7. Equivalent network for FHA.

In our design, $n = 1$ has been chosen to simplify the transformer design. The half bridge will generate a square voltage V_{bridge} between V_{sup_bridge} an 0 V. In order to calculate i_{res_load}, the different reactive elements can be grouped. In Figure 7, they are grouped in three different impedances Z_{tank}, Z_{eq}, and Z_{sec}. Thus, in the frequency domain,

$$Z_{sec} = R_{eq} + R_{p2} + j \cdot \omega_s \cdot L_{lk2} \tag{4}$$

where ω_s is the pulsation at the switching frequency f_s. Z_{eq} is then

$$Z_{eq} = \frac{Z_{sec} \cdot j \cdot \omega_s \cdot L_m}{j \cdot \omega_s \cdot L_m + Z_{sec}} \tag{5}$$

and Z_{tank} will be

$$Z_{tank} = j \left(w_s \cdot L_{lk1} + \frac{1}{C_{tank} \cdot \omega_s} \right) \tag{6}$$

Z_{tank} will be 0 at the resonant frequency f_r

$$f_r = \frac{1}{2\pi} \frac{1}{\sqrt{L_{lk1} \cdot C_{tank}}} \tag{7}$$

In order to adjust the gain between V_{out} and V_{in}, $G_{iso} = V_{out}/V_{in}$, Z_{tank} has to be properly chosen. This is accomplished by choosing the ratio between the resonant frequency of Z_{tank}, f_r, and the switching frequency f_s, f_r/f_s; thus, Z_{tank} could be rewritten as

$$Z_{tank} = j \cdot \omega_s \cdot L_{lk\_1} \left(1 - \left(\frac{f_r}{f_s}\right)^2\right) \tag{8}$$

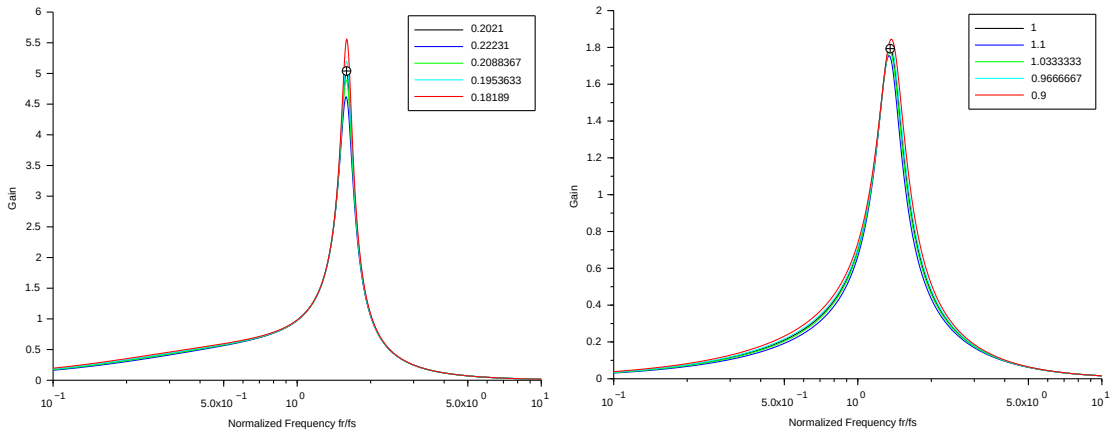
The other parameter affecting G_{iso} will be the quality factor, Q_{tank} of the resonant network

$$Q_{tank} = \frac{\frac{f_r}{f_s} \cdot \omega_s \cdot L_{lk\_1}}{R_{eq} + R_{p1} + R_{p2}} \tag{9}$$

Solving the impedance divider, it is possible to obtain the ratio between the first harmonic of V_{bridge}, V_{bridge_1st}, and the amplitude of V_{out_1st}, in absolute value is

$$G_{tank} = \frac{Z_{eq}}{Z_{eq} + Z_{tank} + R_{p1} \cdot \frac{R_{eq}}{Z_{sec}}} = \frac{V_{out\_1st}}{V_{bridge\_1st}} \tag{10}$$

As can be inferred, G_{tank} depends on the values of the primary and secondary leakage inductance of the transformer, L_{lk1}, L_{lk2} and the magnetizing one L_m. The evaluation of G_{tank} according to Equation (10) for the inductor values described in Section 4 can be found in Figure 8 for different f_r/f_s ratios and Q_{tank} values. In Figure 8a, Q_{tank} is varied around 0.2 whilst f_r/f_s varies from 1/10 to 10. In this gain, the maximum gain is close to 6. For the same f_r/f_s variation, Figure 8b shows the gain achieved with Q_{tank} varying around 1. In this case, the peak gain is around 2. It can be seen how different gain values higher than 1 can be achieved by the right combination of f_r/f_s and Q_{tank}. Having f_r/f_s bigger than 1 implies that the load seen by the half bridge is inductive. This will help discharge the parasitic output capacitance of the half bridge and have Zero Voltage Switching (ZVS) in the transistors [15].



(**a**) (**b**)

Figure 8. Gain of the resonant network: (**a**) With $Q_{tank} = 0.2$; (**b**) With $Q_{tank} = 1$.

The amplitude of the first harmonic of V_{bridge} can be calculated by decomposing a square waveform at frequency f_s between V_{in} and 0 with duty cycle D into its Fourier series components

$$V_{bridge}(t) = V_{in} \cdot \left(D + \sum_{k=1}^{\infty} \frac{2}{k \cdot \pi} \sin(k \cdot \pi \cdot D) \cdot \cos(2\pi \cdot k \cdot \pi \cdot D \cdot f_s \cdot t) \right) \tag{11}$$

Therefore, with $D = 0.5$, the amplitude of the first harmonic $V_{bridge\_1st} = V_{in} \cdot \frac{2}{\pi}$. Then,

$$V_{out\_1st} = G_{tank} \cdot \frac{2}{\pi} \cdot V_{in} \tag{12}$$

and

$$i_{res\_load} = \frac{V_{out\_1st}}{R_{eq}} = G_{tank} \cdot \frac{2}{\pi} \cdot \frac{1}{R_{eq}} \cdot V_{in} \tag{13}$$

Then, applying (1) and (3) V_{out} is

$$V_{out} = \frac{2}{\pi} \cdot i_{res\_load} \cdot R_l = \frac{4}{\pi^2} \cdot \frac{R_l}{R_{eq}} \cdot G_{tank} \cdot V_{in} \tag{14}$$

and then $G_{iso} = V_{out}/V_{in}$

$$G_{iso} = \frac{1}{2} \cdot G_{tank} \tag{15}$$

and for a square waveform with duty cycle D

$$G_{iso} = \frac{1}{2} \cdot G_{tank} \cdot \sin(k \cdot \pi \cdot D) \tag{16}$$

4. Experimental Results

4.1. Design Procedure

The design of the analog isolator would be oriented to achieve a certain gain G_{iso} fixed at design stage so it could be integrated in the application. This gain would be achieved through the process described in Section 3.1.2. However, there are many degrees of freedom so the same goal could be achieved by several means. The process used for this paper is described below.

1. Choose a the switching frequency at least 10 times higher than the desired bandwidth. In this case, it was set to 4 MHz.
2. Design a transformer. The turns ratio will be 1. This will fix the values of L_{lk1}, L_{lk2} and L_m which can be obtained by measurement or by simulation through a finite element analysis software.
3. Choose the desired G_{iso} and therefore G_{tank}. Plot Equation (10) with different ranges of Q_{tank} and f_r/f_s. The values of the resistances r_{p1} and r_{p2} can be approximated by the parasitic resistance of the windings plus the ESR of the resonant capacitor.
4. With G_{tank} selected to achieve G_{iso} fix Q_{tank} and f_r/f_s. The latter with the selected f_s determines f_r.
5. With f_r and L_{lk1}, select C_{tank} using Equation (7).
6. With L_{lk1} and f_r, select R_{eq} that guarantees the desired Q_{tank} using Equation (9).
7. Transform R_{eq} to R_l using Equation (1) to finish the design.

In order to verify the resonant network design, a PSIM simulation was carried out. The design of the resonant circuit is based on having a $Q_{tank} = 0.2$. The switching frequency was fixed at 4.08 MHz with a duty cycle $D = 0.5$ and the objective is to achieve the maximum gain. Thus, $f_r/f_s = 1.59$ and then $f_r = 6.5$ MHz. The transformer is characterized by $L_{lk1} = L_{lk2} = 8.8$ µH and $L_m = 14.3$ µH with Parasitic resistances $r_{p1} = r_{p2} = 1.12$ Ω. In order to achieve the desired f_r, then $C_{tank} = 68$ pF and Q_{tank} are guaranteed with a $R_l = 2.2$ kΩ. Following Equation (10) and Figure 8a, it is possible

to derive a value of $G_{tank} = 5.04$, thus achieving $G_{iso} = 2.52$. Results of the simulation can be seen in Figure 9. It can be seen how V_{bridge} is a square waveform of the desired frequency with an amplitude equal to V_{in} and how V_o is significantly higher. In addition, the resonant current i_{res} is very sinusoidal, highlighting the FHA assumption that only the current at the switching frequency circulation is correct. The simulated value for $G_iso \approx 2.49$, very close to the predicted value.

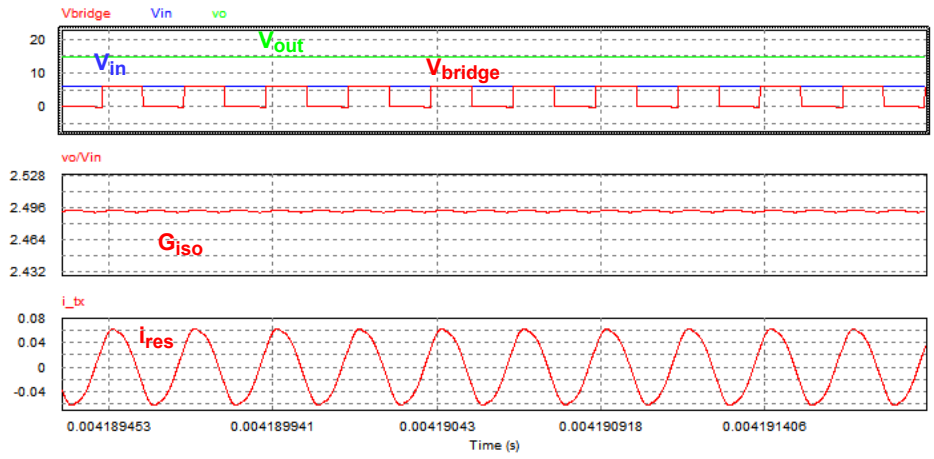


Figure 9. PSIM simulation results.

4.2. Prototype Measurements

Using the procedure described in Section 4.1, an analog isolator was constructed. It was designed to have a $G_{iso} = 2.5$ using a switching frequency $f_s = 4$ MHz.

The schematic of Figure 4a was implemented as a prototype to verify the behavior of the system. Following the necessity of using space qualified components (preferably from [7]), all the NPN transistors are 2N2222 and the PNP are 2N2907 and the diodes are 1N4148. The oscillator is built using a CD4093B CMOS NAND gate array, which features four gates and the op-amp is the LT6020 from Analog Devices, which has a space grade counterpart.

The transformer was implemented using a small iron powder toroidal core from Micrometals. The size is a T37 and the material is the -8. These magnetic cores are usually used implementing transformers and inductors for RF and power conversion applications. With this material, the permeability variation against frequency is negligible up to 20 MHz. The toroidal shape implies that the only way for adjusting L_m is the number of turns and in order to adjust L_{lk1} and L_{lk2} the separation of the windings shall be controlled. In the design, $L_m = 14$ µH and $L_{lk1} = L_{lk2} = 8.8$ µH, which are very close with the values simulated with ANSYS PEmag. Note how similar that L_m is to L_{lk1}. This is the reason behind the analysis performed in Section 3.1.2. The parasitic resistances considered are $r_{p1} = 1.12\ \Omega$ and $r_{p2} = 1.12\ \Omega$. Having the winding separated also contributes to minimizing the parasitic capacitance between the primary and the secondary of the transformer. No other stray capacitances were considered since the ones to the enclosure will greatly depend on the final implementation.

The goal would be to have a gain $G_{tank} = 5.0$. The design procedure leads to having $C_{tank} = 68$ pF and $R_l = 2.2$ kΩ. The output capacitor $C_o = 22$ nF. It is important to remark that the current through C_{tank} will have a frequency of 4 MHz, so high frequency RF capacitors shall be used since normal ceramic ones will have a very high ESR. With this design, gain G_{tank} should be 5 and therefore $G_{iso} = 2.5$.

The prototype is supplied with $V_{DD} = 15$ V. The main waveforms of the analog isolator can be seen in Figure 10. The isolator is tasked there to track voltage V_{in}, which is a DC voltage of 6 V (depicted in green). The oscillator output waveforms (depicted in yellow), which should be 15 V amplitude, are clamped to 7 V, which is the V_{sup_bridge} voltage plus the voltage drop in the diode. This avoids BJT saturation. It can be appreciated how V_{bridge} (depicted in blue) rises before the oscillator indicating

ZVS behavior in the bridge. It can be seen how the isolator provides a gain having an output voltage of $V_{out} = 9.54$ V (depicted in purple). Thus, having a gain of $G_{iso} = 1.59$, which according to (15) would mean that $G_{tank} = 3.18$, way below the target value of $G_{tank} = 5$. However, the expression of (11) is for a perfectly square waveform between 0 and V_{in}. In Figure 10, it can be seen how the minimum value of V_{bridge} is around 0.7 V. This is coincident with the fact that the saturation voltage of the BJTS is around 0.7 V. Moreover, (11) is for a duty cycle of $D = 0.5$; in the waveforms, it is around $D = 0.55$. Then, the first harmonic of the voltage is smaller than the one calculated by (11). Re-evaluating G_{tank} using (16) with the amplitude and duty cycle measured with the oscilloscope for V_{bridge} (then having $V_{in} = V_{bridge\_max} - V_{bridge\_min}$), the value obtained is $G_{tank} = 4.88$, which is much closer to the theoretical value.

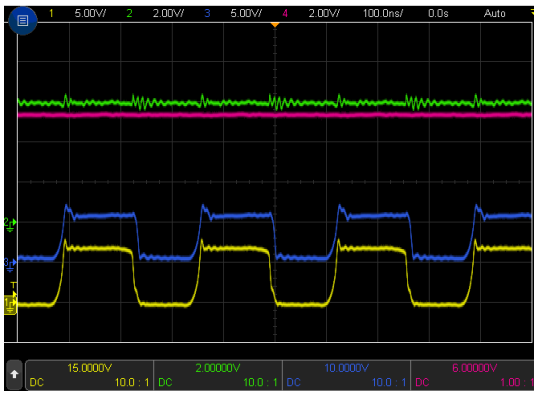


Figure 10. Waveforms of the isolator.

As this isolator is designed to track varying voltages and to integrate it in control loops, it is necessary to measure the transfer function between V_{in} and V_{out} using a network analyzer around the DC point of 6 V. The frequency range was between 10 Hz and 1 MHz. Results can be seen in Figure 11. It can be seen how the gain is flat up to 20 kHz having a small signal gain at 10 Hz of G_{iso_ss} = 4.6 dB, which in natural units is $G_{iso\_ss} = 1.69$, very close to the static gain measured $G_{iso} = 1.59$. This frequency behavior has to be taken into account for integrating the analog isolator in a control loop such as in Figure 4b.

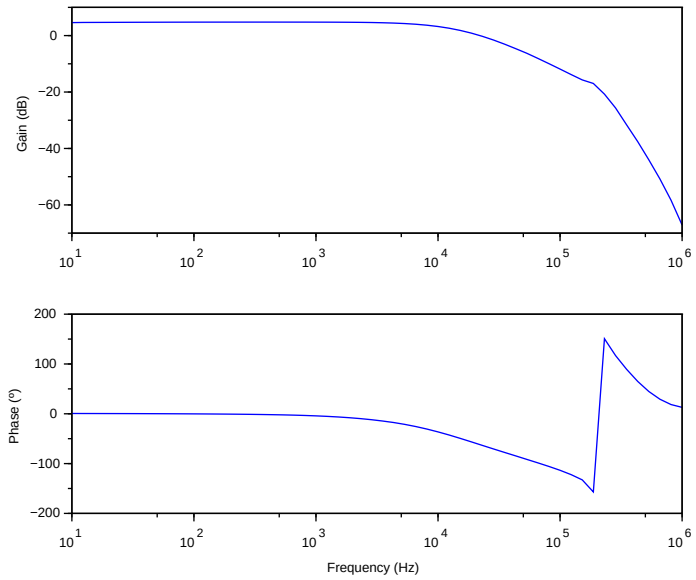


Figure 11. Bode plot of the gain of the Analog Isolator.

The Bode plot of Figure 11 was used to tune the current control loop of an LCL based on an N channel SiC MOSFET. The circuit for the LCL (depicted in Figure 2b) with the current sensor, the controller, and the analog isolator were simulated in LTSPICE. Figure 12 shows the result of the simulation. It can be seen how the measured current is below the reference. After a faulty overload, the control loop reacts lowering the gate to source voltage. This makes the MOSFET operate as a current source and then it limits the current demanded by the load. It can be seen how the measured current follows the reference value in a smooth way without any oscillation. This verifies the applicability of the analog isolator design for driving the gate of a MOSFET operating as a current source.

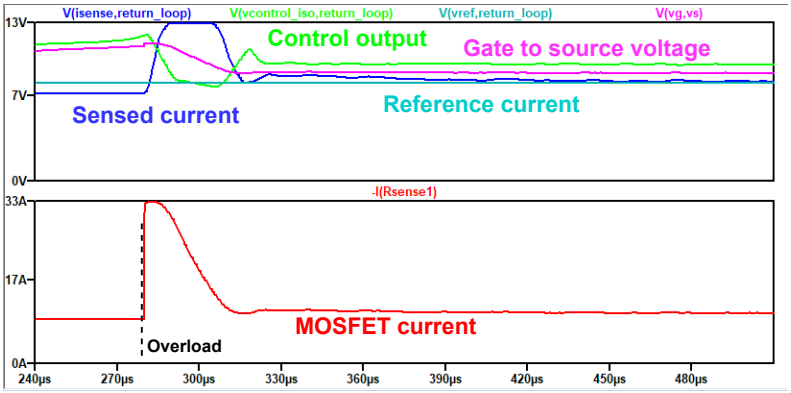


Figure 12. LTSPICE simulation results of the LCL.

5. Conclusions

The present paper shows a design of an analog isolator capable of being integrated in power applications. As its design uses discrete rad-hard components, it can be used in space applications. The design procedure is flexible enough so it can be tailored for specific applications. The static gain can be adjusted by means of adjusting the resonant tank but margins for taking into account the saturation voltage of BJTs and other non-idealities shall be considered. No power is necessary for the secondary part of the isolator making it adequate for driving the gate of an N channel MOSFET in linear mode thus controlling a Latching current limiter.

As desired, the bandwidth is quite high, making it capable of complying in simulation with the requirements of the Latching current limiters which was the target application. Nonetheless, it can be used for other applications in which a measurement of an isolated voltage is needed.

The proposed design is based on an LLC converter. However, other DC/DC converters can be used for the same application based on the principle of changing the input voltage. The LLC allows for adjusting the gain, but it is a complicated design. For other applications, other topologies can be used. One of the drawbacks is that it can only measure a positive voltage. Some modifications will be needed for negative ones.

The design also shows one of the characteristics of space applications. As the devices shall be rad-hard, the availability is much scarce. For the present design, it meant going for a fully discrete implementation. The switching devices (BJTs) are probably not the best option. For a terrestrial application (provided that some of the characteristics of the presented magnetic isolator were desired), it would have been better to use P and N MOSFETS driven by logic levels. Even better, it would have been to use a high current high speed inverter or a high speed MOSFET driver as the Renesas EL7156 as the switching half-bridge. However, to the best knowledge of the authors, such devices are not available as space grade components.

The use of a discrete approach has also one advantage. It is easier to investigate the effect of failures in the individual components rather than in an integrated circuit. These are the analysis known as Failure Mode Effect and Criticality Analysis (FMECA) which are required for any space application.

In summary, the paper presents an analog isolator design compatible with space power application that can be tailored to specific requirements regarding isolation, gain, and bandwidth.

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