Realizable reference anti-windup implementation for parallel controller structures

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***Abstract*—Parallel controller structures are often used for the control of harmonic components in those power converters including harmonic compensation functions. The controlled signal can be distorted during voltage saturation of the power converter output. This paper proposes an implementation of the realizable reference anti-windup technique suitable for parallel controllers in multiple reference frames. The proposed implementation is simple and does not require a particular type of controllers nor special controller arrangements. The proposed implementation can be used for any kind of linear controller structure regardless of the variables being controlled. In the context of harmonic current controllers, the anti-windup implementation allows separating the harmonic controller outputs for canceling or decreasing them during steady-state saturation to improve the waveform quality. Different saturation options are analyzed for the inner-loop current controller of grid-forming converter applications.**

***Index Terms*—Current control, harmonic compensation, saturation, parallel controllers, multifrequency**

I. Introduction

Distributed power generation systems (DPGSs) have increased their presence in the grid, especially those based on renewable energies, like solar or wind energy [1]. Microgrids capable to operate independently of the grid are also increasing in size and quantity [2]. In both cases, there is a high percentage of non-linear loads [3] injecting a significant amount of current harmonic content that eventually can distort the grid voltage. Therefore, requirements for harmonics content have been toughened up to improve general power quality [4]. Harmonic compensation can be implemented using dedicated units, as passive filters or centralized active filters [5], [6] increasing the system cost. However, since the interface of DPGSs is generally based on power converters, this opens opportunities for harmonic compensation [6]. Harmonic compensation increases the voltage and current controller complexity requiring parallel structures [1]. The most used are those based on proportional-resonant (PR) controllers [7], also known as second-order generalized integrators (SOGI); and those based on synchronous proportional-integral (PI) controllers, implemented either in the synchronous or stationary reference frames [8], [9], also known as reduced-order generalized integrators (ROGI).

Despite the controller type or design, there is always a maximum voltage available for compensation. Due to this, the current controller voltage demand can exceed the maximum available voltage under heavy load conditions, supply voltage drop, or if there is a sudden change of power demand. During a saturated state, two problems may arise: controller wind-up and harmonic distortion. Both situations can produce potentially dangerous overcurrents: windup can lead to a large overshoot in the controller response when the voltage is reestablished and harmonic distortion can produce the loss of synchronization in grid-feeding applications, also leading to overcurrent.

There are different anti-windup methods for parallel controllers in the literature [10]–[16]. The controller wind-up can be avoided by individually saturating the parallel controllers to different preset values [10]. However, this solution does not ensure an efficient voltage utilization and correct transition from saturated to non-saturated state. A back-tracking algorithm with proportionally assigned gains for each controller has been proposed [11] to overcome this issue. Again, the need for preset saturation limits for each controller makes the solution inefficient in a general case. A state feedback anti-windup algorithm is proposed in [12]. This solution is essentially the same as [10], [11] with a state-space formulation. A conditional cancellation of the multiple reference frame parallel controllers is proposed in [13]. It requires tuning of a voltage threshold to disable the controller integrators as well as the calculation of the control signal derivative to enable and disable the cancellation of the different controllers. The slow dynamic response of this solution makes it inefficient for continuously varying conditions. Moreover, it requires a particular controller structure. An interesting method has been recently proposed [16] for controllers in stationary reference frame. The anti-windup mechanism is locally applied to the different controllers in the parallel structure. The saturation

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limits for each controller are calculated at every control sample following different strategies.

An effective realizable reference (RR) anti-windup technique has been recently presented for stationary reference frame parallel controllers [14], [15]. The implementation requires a special formulation for the controller since it is efficiently implemented as a single transfer function. Unfortunately, this prevents manipulation of the individual parallel controllers outputs, which can be used to minimize harmonic distortion as will be discussed next. Moreover, the solution cannot be used when different types of controllers are used, or in different reference frames.

Along with the windup problem, saturation also produces waveform distortion in the controlled signals and there have been different proposals to mitigate its effect [16]–[26]. A trajectory analyzer is proposed in [17], [18] to limit the controller output in case of saturation and avoid harmonic injection. This analyzer is used to adapt the output voltage in stationary reference frame. The main drawback is that due to its complexity it is limited to fundamental and negative sequence harmonic controllers. Moreover, the saturation is considered with respect to the hexagon inner circle, limiting the dc-link usage. A back-tracking scheme is proposed in [19] for a parallel structure based on ROGI in multiple reference frames. When output saturation is produced, the different voltage components are adjusted in such a way that lesser priority harmonics are removed from compensation. Although simpler, this method does not entirely eliminate the distortion and requires a particular controller structure. [20] proposes also a saturation scheme for a parallel structure based on ROGI. When output saturation is produced, the different voltage components are adjusted following a gain adjustment. The dynamic behavior of this method is improved in [21], while it is extended to multi-phase machines in [22]. This proposal was further improved in [23], including current limits to the control algorithm. The main drawbacks of this method are the required tuning process and the dynamic performance since the gain adjustment is driven by integral controllers. In [24], a partial current harmonic compensation for dual three-phase permanent magnet synchronous machines (PMSM) is proposed, based on manipulating the reference signals for the current harmonics. Since this scheme is presented for an electric machine, torque production (fundamental component) is favored over the current harmonics, whose control is completely disabled if necessary. In this paper, only 5^{th} and 7^{th} harmonics are taken into consideration; the partial compensation is based on finding the optimal compensation level for each current harmonic (λ_h) based on a previous commissioning process, which makes it impractical for general application. [25] proposes an instantaneous method that calculates a trajectory that avoids overmodulation at every time step to reduce the total harmonic distortion (THD) maximizing the power injected to the grid. However, this method is based on analytically solving non-linear equations any time that a trajectory reduction is predicted, which also increases the complexity as the number of harmonics to compensate increases. In practice, the method maintains a low THD of the injected current by decreasing the reactive power. The computational burden of this method is reduced in [26]. Three saturation strategies intended for active power filters are compared in [16]. The saturated voltage is calculated at every control step in all cases.

This paper generalizes the instantaneous realizable reference algorithm for application in parallel controller structures which has been initially drafted in conference paper [27]. The proposed anti-windup implementation allows the proper saturation of controllers in multiple reference frames and it does not require gain tuning. Furthermore, it is not restricted to any special type of controllers, allowing to develop new controller types and combine different controllers in different reference frames. It is also noted that the proposed implementation can be applied to any parallel controller structures regardless of the variables being controlled.

The proposed anti-windup implementation is independent of the strategy followed to reduce harmonic distortion during saturation in current controllers. Cancellation or minimization of the compensation of lower priority harmonics during saturation is easily achieved. If required, any controller in the parallel structure can be easily disabled by just setting its output to zero. It can also be used in combination with the trajectory-based methods proposed in the literature.

The anti-windup method is tested for proper saturation of the inner-loop current controllers of a grid forming application, although it is suitable for any application (e.g. grid support, electric drives, etc.). In this regard, the paper analyzes different options for the selection of the saturated voltage vector to minimize current waveform distortion, recommending one especially suited for grid-forming applications. In general, researchers have focused on the concept of "distortion-free" saturation methods [18]–[22], [25] for grid injection and electrical machine current control. The main goal is preserving the sinusoidal waveform shape of the currents injected to the grid or electrical machines, rejecting harmonic distortion to comply with grid codes or to minimize the torque ripple. However, this always implies the reduction of the fundamental component magnitude. This will reduce the injected power to the grid or the fundamental torque component in electrical machines. In the case of electrical machines, that strategy is questionable but can still be useful for certain applications. However, it will be shown that for grid-forming applications in the presence of non-linear loads, the saturation strategy goal might be different since the preservation of the fundamental component magnitude is a main requirement. The paper analyzes this extent.

This paper is organized as follows: the realizable reference anti-windup implementation for parallel controllers is explained in Section II; different saturated voltage vector selection strategies applied to the inner-loop current controllers of grid forming applications are described in Section III; the comparison of the proposed strategies is analyzed in Section IV, where simulation results in open and closed-loop are provided with a special focus in grid-forming applications;

experimental results are presented in Section V; finally, a summary of proposed ideas is found in Section VI.

II. Realizable reference for parallel controllers

A. Basic concept

The transfer function of a discrete-time controller can be expressed as

$$D(z) = \frac{u(z)}{\varepsilon(z)} = \frac{b_0 + b_1 z^{-1} + \cdots + b_n z^{-n}}{1 + a_1 z^{-1} + \cdots + a_n z^{-n}} \tag{1}$$

assuming it has the same number n of poles as zeroes, where u is the controller output (i.e. inverter output voltage in a current controller); ε is the error signal (i.e. current error in a current controller); and b_i and a_i $(i = 1, 2, ...n)$ are the polynomial coefficients. Note that u and ε can be either scalar or complex vector quantities, as well as the polynomial coefficients.

The assumption of having the same number of poles as zeroes is not very restrictive since all continuous-time controllers discretized using the bilinear (Tustin), matched pole-zero, first-order hold, or backward Euler approximations will meet this condition. For the zero-hold, forward Euler, or modified matched pole-zero approximations this condition is not necessarily met, resulting in discrete-time transfer functions that may have one more pole than zeroes. This can be circumvented by adding $\frac{T}{2}(z+1)$ to the numerator of the controller, where T is the sampling period; the new controller exhibiting a very similar response. Nevertheless, the discussion will be later extended to the case the controller transfer function might have a different number of poles than zeroes.

The difference equation needed for computer (e.g. microcontroller) implementation can be easily obtained as

$$u[k] = \sum_{i=0}^{n} b_i \varepsilon[k-i] - \sum_{i=1}^{n} a_i u[k-i] \tag{2}$$

The controller output must be limited to the actuator operating range to avoid controller windup. In case of scalar output (i.e. using dc power source), a maximum and minimum voltage will be easily set

$$u[k] = u_{\text{sat}} = \begin{cases} u_{\max}, \text{if } u[k] > u_{\max} \\ u_{\min}, \text{if } u[k] < u_{\min} \end{cases} \tag{3}$$

In the case of a complex vector output (i.e. using a three-phase inverter), more complicated expressions apply. Fig. 1(a) shows the maximum allowable voltage range using a three-phase inverter. It is given by a hexagon with radius $\frac{2}{3}V_{dc}$ and apothem $\frac{V_{dc}}{\sqrt{3}}$, being V_{dc} the dc-link voltage. When the amplitude of a voltage command u surpasses the voltage hexagon limits, its amplitude must be limited or its phase distorted. In this case, multiple options exist. Commonly used options are shown in Fig. 1(a): u_{sat} keeps the original vector angle; u_{sat1} maximizes $q-$axis component; u_{sat2} maximizes the $d-$axis component. The hexagon limitation maximizes the inverter voltage utilization but brings implementation complexity, reference frame dependence, and the injection of additional harmonics when the voltage moves along the hexagon sides. To avoid this, the hexagon inscribed circle seen in Fig. 1(b) is often selected as voltage limit. To achieve those limits either Sinusoidal PWM (SPWM) with third harmonic injection or Space Vector Modulation (SVM) are required.

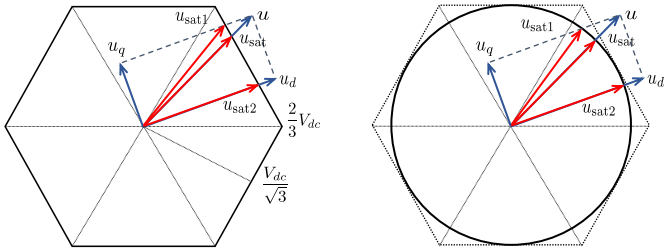

Fig. 1. Complex vector voltage limits. (a) Hexagon saturation. (b) Circle saturation.

Limitation of the digital controller output to the actuator limits prevents from windup, but does not ensure a correct controller operation during the saturation state and a fast transition to normal operation when the saturation cause ceases. There exist different anti-windup mechanisms, as described in the introduction; the back-calculation or realizable reference method [28], [29] being the most effective and straightforward for digital implementation. It consists of calculating the error signal that would have made the controller to exactly produce the saturated output

$$\varepsilon_{\text{sat}} = \frac{1}{b_0}\left(u_{\text{sat}} - \sum_{i=1}^{n} b_i \varepsilon[k-i] + \sum_{i=1}^{n} a_i u[k-i]\right) \tag{4}$$

This value will be used as the previous step error signal in the next control period. This makes the controller always operate in the linear region, even under output saturation. Calculation of ε_{sat} requires recalculating the last two terms on the right side of (4) or storing those values during the controller computation. A simpler implementation is proposed next for later extension to parallel controllers.

B. Efficient implementation

The controller difference equation seen in (2) can be rewritten by extracting the first polynomial coefficient out of the summation

$$u[k] = b_0 \varepsilon[k] + \sum_{i=1}^{n} b_i \varepsilon[k-i] - \sum_{i=1}^{n} a_i u[k-i] \tag{5}$$

In case of saturation, the saturated controller output as a function of the realizable error (i.e. realizable reference minus present output) can be calculated as

$$u_{\text{sat}} = b_0 \varepsilon_{\text{sat}} + \sum_{i=1}^{n} b_i \varepsilon[k-i] - \sum_{i=1}^{n} a_i u[k-i] \tag{6}$$

By subtracting (5) from (6) a simpler expression only dependent on the last terms can be obtained

$$u_{\text{sat}} - u[k] = b_0 \left(\varepsilon_{\text{sat}} - \varepsilon[k]\right) \tag{7}$$

Therefore, the realizable error can be easily calculated by only using the present period input and output of the controller

$$\varepsilon_{\text{sat}} = \varepsilon[k] + \frac{1}{b_0}\left(u_{\text{sat}} - u[k]\right) \tag{8}$$

C. Parallel controllers in stationary reference frame

In grid-forming, grid-connected, or active filter inverters, parallel controllers are often used for the control of the fundamental current (or voltage) and its harmonics. A structure using stationary reference frame parallel controllers can be seen in Fig. 2.

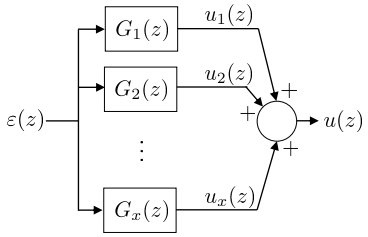

Fig. 2. Block diagram of a stationary reference frame parallel controller structure.

A back-calculation or realizable reference anti-windup implementation has been proposed for a parallel structure composed of one proportional plus resonant harmonic controllers [14], [15] in a per phase scalar structure. The implementation in [14], [15] allows the independent design of the fundamental and harmonic controllers and a straightforward anti-windup computation. The drawbacks are: 1) It requires a special arrangement of the controllers; 2) The structure is limited to proportional plus resonant controllers; 3) Individual controller outputs cannot be analyzed or limited; 4) It is only intended for controllers implemented in stationary reference frame; 5) It is intended for scalar implementation. The anti-windup implementation proposed in this paper overcomes those limitations.

The difference equation for the individual controllers are:

$$u_1[k] = b_{1,0}\ \varepsilon[k] + \sum_{i=1}^{n_1} b_{1,i}\ \varepsilon[k-i] - \sum_{i=1}^{n_1} a_{1,i}\ u_1[k-i] \tag{9a}$$

$$u_2[k] = b_{2,0}\ \varepsilon[k] + \sum_{i=1}^{n_2} b_{2,i}\ \varepsilon[k-i] - \sum_{i=1}^{n_2} a_{2,i}\ u_2[k-i] \tag{9b}$$

$$\vdots$$

$$u_x[k] = b_{x,0}\ \varepsilon[k] + \sum_{i=1}^{n_x} b_{x,i}\ \varepsilon[k-i] - \sum_{i=1}^{n_x} a_{x,i}\ u_x[k-i] \tag{9c}$$

They are computed as x independent controllers, where $u_j (j = 1, 2, \cdots, x)$ are the controller outputs, and $b_{j,i}$ and $a_{j,i} (i = 1, 2, \cdots, n)$, are the discrete-time controller coefficients. Please, note the error signal is common for all of them. The total controller output is the sum of the individual controller outputs

$$u_T[k] = \sum_{i=1}^{x} u_i[k] \tag{10}$$

An identical result is obtained by summing the controller difference equations in (9), resulting in

$$u_T[k] = \sum_{l=1}^{x} b_{l,0}\ \varepsilon[k] + \sum_{l=1}^{x}\sum_{i=1}^{n_l} b_{l,i}\ \varepsilon[k-i] - \sum_{l=1}^{x}\sum_{i=1}^{n_l} a_{l,i}\ u_l[k-i] \tag{11}$$

Similarly to the single controller case, replacing the present output and error signal by their saturated counterparts, gives

$$u_{\text{sat}} = \sum_{l=1}^{x} b_{l,0}\ \varepsilon_{\text{sat}} + \sum_{l=1}^{x}\sum_{i=1}^{n_l} b_{l,i}\ \varepsilon[k-i] - \sum_{l=1}^{x}\sum_{i=1}^{n_l} a_{l,i}\ u_l[k-i] \tag{12}$$

Finally, subtracting (11) from (12), and after clearing ε_{sat}, yields

$$\varepsilon_{\text{sat}} = \varepsilon[k] + \frac{1}{\sum_{l=1}^{x} b_{l,0}}\left(u_{\text{sat}} - u_T[k]\right) \tag{13}$$

The obtained result shows the error back-calculation process is as simple as for the single controller. It must be remarked that (11) does not need to be computed; the parallel implementation, (9) and (10), are used instead. Finally, the fraction of saturation voltage corresponding to each parallel controller must be calculated

$$u_{l\_\text{sat}} = u_l[k] + b_{l,0}\left(\varepsilon_{\text{sat}} - \varepsilon[k]\right) \text{ for } l = 1, 2, ..., x \tag{14}$$

It is noted that only (13) and (14) must be computed for the anti-windup implementation once the saturated voltage (u_{sat}) is obtained. This implementation is advantageous since it allows disabling some harmonic controllers in case of saturation as it will be discussed in Section III. Moreover, it mitigates rounding errors when combining large and small coefficients of the parallel controllers in a single controller implementation due to the numerical precision of the digital system [30].

In a general case, the parallel controllers can be designed and implemented in different reference frames. Therefore, a realizable reference anti-windup implementation for multiple reference frames will be described next.

D. Parallel controllers in multiple reference frames

Different reference frames can be used for the design and implementation of the different controllers in the parallel structure as can be seen in Fig. 3.

The error signal is first transformed into the different reference frames. Each controller produces an output in its own reference frame; and finally, the outputs are transformed

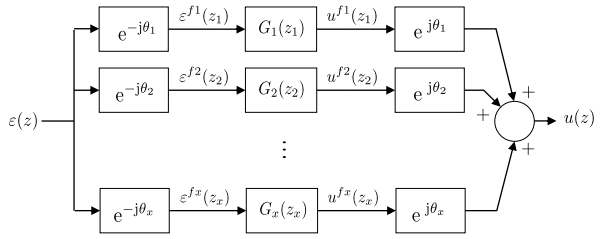

Fig. 3. Block diagram of a multiple reference frame parallel controller structure.

into a common reference frame (i.e. stationary) and added up. Superscript fl $(l = 1, 2, ..., x)$ is used to specify the different reference frames for the parallel controllers. The difference equations for the parallel controllers can be expressed as

$$u_1^{f1}[k] = b_{1,0}\ \varepsilon^{f1}[k] + \sum_{i=1}^{n_1} b_{1,i}\ \varepsilon^{f1}[k-i] - \sum_{i=1}^{n_1} a_{1,i}\ u_1^{f1}[k-i] \tag{15a}$$

$$u_2^{f2}[k] = b_{2,0}\ \varepsilon^{f2}[k] + \sum_{i=1}^{n_2} b_{2,i}\ \varepsilon^{f2}[k-i] - \sum_{i=1}^{n_2} a_{2,i}\ u_2^{f2}[k-i] \tag{15b}$$

$$\vdots$$

$$u_x^{fx}[k] = b_{x,0}\ \varepsilon^{fx}[k] + \sum_{i=1}^{n_x} b_{x,i}\ \varepsilon^{fx}[k-i] - \sum_{i=1}^{n_x} a_{x,i}\ u_x^{fx}[k-i] \tag{15c}$$

After computation of the parallel controllers, the total output can be easily obtained

$$u_T[k] = \sum_{l=1}^{x} u_l[k] = \sum_{l=1}^{x} u_l^{fl}[k]\ \mathrm{e}^{\,\mathrm{j}\theta_l[k]} \tag{16}$$

where $\theta_l[k]$ is the angular position of the fl reference frame in the present sampling period and 'e' the Euler number.

Summing the difference equations in (15) after transforming them to a stationary reference frame, gives

$$\begin{aligned} u_T[k] = &\sum_{l=1}^{x} b_{l,0}\ \varepsilon^{fl}[k]\mathrm{e}^{\,\mathrm{j}\theta_l[k]} + \sum_{l=1}^{x}\left(\sum_{i=1}^{n_l} b_{l,i}\ \varepsilon^{fl}[k-i]\right)\mathrm{e}^{\,\mathrm{j}\theta_l[k]} \\ &- \sum_{l=1}^{x}\left(\sum_{i=1}^{n_l} a_{l,i}\ u_l^{fl}[k-i]\right)\mathrm{e}^{\,\mathrm{j}\theta_l[k]} \end{aligned} \tag{17}$$

Writing the synchronous reference frame error signal in (17) in terms of the stationary reference frame error signal

$$\varepsilon^{fl}[k] = \varepsilon[k]\mathrm{e}^{-\,\mathrm{j}\theta_l[k]} \tag{18}$$

results in

$$\begin{aligned} u_T[k] = &\sum_{l=1}^{x} b_{l,0}\ \varepsilon[k] + \sum_{l=1}^{x}\left(\sum_{i=1}^{n_l} b_{l,i}\ \varepsilon^{fl}[k-i]\right)\mathrm{e}^{\,\mathrm{j}\theta_l[k]} \\ &- \sum_{l=1}^{x}\left(\sum_{i=1}^{n_l} a_{l,i}\ u_l^{fl}[k-i]\right)\mathrm{e}^{\,\mathrm{j}\theta_l[k]} \end{aligned} \tag{19}$$

This expression contains both the total controller output and the present error signal in stationary reference frame.

Following the same thought process as in stationary reference frame, both the present voltage and error signals can be replaced by the saturated versions

$$\begin{aligned} u_{\mathrm{sat}} = &\sum_{l=1}^{x} b_{l,0}\ \varepsilon_{\mathrm{sat}} + \sum_{l=1}^{x}\left(\sum_{i=1}^{n_l} b_{l,i}\ \varepsilon^{fl}[k-i]\right)\mathrm{e}^{\,\mathrm{j}\theta_l[k]} \\ &- \sum_{l=1}^{x}\left(\sum_{i=1}^{n_l} a_{l,i}\ u_l^{fl}[k-i]\right)\mathrm{e}^{\,\mathrm{j}\theta_l[k]} \end{aligned} \tag{20}$$

By subtracting (19) from (20), and after clearing $\varepsilon_{\mathrm{sat}}$, equation (13) is again obtained. Therefore, there is no difference in the calculation of the realizable error signal between the implementation in stationary or multiple reference frames. However, a final step is required in this case to provide the realizable error signal in each of the multiple reference frames

$$\varepsilon_{\mathrm{sat}}^{fl} = \varepsilon_{\mathrm{sat}}\ \mathrm{e}^{-\,\mathrm{j}\theta_l[k]} \text{ for } l = 1, 2, ..., x \tag{21}$$

The saturation voltage corresponding to each controller in the parallel structure can be then calculated similarly to the stationary reference frame case

$$u_{l\_\mathrm{sat}}^{fl} = u_l^{fl}[k] + b_{l,0}\left(\varepsilon_{\mathrm{sat}}^{fl} - \varepsilon^{fl}[k]\right) \text{ for } l = 1, 2, ..., x \tag{22}$$

E. Controllers with different number of poles and zeroes

As stated, the former expressions assume each controller discrete-time transfer function has the same number of poles and zeroes. Note this does not mean all the controllers in the parallel structure must have the same number of poles, it means that all the controller outputs are updated with the error value at the present instant. However, similar results can be obtained if the controllers have a different number of poles than zeroes while all of them have the same pole/zero difference:

$$n_1 - m_1 = n_2 - m_2 = \cdots = n_x - m_x \tag{23}$$

where m_l are the number of zeroes of controllers $l = 1, 2, ..., x$. This means that all the controllers are updated with the same previous instant error value. Otherwise, a more complex and unpractical saturation scheme should be derived, in case the different controllers were updated with the error at different time instants. Although mathematically possible, this situation will not occur in practice.

III. Saturation strategies

The previous section has demonstrated the realizable reference anti-windup technique can be easily implemented in the case of parallel controllers independently of the reference frame. This technique ensures a fast transition from saturated to non-saturated state. However, this does not imply correct harmonic compensation or fundamental component realization during the saturated state. As it was described in the introduction, several researchers [13], [16]–[21], [24], [25] have dealt with the problem of the voltage command adaptation during saturation. The use of the realizable reference technique will further simplify the introduction of compensation mechanisms but the fundamental component production and the harmonic distortion will depend on the selection of the saturated complex vector. As it was seen in Fig. 1, multiple saturation options exist when the controller output magnitude exceeds the hexagon limits. In the case of parallel controllers, an increased number of options exist. Fig. 4 shows the options analyzed in this paper. It is considered that four parallel controllers would provide four voltage commands to exemplify the different analyzed options. The controllers are sorted (and numbered) in order of importance regarding fundamental component production and harmonic compensation, being u_1 the fundamental component.

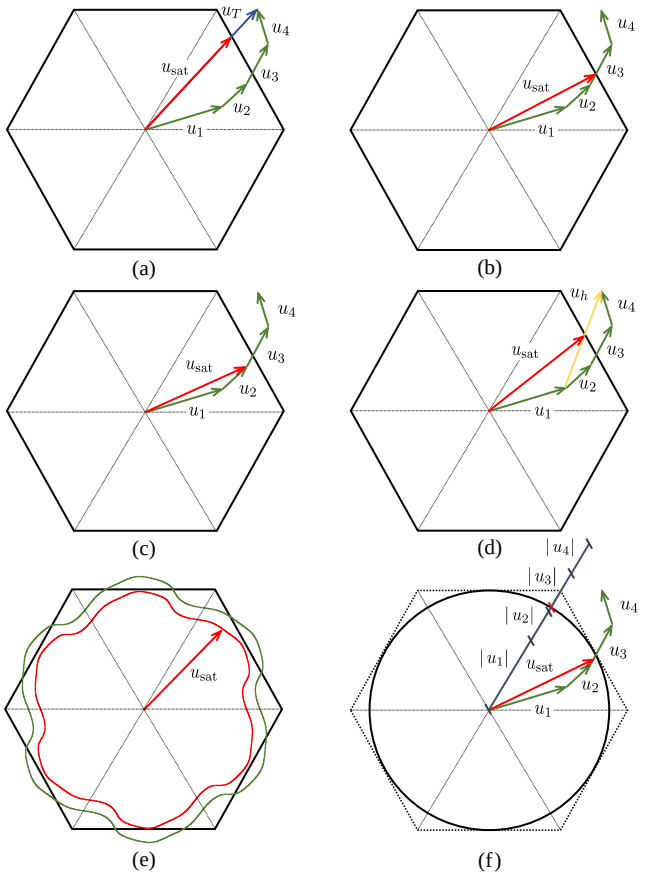

Fig. 4. Saturation options analyzed: (a) Global. (b) Incremental-1. (c) Incremental-2. (d) Group (proposed method). (e) Trajectory. (f) Magnitude.

Fig. 4(a) shows the first option that will be termed Global in this discussion. In this case, the resulting vector addition of the parallel controllers is compared with the hexagon limits. Since the magnitude exceeds the limits, the output voltage will be limited to the hexagon but keeping the original angle. This can be also applied using the inscribed circle limits for simpler implementation and lower harmonic distortion, but worse voltage utilization.

Fig. 4(b) shows another option, termed Incremental-1, in which the saturated voltage is calculated from the first component crossing the hexagon (or circle) limit. The remaining voltage components are disregarded. A modified version is shown in Fig. 4(c), termed Incremental-2. The same idea applies, but the saturated vector is calculated also rejecting the component crossing the hexagon (or circle) limit.

A fourth approach can be seen in Fig. 4(d), called Group. The different components are grouped in two: the fundamental u_1 and the addition of the remaining voltage vectors u_h. A similar saturation technique to that described for Fig. 4(b) is then applied. An optimal version of this method is proposed in [24] where an algorithm decides each instant the weighting for the harmonic reduction. However, its complexity makes it difficult for grid-forming applications where several harmonics are compensated and the load type is subject to change. The Group approach is also found in [16], where an optimized approach is also presented. The main drawback is that efficient implementation is restricted to the voltage circle limit.

Once the saturated vector is calculated following one of the described methods, no special treatment must be done to the controllers which outputs are disregarded, since the back-calculation method described in the previous section will automatically disable them in practice. It is also noted that the voltage vector is checked at every control step and no action is taken if the voltage is within limits.

The above-described methods provide an instantaneous voltage command at each modulation step but can increase the harmonic distortion due to the clipping of the voltage trajectory to the hexagon or voltage limits during saturation. Trajectory-based methods adapt the current commands to force the current controllers to produce voltage command outputs within the voltage limits in the whole fundamental voltage trajectory. In [13], [19] the harmonic controllers are progressively disabled when saturation is detected to make the voltage trajectory fit in the limits. Researchers have also proposed "distortion-free" saturators where the voltage trajectory is adapted to be contained within the voltage limits with no harmonic distortion. An example can be seen in Fig. 4(e) where all the components have been proportionally reduced to fit in the hexagon limits. This solution has been proposed in [17], [18] for the inscribed circle limit and in [20]–[22], [25] using the hexagon. The disadvantage of these methods is the increased complexity and lesser voltage utilization compared with the above-described methods. They are well suited for low-harmonic distortion current injection in grid supporting applications but could not be advisable in grid forming applications, where the magnitude of the fundamental voltage component is key. Moreover, they

still need a proper controller anti-windup method during the trajectory adaption. Therefore, they can be also benefited from the anti-windup implementation proposed in Section II.

The last approach, seen in Fig. 4(f), can be seen as a simpler but less voltage-efficient implementation of trajectory-based methods. In this case, the magnitudes of the voltage vector components coming from the current controllers are added and compared with the circle voltage limit. The magnitude of the first voltage component crossing the inner circle will be limited, and the higher-order or less important components disregarded. Another option is to proportionally reduce all components to resemble "distortion-free" methods. Both solutions theoretically eliminate voltage clipping during steady saturation. The first case will favor the fundamental component magnitude while the second a low THD. Due to both the relative angular position of the harmonic voltage components is not considered, and the circle is used as the voltage limit to make it simple, the voltage utilization will be poor. The phase of the voltage components can make the inverter voltage command to fit into the voltage limits along the whole voltage vector trajectory even in cases the sum of their magnitudes is beyond the limits. It is noted that this solution can still unnecessarily modify the trajectory in that case. This solution will be termed Magnitude for comparison.

IV. Comparison of Saturation Strategies

The distortion introduced by the different methods will depend both on the saturation level and the type of loads present in the system. A grid-forming scenario has been used to test the described alternatives. Fig. 5 shows a three-phase inverter with an output LC filter, an unbalanced three-phase linear load, and a non-linear load. The main system parameters can be found in Table I. The linear and non-linear loads draw about 40 % and 35 % of the rated power respectively.

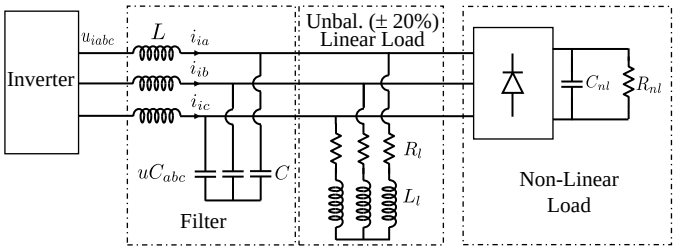

Fig. 5. Test system: Grid forming scenario including unbalanced and non-linear loads.

The inverter control goal is to obtain a balanced three-phase voltage at the filter output. The quality of this voltage will be used to benchmark the different methods. The typical grid-forming inverter control structure uses an outer voltage control loop controlling the capacitor voltage and an inner current control loop controlling the inverter currents. At steady state, the voltage controller will provide the adequate inverter current commands to achieve the desired voltage at the capacitors. To avoid the interaction of the voltage controllers in the analysis of the different saturation methods, the current commands at steady state will be pre-calculated and not modified. Otherwise, the voltage controllers would react during saturation modifying the current commands and making the analysis very complex. The interaction with the voltage controllers is beyond the paper scope.

TABLE I
SYSTEM PARAMETERS FOR ANALYSIS

Rated voltage	V_r	400 V_{rms}
Rated current	I_r	144 A_{rms}
Filter	L	260 µH
Filter	C	270 µF
Linear load	R_l	3.36 Ω
Linear load	L_l	6.6 mH
Linear load	Unbalance	±20%
Non-linear load	C_{nl}	1 mF
Non-linear load	R_{nl}	8.35 Ω

The necessary current to achieve the desired capacitor voltage can be easily calculated by replacing the inverter and the filter inductor L by an ideal three-phase source. Fig. 6(a) shows the current (i_{iqd}) needed to obtain the voltage trajectory at the filter capacitor (uC_{qd}) shown in Fig. 6(c). It is also possible to calculate the inverter voltage trajectory (u_{iqd}) to achieve both the inverter current and the capacitor voltage, as seen in Fig. 6(b).

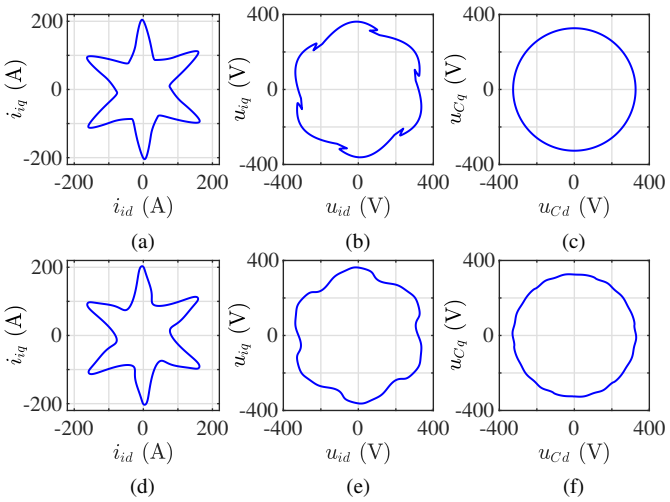

Fig. 6. Current and voltage trajectories for the system under test. (a),(d): Inverter current. (b),(e): Inverter voltage. (c),(f): Capacitor voltage. (a)-(c): Unlimited bandwidth. (d)-(f): Considering fundamental and six main harmonics.

An unrealistic bandwidth would be needed for the current controller to produce the trajectories seen in Fig. 6(a)-(c). Assuming a parallel controller structure composed of a fundamental current controller, a negative sequence current controller, and five harmonic controllers the modified trajectories seen in Fig. 6(d)-(f) are considered. They include the fundamental voltage at 50 Hz and harmonics at -250, 350, -50, -550, 650, -850 Hz in decreasing order of magnitude. The resulting capacitor voltage shown in Fig. 6(f) has a small

complex vector THD of 0.74 % and a magnitude error of -0.01 %. The magnitude error is defined as the difference between the magnitude of the fundamental component (i.e. 50 Hz component) of the capacitor voltage complex vector in steady-state and the magnitude of the capacitor voltage command (i.e. ideal voltage) complex vector [see Fig. 6(c)] . The magnitude of the fundamental component is obtained by performing the Fast Fourier Transform (FFT) to the capacitor voltage complex vector. If only the fundamental component of the inverter voltage seen in Fig. 6(b) were injected, the THD would be 6.85 %, the magnitude error -0.1 %, and the phase-voltage unbalance 0.58 %.

If voltage saturation occurs, the previous trajectories will be distorted. The following discussion will analyze the resulting capacitor voltage trajectory when the different methods described in the previous section are used. First, open-loop analysis using the voltage trajectory seen in Fig. 6(e) will be carried out. This avoids the interaction on the current controller and the time to recover from saturation to better understand the different saturation options. Later, closed-loop current control will be enabled to analyze the interaction of the current controller and the validity of the proposed realizable reference implementation, described in Section II. Three levels of saturation are imposed assuming dc-link voltages of 600, 570, and 540 V. The corresponding hexagon limits can be seen in Fig. 7.

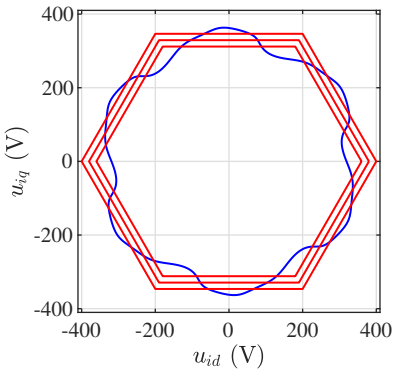

Fig. 7. Non-saturated inverter voltage trajectory (blue) and hexagon voltage limits (600, 570, 540 V).

A. Open-loop analysis

The different saturation strategies described in Section III are analyzed in simulation. The simulations have been carried out using the Specialized Power Systems library of the Matlab/Simulink Simscape Electrical toolbox. The control routines have been coded in C language. The inverter shown in Fig. 5 is simplified by using a linear voltage source to speed up the simulations. The voltage trajectory in Fig. 7 is the inverter voltage command before saturation. The measured capacitor voltage THD, fundamental voltage magnitude error, the fundamental voltage phase angle and the phase unbalance are taken as figures of merit for the different methods. The phase angle is given with respect to the non-saturated capacitor voltage, whose trajectory is seen in Fig. 6(f). The phase unbalance is calculated as the difference between the fundamental peak of the highest and smallest phase voltages normalized by the mean phase voltage.

Table II summarizes the obtained results. Focusing first in the direct saturation methods, it can be seen that the Group strategy [see Fig. 4(d)] gives both low THD and magnitude error. The Global strategy [see Fig. 4(a)] offers the second-best results for THD and magnitude errors, and the best for angle phase distortion and unbalance; moreover, it has the benefit of being the simplest for computer implementation. The Incremental strategies [see Fig. 4(b,c)] do not provide good results; this, in addition to their increased complexity, discards them for the closed-loop analysis. All methods have been tested using both the hexagon and circle limits. As expected, a better THD is obtained in all cases with the circle limit, but at the cost of a higher magnitude error and unbalance.

Voltage trajectories fitting the hexagon limit were synthesized from the original trajectory with three different strategies: decreasing the overall voltage (Global), canceling harmonics until the trajectory fits in the hexagon (Incremental-1 and 2), and reducing first the grouped harmonic components (Group). As can be seen in Table II the Trajectory Global strategy preserves the original (i.e. unsaturated) THD, but the magnitude error is larger than in other methods. The small voltage margin left by the fundamental component makes the other two trajectory strategies to have worse THD than non-trajectory methods. The advantage of both the Trajectory Group and the Trajectory Incremental strategies over the Trajectory Global Strategy is that they better preserve the fundamental magnitude under light saturation and the fundamental voltage phase under deep saturation. It must be remarked that these are best-case results trying to resemble the behavior of trajectory-based methods. In practice, tracking the feasible trajectory is not straightforward and worse results should be expected. The preservation of THD shown by the Trajectory Global method makes this strategy ideal for grid supporting applications, but grid forming applications require both harmonic quality and preservation of the fundamental voltage. A weighting algorithm could be implemented to trade-off THD and fundamental voltage reduction. However, that is far beyond the scope of this paper.

The Magnitude strategy [see Fig. 4(e)], shows similar results to trajectory-based methods. However, in the case of the Global strategy, the worst voltage utilization by both using the circle limit and neglecting the component phases, makes the fundamental magnitude error to be significantly higher.

B. Closed-loop analysis

The validity of the proposed anti-windup algorithm is analyzed in combination with some saturation strategies selected from the previous discussion. The Global and Group strategies are selected for their implementation simplicity and good results, respectively. The online adaptation of the current

TABLE II
CAPACITOR VOLTAGE DISTORTION USING DIFFERENT SATURATION STRATEGIES FOR OPEN-LOOP INVERTER VOLTAGE COMMAND.

	600 V				570 V				540 V			
Method	THD (%)	Mag. Error (%)	Angle (deg)	Unbal. (%)	THD (%)	Mag. Error (%)	Angle (deg)	Unbal. (%)	THD (%)	Mag. Error (%)	Angle (deg)	Unbal. (%)
Global (circle)	2.15	1.27	0	0.14	2.98	4.34	0	0.22	3.84	8.45	-0.01	0.29
Global (hexagon)	2.17	0.99	0	0.10	4.1	3.25	0.01	0.17	5.04	6.43	0	0.21
Incremental-1 (circle)	4.47	1.27	0.32	0.25	3.35	4.34	0.53	0.41	6.32	8.44	0.13	0.57
Incremental-1 (hexagon)	4.01	1.02	0.22	0.19	3.71	3.20	0.41	0.31	5.9	5.91	0.41	0.40
Incremental-2 (circle)	3.04	1.96	0.28	0.27	3.35	4.34	0.53	0.42	6.32	8.44	0.13	0.57
Incremental-2 (hexagon)	3.39	1.63	0.22	0.22	3.62	3.22	0.44	0.31	5.9	6.22	0.43	0.46
Group (circle)	1.87	1.26	0.25	0.21	2.59	4.57	0.57	0.42	2.54	10.06	0.61	0.58
Group (hexagon)	2.07	0.97	0.14	0.15	3.71	3.18	0.47	0.30	4.94	6.47	0.59	0.35
Trajectory Global	0.74	4.58	0	0	0.74	9.35	0	0	0.74	14.13	0	0
Trajectory Incremental	6.35	-0.07	-0.03	0.59	6.85	3.33	-0.03	0.55	6.85	8.42	-0.03	0.50
Trajectory Group	5.45	-0.07	-0.02	0.44	6.85	3.33	-0.03	0.55	6.85	8.42	-0.03	0.50
Magnitude Global	0.74	8.19	0	0	0.74	12.78	0	0	0.74	17.37	0	0
Magnitude Incremental	6.35	-0.07	-0.03	0.59	6.85	3.33	-0.03	0.59	6.85	8.42	-0.03	0.59

commands proposed by trajectory methods is beyond the scope of this paper and they have not been implemented.

The current trajectory shown in Fig. 6(d) is commanded to a current controller using a parallel structure (see Fig. 3) composed of seven complex vector PI controllers [31] for the fundamental, negative sequence, and main five harmonic components. Each controller is independently tuned in its reference frame. The measured capacitor voltage is used as a feedforward term for disturbance decoupling. This feedforward signal and the output of the fundamental current controller will be considered as the fundamental voltage component for the saturation strategy implementation. It is noted the feedforward term can also contain harmonic content during transients and also in steady-state if low harmonic distortion is not achieved.

The capacitor voltage THD using this controller and assuming no saturation is 1.03 %, the fundamental voltage component magnitude error is 0.1 %, and the phase unbalance 0.04 %. Linear sources are first used in the simulation to separate the effects of the current controller bandwidth and anti-windup method from the inverter non-linear behavior. When inverter voltage saturation is introduced the results shown in Table III are obtained. Slightly increased THD and magnitude distortion values compared to those obtained for the open-loop inverter voltage are obtained. This is explained by the bandwidth limitation of the controllers. Nevertheless, the comparative results are similar to the case of open-loop voltage injection meaning than the proposed anti-windup implementation is working as expected.

To prove the validity of the described anti-windup technique, the Group hexagon saturation strategy was also implemented without the proposed anti-windup algorithm in two cases. One, calculating the individual output voltages after saturation according to the given strategy (see "State saturation" in Table III); the second, limiting only the global controller output according to the same strategy but not calculating the individual outputs (see "No state saturation" in Table III). The results are worse than for the case in which the proposed anti-windup technique is enabled. However, the THD and magnitude error for the particular case of 540 V are better in the case of only applying state saturation. In this case, the distortion is mainly affecting the phase (i.e. angle error) of the fundamental voltage component.

The same simulations carried out to obtain the values of Table III were repeated with a three-phase switching inverter showing slightly increased THD values and magnitude error under low saturation (600 V), similar at 570 V, and slightly better under large saturation (540 V).

The transient response was also analyzed through simulation before the experimental verification. Fig. 8(b) shows the current commands before and after the realizable reference calculation. The Group saturation strategy is used. It is remarked the calculation of the realizable reference is not strictly required in the implementation, but it better explains the technique behavior. Both commands are the same before 0.5 s, since the controller output is not saturated. At t = 0.5 s, the dc-link voltage drops to 500 V (33 % drop) [see Fig. 8(a)]. At this moment, the realizable reference (continuous line) is calculated, differing from the non-saturated command (dotted line). The actual currents follow the realizable references as can be seen in Fig. 8(c). The realizable reference reaches steady state in 1 fundamental cycle, while the actual current needs around 2 cycles in this example. It is noted that the filter and load parameters for this simulation are the ones for the experimental setup, shown in Section V.

V. EXPERIMENTAL RESULTS

The experimental setup consists of an interleaving dc/dc converter and a grid-forming dc/ac converter manufactured by ELINSA. The dc/dc converter is intended to interface a $LiFePO_4$ battery pack, but in this work it is used to force dc-link voltage variations. An LC filter is used to smooth the output voltage to supply the loads, with the structure shown in Fig. 5. The experimental setup can be seen in Fig. 9. The converter control stage is based on a Texas Instruments TMS320F28335 digital signal controller board. The dc/ac converter switching and control frequency is 10 kHz.

The proposed realizable reference anti-windup implementation along with the Group saturation strategy was experimentally tested. Due to laboratory power constraints, the inverter LC filter and the load shown in Table I were resized to the values shown in Table IV to allow voltage saturation within the lab current limit. The linear load absorbs 41 % of the rated power and the non-linear load around 32 %.

The current controller can be seen in Fig. 10. The controller is composed of eight complex vector PI controllers for the fundamental, dc component, negative sequence, and the main

TABLE III

CAPACITOR VOLTAGE DISTORTION USING DIFFERENT SATURATION STRATEGIES FOR CLOSED-LOOP INVERTER CURRENT INJECTION.

	600 V				570 V				540 V			
Method	THD (%)	Mag. Error (%)	Angle (deg)	Unbal. (%)	THD (%)	Mag. Error (%)	Angle (deg)	Unbal. (%)	THD (%)	Mag. Error (%)	Angle (deg)	Unbal. (%)
Global (circle)	2.99	2.16	-0.17	0.52	5.84	6.8	-1.1	0.8	7.75	11.18	-2.38	1.17
Global (hexagon)	3	1.54	-0.03	0.56	6.28	6.24	-0.53	1.08	9.46	10.81	-1.51	1.52
Group (circle)	1.99	2	0.95	0.54	4.30	6.24	0.94	1.10	7.50	10.39	-0.62	0.79
Group (hexagon)	2.21	1.48	0.669	0.4	4.2	5.2	2.16	0.84	6.32	9.26	2.47	0.97
State saturation	6.09	0.02	-2.87	0.52	7.25	4.53	-4.58	3.43	5.78	8.78	-5.71	1.39
No state saturation	8.30	-6.73	-3.34	1.16	9.78	0.48	-0.64	1.18		Unstable		

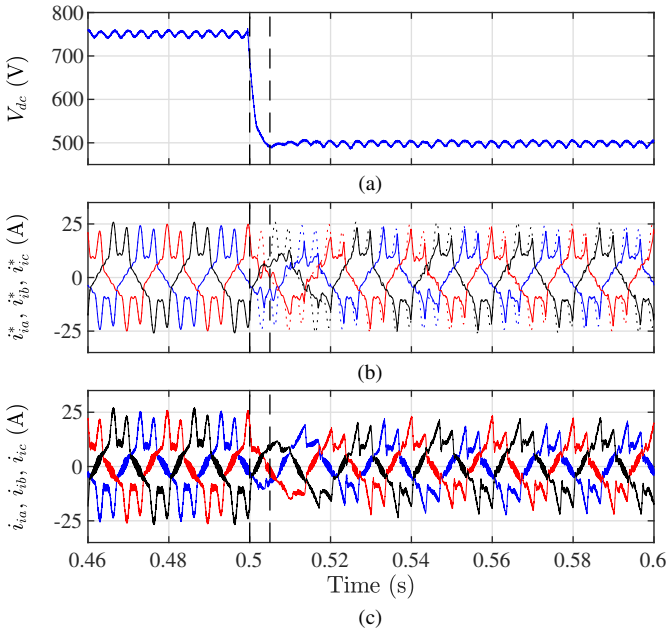

Fig. 8. Simulation. Realizable reference anti-windup transient performance. (a) dc-link voltage (750 V $\rightarrow$ 500 V); (b) Ideal (dotted line) and realizable (continuous line) references for the three-phase currents; (c) Three-phase inverter currents.

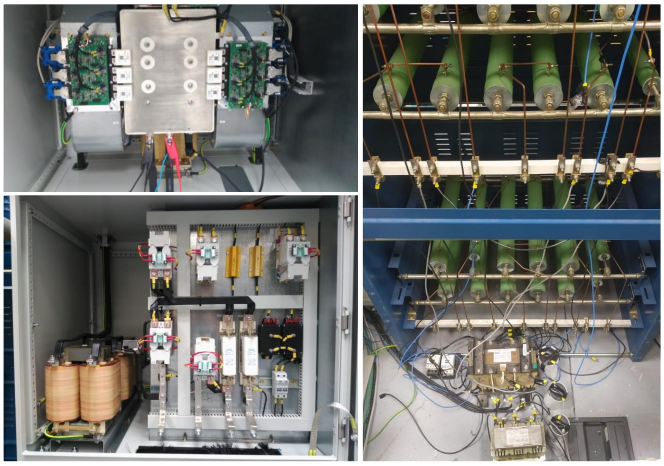

Fig. 9. Experimental setup. Top left: dc/dc and dc/ac power converters. Bottom left: Output filter. Right: Connected loads.

five harmonic components(-250, 350, -550, 650, and 950 Hz). As in simulation, each controller is independently tuned in its reference frame. The measured capacitor voltage (u_{Cqd}) is used as a feedforward signal for disturbance decoupling. The inverter non-idealities may result in the injection of small dc voltage and current components in the ac output [32], [33]. The capacitor voltage feedforward term of the current controller creates a positive feedback loop for the dc component giving rise to large dc offsets and even to controller output saturation. To avoid this, a dc component controller is added to the parallel structure. The sum of the feedforward signal and the fundamental and dc current controller outputs will be considered as the main voltage component for the Group saturation strategy.

TABLE IV

EXPERIMENTAL SYSTEM PARAMETERS

Rated voltage	V_r	400 V_{rms}
Rated current	I_r	16 A_{rms}
Filter	L	2 mH
Filter	C	16 µF
Linear load	R_l	35 Ω
Linear load	L_l	2.4 mH
Linear load	Unbalance	±25%
Non-linear load	C_{nl}	500 µF
Non-linear load	R_{nl}	106 Ω

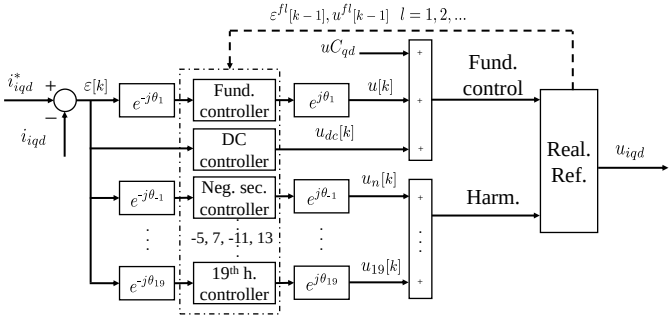

Fig. 10. Current controller including realizable reference anti-windup.

The measured inverter current, i_{iqd}, is compared with the current trajectory command, i_{iqd}^*, seen in Fig. 11(a). This trajectory is obtained in simulation using the experimental setup parameters as described in Section IV. Fig. 11(b) shows the corresponding theoretical non-saturated inverter voltage trajectory, and 11(c) the resulting capacitor voltage when the described harmonics are injected. This must be taken as the best output voltage trajectory achievable by the implemented controller structure. The THD in the capacitor voltage is

3.28 % due to the strong non-linear load selected. To decrease the THD below 1 %, five additional parallel harmonic controllers would be required. Compensation of those additional harmonics would require direct discrete-time design of the controllers [34] or delay compensation [35] which is out of the scope of this paper. However, the THD is still below 8 %, which is the limit recommended by the IEEE Standard 519-2014 [4] for voltages below 1000 V. The resulting voltage u_{iqd} from the control loop, after proper saturation, is commanded to the inverter using SVM.

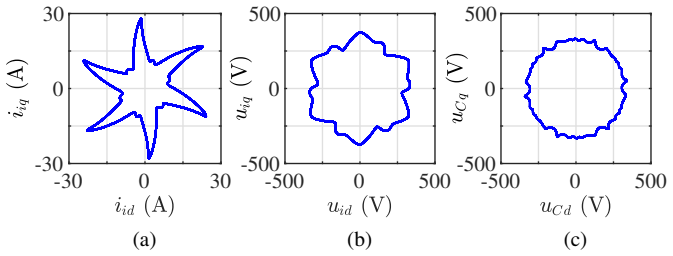

Fig. 11. Current commands and predicted voltage trajectories for the experimental system. (a) Inverter current. (b) Inverter voltage. (c) Capacitor voltage.

The realizable reference block (Real. Ref. in Fig. 10) is computed according to the flow diagram shown in Fig. 12. The function receives the present period controller error and outputs (i.e. voltage commands). According to the voltage limit selected, circle or hexagon, the maximum voltage available is calculated. This step is straightforward in the case of the circle limit, but it needs some computation time in case of the hexagon. Once the limit is obtained, a magnitude comparison is done with the actual voltage command. Nothing is done if the voltage command does not exceed the limit. On the contrary, a voltage command replacement must be selected according to the trajectories described in Section III. Then, only by computing the equations in the blocks of Fig. 12 labeled as 'Realizable reference anti-windup', the anti-windup algorithm is performed.

The execution times of this algorithm using the 32-bit 150 MHz TMS320F28335 microcontroller are given in Table V for the controller structure used in this experimental section (8 parallel controllers) and adding five additional harmonic controllers. The hexagon limit and the Group strategy are implemented. It is also included the time to compute the controllers, not included in the flow diagram of Fig. 12. It can be seen that the most demanding part of the algorithm is the calculation of the saturated voltage, but it is still affordable for medium performance microcontrollers. Circle limit strategies reduce this time. It is noted the total time in the table does not include additional functions as AD converters reading, SVM, or protection functions.

Fig. 13 shows the trajectory of the actual non-saturated inverter voltage command when the current trajectory seen in Fig. 11(a) is commanded. The differences with the theoretical trajectory shown in Fig. 11(b) are due to the inverter non-

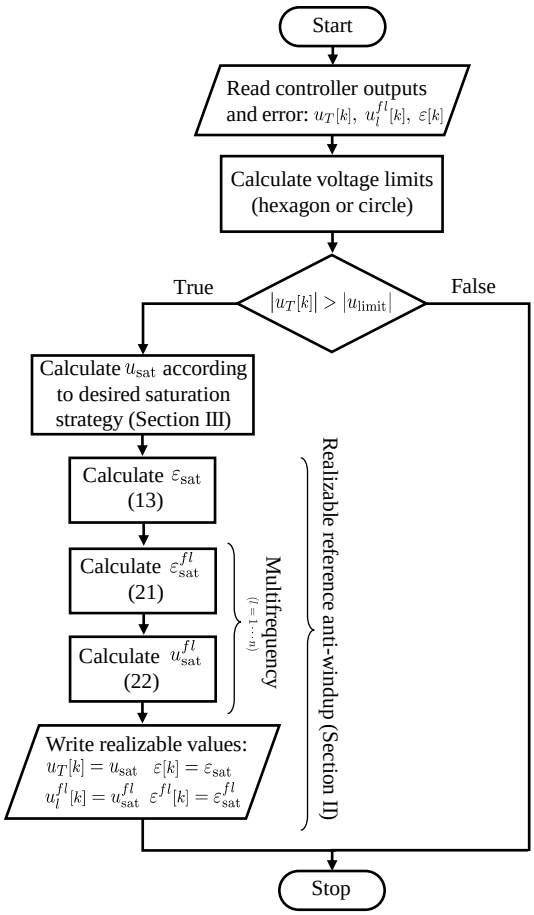

Fig. 12. Flow diagram of the implementation of the proposed anti-windup algorithm.

TABLE V
COMPUTATION TIME OF THE PROPOSED METHOD

	8 controllers	13 controllers
Controllers	5.5 µs	8.4 µs
Hexagon limit	0.8 µs	0.8 µs
Group (hexagon)	5.3 µs	7.8 µs
Realizable reference anti-windup	0.6 µs	1 µs
Total (w/o. controllers)	6.7 µs	9.6 µs
Total (w. controllers)	12.2 µs	18 µs

idealities. Voltage hexagon limits for dc-link voltages of 750, 570 and 500 V are also shown in Fig. 13. While a 750 V dc-link voltage ensures non-saturated operation, both 570 and 500 V impose increasing levels of saturation. These dc-link voltage levels will be used to test the proposed method performance.

Fig. 14 compares the behavior of the proposed realizable reference (RR) method versus a simple state saturation (SS). In the latter case, when the controller output exceeds the voltage hexagon limits, it is also limited following the Group strategy and the corresponding individual controller outputs are calculated, but the realizable reference (i.e. error) is not computed. This prevents from windup [28], [29] but does not ensure a bumpless transition from the saturated to the non-

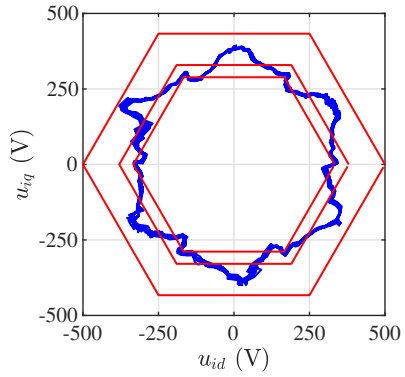

Fig. 13. Experimental non-saturated inverter voltage trajectory and voltage hexagon limits under test: 500, 570, and 750 V.

saturated state.

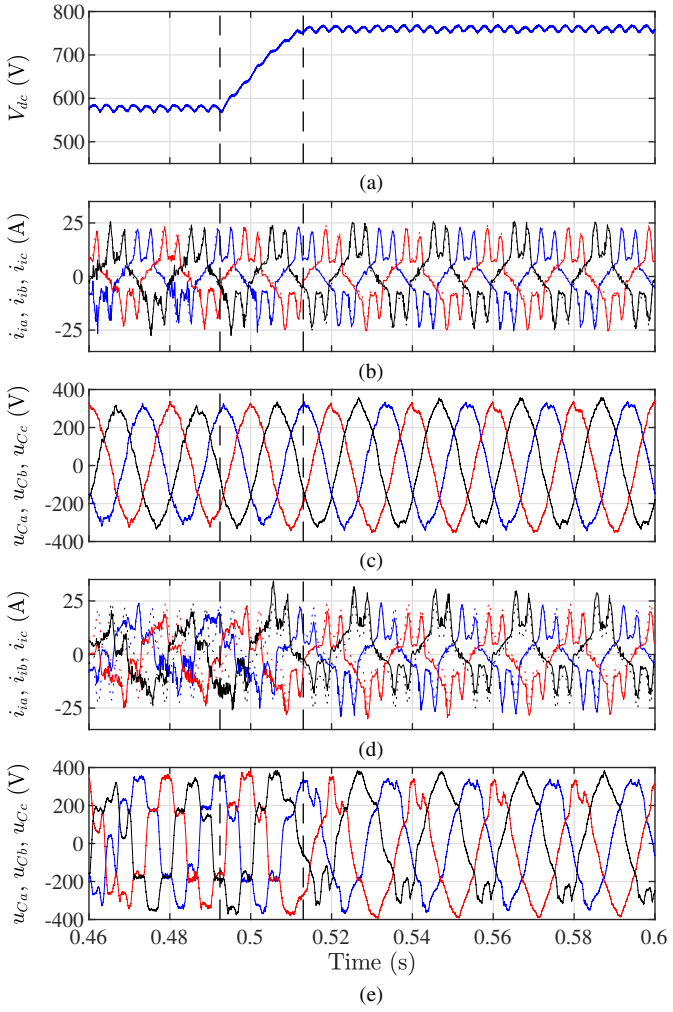

Fig. 14. Experimental. Realizable reference and state-saturation anti-windup performance during saturation and transition to non-saturated state. (a): dc-link voltage (570 V $\rightarrow$ 750 V). (b)-(d): Phase currents (solid line) and current commands (dashed line). (c)-(e): Capacitor voltages. (b)-(c): Realizable reference. (d)-(e): State saturation. Blue: phase-a; red: phase-b; black: phase-c.

Fig. 14(a) shows a dc-link voltage transition from 570 V to 750 V. Fig. 14(b,d) show the inverter output current commands and actual phase currents. It can be observed that the current during saturation cannot accurately follow the command, but the distortion is small for RR, while in the case of SS there is noticeable distortion. Moreover, when the dc-link voltage is restored, the RR algorithm ensures a fast transition to the correct signal tracking (less than 1 fundamental cycle). SS transition is slower, needing 7 fundamental cycles for complete recovery (not shown in the graph). The current command tracking also impacts the output voltage waveform. The output voltage can be seen in Fig. 14(c,e). In the case of RR, the distortion is low during voltage saturation, while a greatly distorted signal is seen for SS. Table VI summarizes THD and fundamental component magnitude error for different dc-link levels analyzed. It must be noted that the THD in the non-saturated case is higher in the experimental results compared with simulation, due to the non-linearities of the real setup and the scaled-down load. A higher dc-link voltage is also needed to avoid saturation. However, the distortion increment during saturation aligns with the results obtained in simulation (Table III).

TABLE VI
EXPERIMENTAL CAPACITOR VOLTAGE DISTORTION USING REALIZABLE REFERENCE (RR) AND STATE SATURATION (SS)

Vdc (V)	Method	THD (%)	Magnitude error (%)
750	RR	3.15	0
	SS	3.15	0
570	RR	3.96	8.6
	SS	19.84	8.35
500	RR	4.93	17.46
	SS	-	-

A deeper saturation situation is shown in Fig. 15. In this case, the converter is initially operated with 500 V of dc-link voltage. This deep saturation level makes SS inoperative, making the system unstable and, therefore, it is not shown. RR can keep a low distortion in the current tracking, as can be seen in Fig. 15(b). This allows to keep a low harmonic distortion in the capacitor voltage during saturation, as seen in Fig. 15(c) and Table VI. However, the large saturation level unavoidably decreases the fundamental component magnitude. Again, once the voltage is restored a fast transition to regular operation is achieved.

The performance of the anti-windup method when the controller enters into saturation can be seen in Fig. 16. Once the dc-link voltage is decreased to 570 V (24 % drop) the currents start following the realizable references instead of the ideal command [Fig. 16(b)]. Despite the large voltage change the currents reach steady state in less than 3 fundamental cycles (t $\approx$ 0.55 s) as well as the capacitor voltages [Fig. 16(c)].

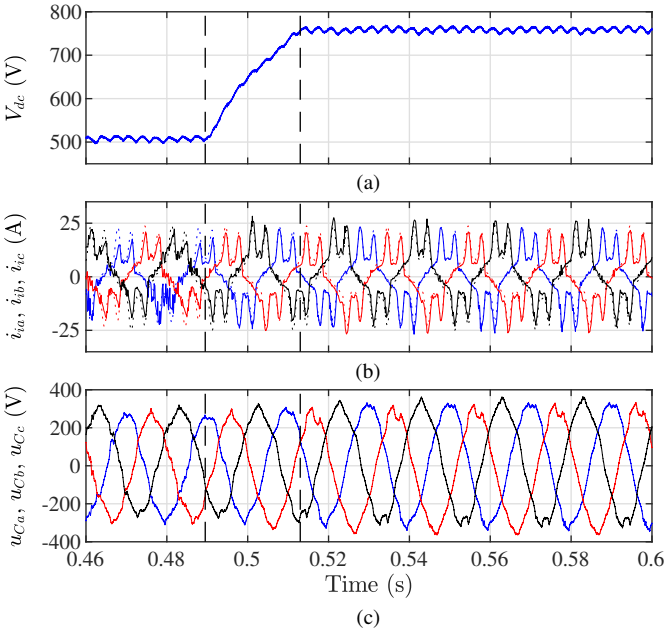

Fig. 15. Experimental. Realizable reference anti-windup performance during saturation and transition to non-saturated state. (a): dc-link voltage (500 V→750 V). (b): Phase currents (solid line) and current commands (dashed line). (c): Capacitor voltages. Blue: phase-a; red: phase-b; black: phase-c.

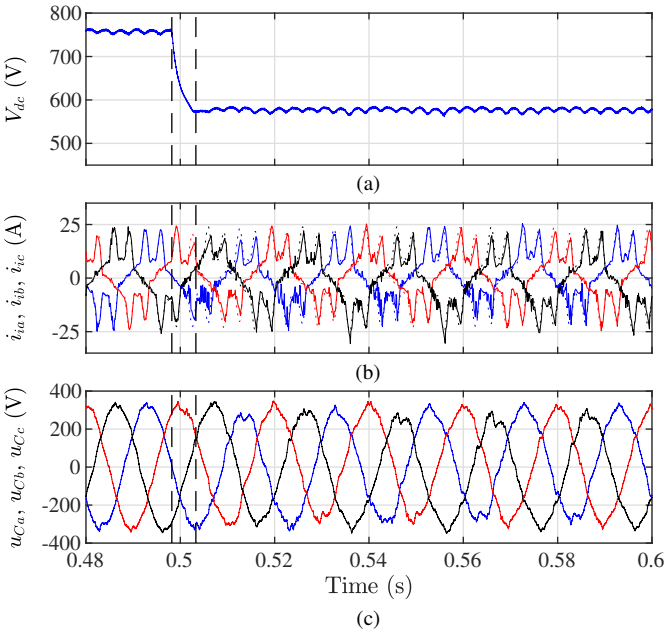

Fig. 16. Experimental. Realizable reference anti-windup performance entering in saturation. (a): dc-link voltage (750 V→570 V). (b): Phase currents (solid line) and current commands (dashed line). (c): Capacitor voltages. Blue: phase-a; red: phase-b; black: phase-c.

VI. Conclusions

This paper develops and demonstrates a simple way of implementing the realizable reference anti-windup technique for parallel controllers in multiple reference frames. The proposed implementation allows to use any kind of controller and, if required, seamless modification of single controller outputs during saturation. The proposed anti-windup technique can be applied to any parallel linear controller structure, regardless of the variables being controlled. However, the choice of the saturated value will depend on the application.

Different saturation options are available and can be easily applied if this technique is used for current controllers. The selection will depend on the final application (e.g. grid support, grid form, etc.). Grouping the harmonic controller outputs shows excellent results for the inner-loop current controllers in grid-forming applications. Simulation and experimental results demonstrate the feasibility and performance of the proposed anti-windup implementation in the current controllers of grid-forming inverters, even under deep dc-link voltage drop.

References

[1] F. Blaabjerg, R. Teodorescu, M. Liserre, and A. V. Timbus, "Overview of Control and Grid Synchronization for Distributed Power Generation Systems," *IEEE Transactions on Industrial Electronics*, vol. 53, no. 5, pp. 1398–1409, Oct. 2006.

[2] A. Hirsch, Y. Parag, and J. Guerrero, "Microgrids: A review of technologies, key drivers, and outstanding issues," *Renewable and Sustainable Energy Reviews*, vol. 90, pp. 402–411, Jul. 2018.

[3] C. Blanco, D. Reigosa, J. C. Vasquez, J. M. Guerrero, and F. Briz, "Virtual Admittance Loop for Voltage Harmonic Compensation in Microgrids," *IEEE Transactions on Industry Applications*, vol. 52, no. 4, pp. 3348–3356, Jul. 2016.

[4] "IEEE Recommended Practice and Requirements for Harmonic Control in Electric Power Systems," *IEEE Std 519-2014 (Revision of IEEE Std 519-1992)*, pp. 1–29, Jun. 2014.

[5] M. El-Habrouk, M. Darwish, and P. Mehta, "Active power filters: a review," *IEE Proceedings - Electric Power Applications*, vol. 147, no. 5, pp. 403–413, Sep. 2000.

[6] Y. W. Li and J. He, "Distribution System Harmonic Compensation Methods: An Overview of DG-Interfacing Inverters," *IEEE Industrial Electronics Magazine*, vol. 8, no. 4, pp. 18–31, Dec. 2014.

[7] R. Teodorescu, F. Blaabjerg, M. Liserre, and P. C. Loh, "Proportional-resonant controllers and filters for grid-connected voltage-source converters," *IEE Proceedings - Electric Power Applications*, vol. 153, no. 5, pp. 750–762, Sep. 2006.

[8] M. J. Newman, D. N. Zmood, and D. G. Holmes, "Stationary frame harmonic reference generation for active filter systems," *IEEE Transactions on Industry Applications*, vol. 38, no. 6, pp. 1591–1599, Nov./Dec. 2002.

[9] P. Mattavelli, "A closed-loop selective harmonic compensation for active filters," *IEEE Transactions on Industry Applications*, vol. 37, no. 1, pp. 81–89, Jan./Feb. 2001.

[10] ——, "Synchronous-frame harmonic control for high-performance AC power supplies," *IEEE Transactions on Industry Applications*, vol. 37, no. 3, pp. 864–872, May/Jun. 2001.

[11] T. C. Y. Wang and X. Yuan, "Design of multiple-reference-frame PI controller for power converters," *in 2004 IEEE 35th Annual Power Electronics Specialists Conference (IEEE Cat. No.04CH37551)*, vol. 5, pp. 3331–3335, Jun. 2004.

[12] I. J. Gabe, F. F., K. Palha, and H. Pinheiro, "Grid connected voltage source inverter control during voltage dips," *in 35th Annual Conference of IEEE Industrial Electronics*, pp. 4571–4576, Nov. 2009.

[13] M. Ochoa-Gimenez, S. D'Arco, and J. A. Suul, "Voltage saturation anti-windup for harmonic controllers in multiple reference frames," *in 2015 IEEE International Conference on Industrial Technology (ICIT)*, pp. 2139–2144, Mar. 2015.

[14] B. P. McGrath and D. G. Holmes, "Anti-windup control for stationary frame current regulators using digital conditioning architectures," *in 2017 IEEE Energy Conversion Congress and Exposition (ECCE)*, pp. 5744–5751, Oct. 2017.

[15] B. P. McGrath, D. G. Holmes, and L. McNabb, "A Signal Conditioning Antiwindup Approach for Digital Stationary Frame Current Regulators," *IEEE Transactions on Industry Applications*, vol. 55, no. 6, pp. 6036–6046, Nov. 2019.

[16] A. Amerise, M. Mengoni, G. Rizzoli, L. Zarri, A. Tani, and D. Casadei, "Comparison of three voltage saturation algorithms in shunt active power filters with selective harmonic control," *IEEE Transactions on Industry Applications*, vol. 56, no. 3, pp. 2762–2772, May 2020.

[17] M. Rizo, A. Rodríguez, F. J. Rodríguez, E. Bueno, and M. Liserre, "Different approaches of stationary reference frames saturators," *in IECON 2012 - 38th Annual Conference on IEEE Industrial Electronics Society*, pp. 2245–2250, Oct. 2012.

[18] M. Rizo, M. Liserre, E. J. Bueno, F. J. Rodríguez, and A. Rodríguez, "Distortion-Free Saturators for Power Converters Under Unbalanced Conditions," *IEEE Transactions on Power Electronics*, vol. 30, no. 6, pp. 3364–3375, Jun. 2015.

[19] L. Harnefors, A. G. Yepes, A. Vidal, and J. Doval-Gandoy, "Reduction of saturation-induced distortion and antiwindup in multifrequency current control," *in 2015 17th European Conference on Power Electronics and Applications (EPE'15 ECCE-Europe)*, pp. 1–7, Sep. 2015.

[20] ——, "Multifrequency Current Control With Distortion-Free Saturation," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 4, no. 1, pp. 37–43, Mar. 2016.

[21] A. G. Yepes, J. Doval-Gandoy, and H. A. Toliyat, "Multifrequency Current Control Including Distortion-Free Saturation and Antiwindup With Enhanced Dynamics," *IEEE Transactions on Power Electronics*, vol. 33, no. 9, pp. 7309–7313, Sep. 2018.

[22] ——, "Multifrequency Current Control for n-Phase Machines Including Antiwindup and Distortion-Free Saturation With Full DC-Bus Utilization," *IEEE Transactions on Power Electronics*, vol. 34, no. 10, pp. 9891–9905, Oct. 2019.

[23] A. G. Yepes and J. Doval-Gandoy, "Effective current limitation for multifrequency current control with distortion-free voltage saturation and antiwindup," *IEEE Transactions on Power Electronics*, vol. 35, no. 12, pp. 13 697–13 713, 2020.

[24] J. Karttunen, S. Kallio, J. Honkanen, P. Peltoniemi, and P. Silventoinen, "Partial Current Harmonic Compensation in Dual Three-Phase PMSMs Considering the Limited Available Voltage," *IEEE Transactions on Industrial Electronics*, vol. 64, no. 2, pp. 1038–1048, Feb. 2017.

[25] J. Moriano, M. Rizo, E. Bueno, J. R. Sendra, and R. Mateos, "Distortion-Free Instantaneous Multifrequency Saturator for THD Current Reduction," *IEEE Transactions on Industrial Electronics*, vol. 66, no. 7, pp. 5310–5320, Jul. 2019.

[26] J. Serrano, J. Moriano, M. Rizo, and F. J. Dongil, "Enhanced current reference calculation to avoid harmonic active power oscillations," *Energies*, vol. 12, no. 21, Oct. 2019.

[27] J. M. Guerrero, C. González-Moral, D. Fernández, D. Reigosa, C. Rivas, and F. Briz, "Realizable References Anti-Windup Implementation for Parallel Controllers in Multiple Reference Frames," in *2018 IEEE Energy Conversion Congress and Exposition (ECCE)*, Sep. 2018, pp. 3142–3149.

[28] Y. Peng, D. Vrancic, and R. Hanus, "Anti-windup, bumpless, and conditioned transfer techniques for PID controllers," *IEEE Control Systems Magazine*, vol. 16, no. 4, pp. 48–57, Aug. 1996.

[29] J. M. Guerrero, F. Briz, A. Diez, and J. C. Alvarez, "Design and tuning of PI velocity regulators for high performance AC drives," *IFAC Workshop on Digital Control - Past, Present and Future of PID Control (PID 00)*, vol. 33, pp. 101–106, April 2000.

[30] K. Ogata, *"Discrete-Time Control Systems," 2^{nd} edition*. Prentice Hall, 1995.

[31] F. B. d. Blanco, M. W. Degner, and R. D. Lorenz, "Dynamic analysis of current regulators for AC motors using complex vectors," *IEEE Transactions on Industry Applications*, vol. 35, no. 6, pp. 1424–1432, Nov./Dec. 1999.

[32] B. Long, M. Zhang, Y. Liao, L. Huang, and K. T. Chong, "An overview of DC component generation, detection and suppression for grid-connected converter systems," *IEEE Access*, vol. 7, pp. 110 426–110 438, Aug. 2019.

[33] V. Salas, E. Olias, M. Alonso, F. Chenlo, and A. Barrado, "DC current injection into the network from PV grid inverters," *in 2006 IEEE 4th World Conference on Photovoltaic Energy Conference*, pp. 2371–2374, May 2006.

[34] H. Kim, M. W. Degner, J. M. Guerrero, F. Briz, and R. D. Lorenz, "Discrete-time current regulator design for AC machine drives," *IEEE Transactions on Industry Applications*, vol. 46, no. 4, pp. 1425–1435, July 2010.

[35] A. G. Yepes, F. D. Freijedo, J. Doval-Gandoy, López, J. Malvar, and P. Fernandez-Comesaña, "Effects of discretization methods on the performance of resonant controllers," *IEEE Transactions on Power Electronics*, vol. 25, no. 7, pp. 1692–1712, July 2010.