Characterization of GaN HEMT Transistors for DC/DC Converters in Transportation Applications

Rand AL Mdanat[†], Ramy Georgious[† ‡], Jorge Garcia[†], Giulio De Donato[§] Fabio Giulii Capponi[§],
[†] Lemur Research Group, Electrical Engineering Dept., University of Oviedo, Gijon, Spain
[‡] Electrical Engineering Dept., University of Port Said, Port Said, Egypt
[§] DIAEE, University of Rome-La Sapienza, Roma, Italy

***Abstract*—The motivation of this work is the characterization of semiconductor switches in DC/DC Wide Band-Gap based converters for electrical vehicle applications. The paper studies Gallium Nitride High Electron Mobility (GaN HEMT) Transistors, which present very good features for high-frequency high-efficiency applications. In order to obtain an efficient DC/DC converter design, a full characterization of these devices must be carried out. A double pulse test is applied to the GaN device, in order to study the switching behavior of these transistors. The test will be performed experimentally and in simulation under different operating conditions, in order to have the ability to understand the difference in the transistor behavior under these different operating points. Finally, the obtained results will be presented, commented and compared to identify the particularities of these devices.**

***Index Terms*—Electric vehicle, DC/DC converters, Gallium Nitride, double pulse test**

I. Introduction

Power electronics technology is the cornerstone of the whole concept of developing environmental-friendly vehicles [1], [2].The importance of the converters in EV is reflected by their role as an interface between the elements in the electric power train and the energy storage systems, which adapt the power to the different voltage levels. Due to the constraints of automotive applications, the power electronics system must be reliable, efficient, and present high power density. Nevertheless achieving these constraints is still a challenge [1], [4]–[6].

In order to improve the efficiency of a power converter, the power switching device needs to be chosen carefully to ensure low switching and conduction losses [7], [8]. In general, silicon (Si) has been the basic and dominant material for the last half-century. However, the operating limitations of such devices might avoid its use in future applications [9]–[11].

Wide bandgap (WBG) semiconductors such as Silicon Carbide (SiC) and Gallium Nitride (GaN), are defined by their larger bandgap compared to Si [12], [13]. In comparison with Si, WBG devices present a better performance in terms of higher blocking voltage capabilities, faster-switching speeds, high-temperature operation, and lower on-state resistance [3], [4], [7]. In fact, WBG devices permit the design of DC/DC converters with higher efficiency, higher temperature limits, and faster switching transient than conventional Si-based systems.

Gallium nitride high electron mobility transistors (GaN HEMTs) have key advantages among their competitors. These devices have a high current density and low channel resistance, which are suitable for high-frequency operation and high-efficiency applications [14]. These novel power devices represent a real breakthrough in power electronics. However, many developments are still required, as GaN devices have not reached their maturity for high power high frequencies applications yet.

The Framework in which this manuscript is presented is to obtain an analytical expression for the switching power losses that can be modeled for real-time computations by focusing on the switching transitions. This paper shows the preliminary steps towards that goal, which can be achieved by means of establishing a procedure. The methodology needs to consider the characteristics under all the conditions in the typical mission profiles for the devices in these applications. These include: full range of current values, the voltage range considered, temperature margins in all the operating range of interest for the application (-55 to 150°C) and the ageing process, which means to run the experiments automatically, and to characterize the parameters under different number of cycles.

Therefore, a procedure for testing, measuring and storing the waveforms of the switching intervals, for these conditions, must be carried out. Basically, this is the work presented in this paper. This procedure will establish the files for the simulation, and also the experimental setup needed to achieve these measurements to compare against the simulated ones.

This paper discusses the performance of GaN devices. Section II reviews the characteristics of the GaN device, in addition to that it explains the switching mechanisms. Moreover, Section III clarifies the methodology and conditions of the test. This test provides a practical method for characterizing the transient performance of semiconductors transistors under hard switching. Section IV shows the results of the performed test. Finally, Section V discusses the conclusions and the future developments.

II. Gallium Nitride Transistors Overview

Gallium Nitride (GaN) based on high electron mobility transistors (HEMTs) is a field-effect transistor in which two layers (AlGaN/GaN) of different bandgap and polarization field are grown upon each other, creating the Two Dimensional Electron Gas (2DEG) channel. This 2DEG at the heterojunction works as the conductive channel for large drain currents in any direction due to high electron mobility and high electron sheet charge density, it behaves as an ideal diode. It can be controlled by the gate of the device. This 2DEG

channel is considered one of the main advantages of GaN HEMT devices [15]. It eliminates the need for a body diode to allow the reverse conduction, therefore there will be no minority carriers. So, no reverse recovery losses in e-mode GaN devices and reverse recovery charge (Q_{RR}) will be zero. This enables GaN-based devices to do hard-switching at a relatively high switching frequency, such as half-bridge hard switching which requires hard commutation (higher efficiency and more robust without body diode) [16].

TABLE I: Material Properties of Silicon, GaN, and SiC

Property		**Si**	**GaN**	**SiC**
Bandgap E_g	eV	1.1	3.4	3.26
Critical Field E_{Crit}	MV/cm	0.3	3.3	2.2
Electron Mobility μ_n	cm^2/V.s	1300	1500	950
Electron Saturation Velocity v_{sat}	10^7cm/s	1.0	2.5	2.0
Thermal Conductivity λ	W/cm.K	1.5	1.3	4.9
Permittivity ε_r		11.8	9.0	9.7

From Table I, it is clear that GaN is superior to SiC and Si in terms of electron mobility, energy gap, and breakdown electric field. The high electrical field as well as the high electron velocity of GaN allow switching at a much higher frequency than Si-based devices [15], and enable the potential to increase output power density [17]. The high-frequency operation leads to a reduction in the size of the passive components of the converter, contributing to achieve a compact module [11]. Moreover, the combination of high electric field and high electron velocity will improve the conductivity of the devices for the same breakdown voltage. Therefore, GaN transistors can provide a lower on-resistance compared to silicon and SiC [18].

The low $R_{DS(on)}$ of GaN is one of the main reasons for its small chip size of the transistor. In addition, high output power density allows the fabrication of much smaller size devices with the same output power [19], which means smaller parasitic capacitance elements. On top of that, due to the low $R_{DS(on)}$ GaN has lower conduction losses compared to Si and SiC. The lower the conduction losses are lead to the simpler cooling and heat system, which is desirable for industries looking into the design and manufacturing of more power-dense and less expensive systems.

To demonstrate the potential of GaN in a more concrete case, it was interesting to compare its' switching losses to different semiconductor technologies (Si, SiC and MOSFET). A 15kW buck converter was designed with 500Vdc, 50% duty ratio, 20% current ripple and 100kHz. The three different switches that were used in the comparison are IPT60R028G7 from Infineon for the Si switch, C2M0025120D from Wolfspeed for the SiC switch and GS66516T from GaN Systems for the GaN switch. Figure 1 present the turn on switching losses for the three different switches. By looking at the figure, it is clear that the Si switch takes more time to turn on while the GaN switch is the fastest to turn on, and this in turn affects the switching losses. To calculate the turn on energy losses (E_{on}), the area under the power curve was integrated. The Si switch had the greatest E_{on} with 6.739mJ followed by the SiC with 1.23mJ while the GaN had the lowest 351μJ. Similarly, GaN had the lowest turn off switching losses (E_{off}) between the mentioned technologies. Altogether, GaN proved to have the lowest switching losses, which means that it can be a more suitable choice for the EV application which requires higher frequency and higher efficiency.

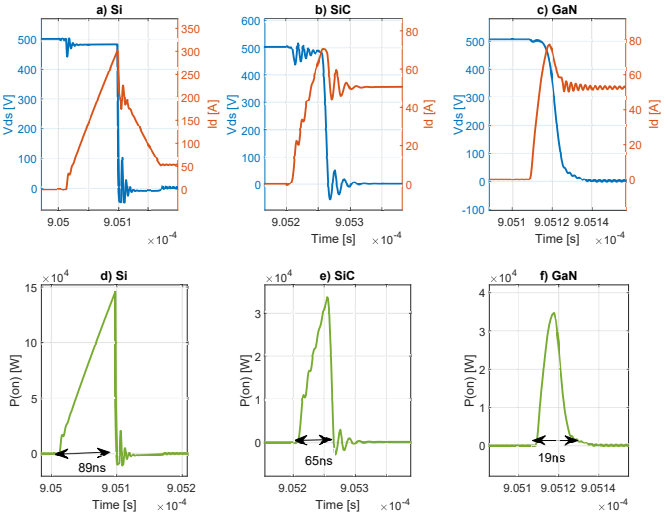


Fig. 1: Switching On transients in A 15kW buck converter using three different semiconductor technologies

In conclusion, GaN has higher efficiency due to its lower conduction, switching losses and the absence of the reverse recovery losses due to zero recovery charges. In addition, it provides the ability to switch at very high switching frequency which can reach MHz. So, all these superior material properties allow the system to be more efficient and lighter-weight, which are the main challenges to achieve in electrical vehicles systems. Although GaN has lower switching losses when compared to the other technologies, parasitic elements will have a serious impact on the switching transients, due to the ability to switch fast. Thus unwanted overshoot and ringing may appear during the switching events. As a consequence, it leads to voltage and current stress of the GaN device, electromagnetic interference (EMI) problems [20]. This creates a challenge to get a simple model of the power losses in HEMT that takes into account all the significant aspects in the switching losses. Nevertheless, this model is important in order to carry out a design that is able to minimize all these aspects. Thus, it is essential to possess information about the switching mechanisms. This information will be analysed and verified through simulations, (relying on the model of the manufacturer) and on the experimental test.

Switching Mechanism

Switching transient analysis is of key significance for the performance evaluation of transistors. During the hard switching, the power device is turned on and off rapidly, while there is still voltage and current across the drain to source channel. This can leads to considerable power losses during the

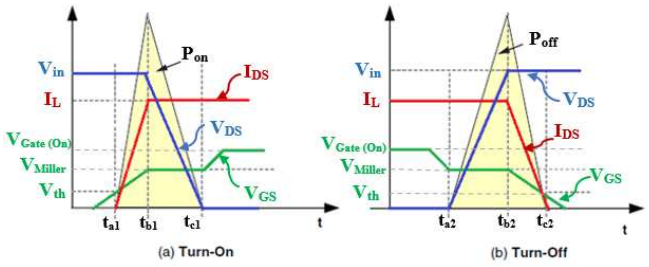
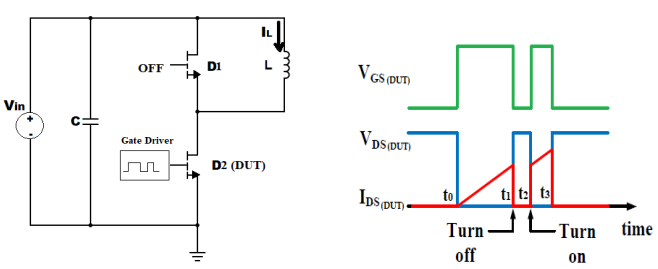


Fig. 2: Idealized switching waveforms used for calculating switching loss (a) turn-on (b) turn-off.



(a) Double-pulse test circuit (b) Double-pulse test signals

Fig. 3: Double Pulse Test.

switching events. Figure 2 shows the switching mechanism and the switching loss during the turn-on and the turn-off events.

At the turn-on event, the gate to source voltage (V_{GS}) starts to increase, and the gate current starts to charge the gate to source capacitance (C_{GS}). At t_{a1}, V_{GS} reaches the threshold voltage and the gate current continues to charge the C_{GS}. From t_{a1} to t_{b1} the drain current (I_{DS}) starts to rise up to reach the load current until C_{GS} is fully charged. After that the gate current starts to charge the gate to drain capacitor (C_{GD}), during this period (t_{b1}-t_{c1}) V_{GS} stays constant, this is known as miller plateau, whereas the drain to source voltage (V_{DS}) starts to fall down, the I_{DS} remains constant when the drain voltage is falling. Charge time for the C_{GD} is larger than that for the C_{GS} due to the fast changing drain voltage between t_{b1}-t_{c1}. However, when both C_{GS} and C_{GD} are fully charged, gate voltage V_{GS} starts increasing again until it reaches the supply voltage. After that, the switch is fully gated on and turn-on transient is over. The overlapping area of V_{DS} and I_{DS} during t_{a1}-t_{c1} is known as the turn-on loss. The turn-off transient is exactly the reverse process [21].

However, the intervals of the waveforms shown in Figure 2 might be a bit different in GaN transistors due to the specific internal structure of the device. Due to these differences the characterization of GaN transistors is required to refine this modeling, which is the main goal of this work.

III. Double Pulse Test

GaN transistors allow operating at a higher frequency which will reduce the overall losses in the system [4]. However, the higher frequency the higher the switching losses in the transistor. For this reason, it is important to understand the behaviour of the switch during each transition and quantifying the losses related to these events.

Double pulse test provides a good method for characterizing the transient performance of the transistor [22], as it allows easy evaluation of the device switching behaviour at high voltage/current without the need to run the system at high power ratings. Furthermore, this test provides the switching loss (E_{on}/E_{off}) measurements, and other switching characterization parameters [23]. On the other hand, the test result accuracy depends a lot on the gate loop and the power loop inductance in the printed circuit board PCB, as well as the measurement techniques.

A double pulse test (DPT) consists of a half-bridge structure with an inductive load, a simplified schematic is shown in Figure 3. The main power loop in the test will start when the device under test (DUT) turns on at t_0, the current will flow from the capacitors to charge the inductor (L) and then flow through the DUT. When the DUT turns off t_1, a freewheeling loop will occur and the inductor will circulate current through the upper transistor and force it to conduct in reverse direction. The upper transistor D1 can be kept turned off during the whole test. In fact, the turn-off and turn-on are the interesting points for this test as they are the hard switching transients for the half-bridge circuit when DUT is under high switching stress.

However, since the test is measuring transient under high stresses, the test result accuracy can be significantly affected by the gate loop or power loop circuit. When switching at high frequency, the parasitic inductances will influence the switching performance of the transistor by creating overshoots and ringing [24]. Not only the design of the power and the gate circuit has an effect on the test accuracy, but also the measurement tool. To determine the switching power characteristics and losses of the power switches precisely, high-performance voltage and current measurement equipment must be used. In addition to the ground loop of the voltage measurement probes should be as short as possible, to prevent it from adding unwanted parasitic inductance which may lead to false and incorrect measurement and evaluation to the behaviour of the transistor.

A. GaN system platform

The test was performed using the high power insulated metal substrate (IMS) evaluation platform from GaN Systems and its corresponding motherboard GSP65HB-EVB, shown in Figure 4. This IMS evaluation platform provides a low-cost solution to transfer heat, increase the power density and cut off the system cost. The GS66516B is a bottom-side cooled E-HEMT, rated at 650V/25mΩ, with Kelvin source pin. The gate voltage operating values according to GS66516B datasheet are 6V/-3V, being the negative bias recommended for the turn-off to prevent false turn-on. This evaluation module is designed with the gate driver as close as possible to the GaN devices to minimize the gate loop inductance. Moreover, the gate resistor is recommended to be separated for turn-on and turn-off.

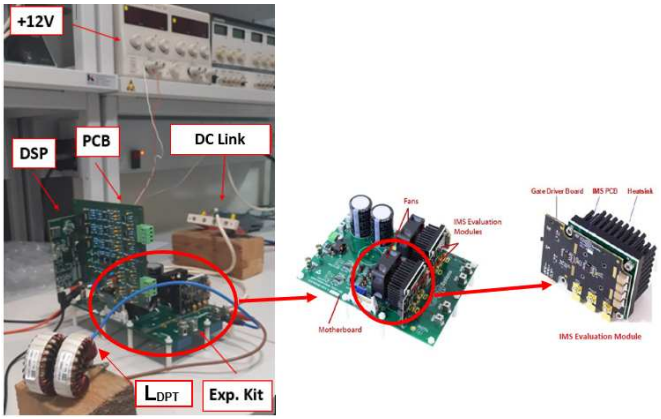


Fig. 4: Double pulse test setup with the experimental evaluation Kit: GSP65RxxHB evaluation motherboard and 650V high power insulated metal substrate (IMS) evaluation modules.

This high-power motherboard is offered by GaN systems it is used to evaluate the IMS evaluation module in any half or full-bridge topology. With this platform, it is possible to evaluate the e-mode GaN HEMT in high-power and high-efficiency applications. The board allows the voltage measurements of V_{GS} and V_{DS}, but unfortunately, it does not have any access to allow measuring the switch current. GaN Systems provides Pspice/ LTSpice simulation models for GaN E-mode HEMT as a development aid tool to evaluate the device performance and to ensure first-pass design success. In addition to that GaN systems provides an LTSpice® simulation file of a half-bridge double pulse test circuit which is used as the test bench to evaluate switching performance under different electrical parameters, it can be found in [26]. This file is a good tool to start and get familiar with the GaN devices switching characteristics. The circuit parameters were modified to match the experimental setup and the evaluation motherboard parameters.

In the next sections, the implementation of the test setup will be discussed. A printed board circuit (PCB) was designed as an interface between the evaluation platform and the micro-control. The DPT signal was generated by Texas Instruments (TI) Microcontroller F28379D controlCARD.

B. Hardware design

GaN devices are very fast switches, any parasitic elements can affect their switching behaviour severely, in a way that may damage the device. The IMS evaluation board is designed to reduce the maximum amount of parasitic elements. Therefore, it is important to pay attention to the setup design, to prevent adding noise to the gate signals that may cause false unwanted turn on, whether for this test or other setups. The setup of the test was designed with a PCB mounted directly on the IMS motherboard through the external PWM and control I/O connector. This PCB is the interface between the F28379D controlCARD, which will be used to generate the gate signals (double pulse signals, PWM signals, etc..), and the IMS motherboard. With this design the least amount of noise will be added to the gate signals, as well the F28379D controlCARD is soldered on top of PCB. To assess the temperature the setup can be easily included in a thermal chamber. And other parameters such as the drain-to-source voltage (V_{DS}) and the gate-to-source voltage (V_{GS}) can be easily obtained with this setup.

The PCB was designed to give the ability of full control of the evaluation board switches in any possible topology. The design was separated into three main parts: voltage and current adapting stage, fault triggering and PWM signal buffering. Fault triggering was designed if the current increases the 30 Amps limit, as the motherboard design does not indicate any faults. The DPT inductor value is 120 µH, the power voltage supply can supply voltage up to 300V. Figure 4 shows the complete setup of the DPT. The test was done under different electrical parameters in order to be able to achieve a clear understanding of the device's performance under different conditions.

The oscilloscope HDO6104A-MS provided by Teledyne LeCroy, is a good choice to measure the voltages and inductor current. It allows to capture and display the signals with 16 times more resolution than other oscilloscopes. Short ground probes were used which have a ground clip attached to the probe ground sleeve, in order to avoid introducing long ground loops to the test. As using a probe with long ground wire will insert unwanted parasitic inductance into the probe measurement path, leading to incorrect measurement results. Furthermore, it is so important to place the probe as close to the required measurement points as possible, to have more accurate results.

IV. Results

In this section, the results of the DPT will be presented and analyzed. The only waveforms that will be analyzed are the (V_{DS}) and the (V_{GS}), since the experimental evaluation board does not allow the accessibility to measure the switch current. However, with these voltages waveforms, it is possible to obtain large information, such as a comparison of the transient response between simulation and experiments, the overshoot voltage, the dV/dt, rise time, fall time and oscillation frequencies. The test was done with input voltages: V_{in} = 50V; 100V; 150V; 200V; 250V; 250V, and 300V. The load currents for each voltage level were: I = 5A; 10A; 15A; 20A; 25A, and 30A. The chosen conditions to be presented in this paper are 300V input voltage, with 5A, 15A and 30A load current. The ambient temperature is around 30°C for the given operating points, due to the very fast nature of the tests and the cooling system, the temperature will not increase too much beyond the room temperature. Nevertheless, the setup proved that it can systematically measure switching intervals of the GaN transistor under any conditions needed to be established.

Figure 5 represents the experimental and simulation results of V_{DS} and V_{GS} transients at turn-off event when V_{DS} equals to 300V with different current ratings. At the turn-off event, a significant increase in the overshoot and the ringing appears when switching off at higher current value.

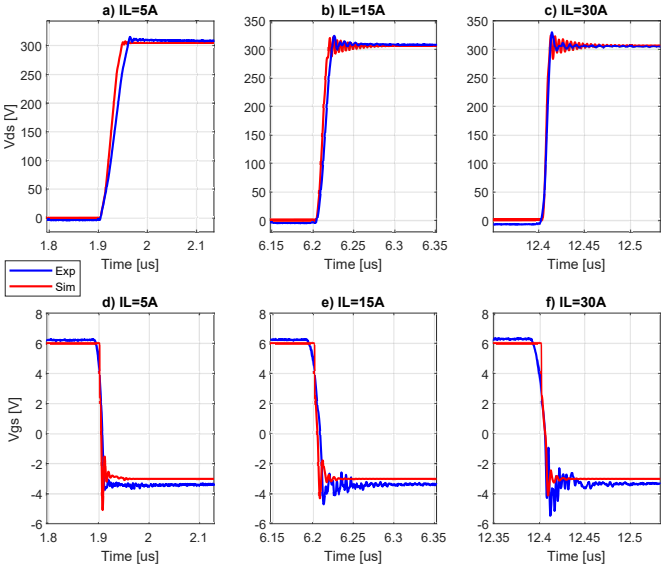


Fig. 5: Turn-off results of the GaN switches at 300V DC link voltage for different operating conditions: Drain to source voltages, V_{DS} (a) at 5A; (b) at 15A (c) at 30A; Gate to source voltage, V_{GS} (d) at 5A; (e) at 15A; (f) at 30A

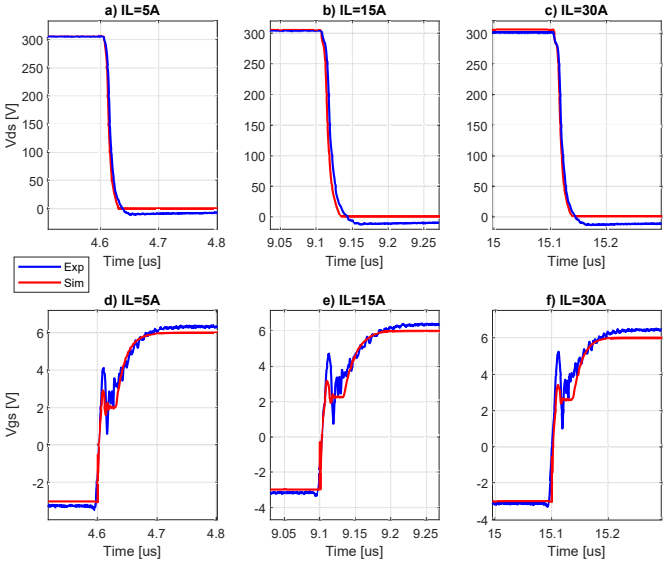


Fig. 6: Turn-on results of the GaN switches at 300V DC link voltage for different operating conditions: Drain to source voltages, V_{DS} (a) at 5A; (b) at 15A (c) at 30A; Gate to source voltage, V_{GS} (d) at 5A; (e) at 15A; (f) at 30A

Nevertheless, increasing the current will increase the dv/dt, thus the transistor will have a faster response, it has increased from 5V/ns to 36.7V/ns. Moreover, it was noted during the test that increasing the voltage for the same current level improves the overshoot as well as enables faster switching. While for V_{GS} More ringing appeared when the current increased.

Figure 6 represents the experimental and simulation results of V_{DS} and V_{GS} transients at turn-on event when V_{DS} equals to 300V with different current ratings. At the turn-on event, increasing the current for the same voltage value did not have much impact on the behaviour of the device, the switch was able to turn on by almost 14V/ns. Notice there is a dip that occurred in V_{DS} waveform, which gets more clear when the current increased, specifically at 30A, this dip is caused by the loop inductance (L_p) which equals to ($\Delta V_{DS} = L_p \times di/dt$). However, during the test, it was noted that for the same current rating but different voltages, the higher the voltage the faster the switching speed will be.

From Figure 6, it can be noted that the miller plateau is close to 3V which is matching with the datasheet of GS66516B. The miller plateau effect is not seen clearly in the turn-off event when compared to the turn on event, explaining why the device switches off faster than switching on. Through out the different tests that were made, it was noted that increasing V_{DS} makes the miller plateau becomes more visible in the V_{GS} at the turn-on event. Finally, turn-off time is shorter than turn-on time is longer when switching at higher current ratings.

From the Figures 5 and 6, it can be observed that the LTspice simulations results match the experiment ones quite good. There is a little bit of voltage drop in the experimental waveforms, this can be due to the losses in the setup or caused by measurement errors. Nevertheless, both ways proved that the GaN device have the ability to switch on and of very fast, which makes it suitable for high frequency applications. However, the final real waveforms are not similar to the the ones depicted in the ideal case of Figure 2, which implies the necessity to derive the model of the analytical expression for the switching power losses. This model should be simple, accurate, and based on experiments, and if not, on simulations. With this model, the design of any converter can be enhanced and it can be used in real-time control application.

Finally because of the good match between both simulations and experimental results, the energy losses can be calculated and analyzed by the simulation tool since the current could not be measured in the experimental work. Figure 7 shows the switching losses E_{on}+E_{off} for different voltage and current levels. The maximum loss was at 300V and 30A which is equal to 129.807 µJ. Anyway this results is pretty close to the values mentioned in the device datasheet, which indicates that at 400V and 20A the E_{on} will be equal to 134.1 µand the E_{off} will be equal to 14.7 µJ, so the total losses 148.8 µJ. From these results, it was confirmed that GaN can be used for high efficiency application such as EVs applications.

V. Conclusion

In this paper, the material properties of the GaN transistor were studied to see the ability of this new technology to meet the future needs of the DC/DC converters for EVs application. In addition to that, a double pulse test was carried out to study the switching behaviour of GaN devices. the test proved that The GaN device can switch fast, it takes 36.7V/ns to turn-off and 14 V/ns to turn-on, which means that this transistor is suitable for the high-frequency application. Unfortunately, the (IMS) evaluation platform from GaN Systems does not allow

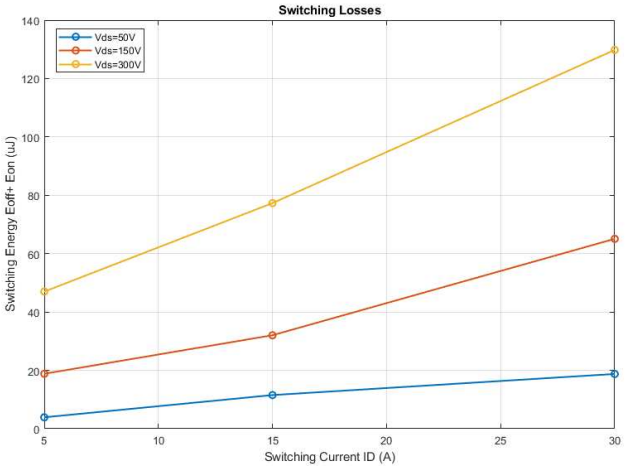


Fig. 7: Switching losses for different voltage and current levels

drain current measurement, so it was not possible to calculate the experimental switching losses. For the future work, it is planned to design a platform that allows access to the drain current. Therefore, with the information about the switch current, it will be possible to drive the final model for losses which allows to calculate the power losses. Moreover, it will be interesting to implement the test under different temperatures, to see the affect of changing the temperature on the device behaviour and the switching losses. The characterisation and the analysis can be extend to other switches to increase the generality of the model. Thus, the optimal design of the DC/DC converter for electrical vehicles can be achieved.

ACKNOWLEDGMENT

This work has been partially funded from the EU H2020 R&I Program under grant agreement 864459 (Project "TALENT"), and through ERFD Structural Funds. This wok has been partially supported by the Spanish Government, ID&R Office (MEC), under research grants ENE2016-77919 (Project "Conciliator"), and PID2019-111051RB-100 (Project "B2B-Energy"). This work has been partially supported by the government of Principality of Asturias (FICYT), under Grant FC-GRUPIN-IDI/2018/000241 and Severo Ochoa research grant PF-BP19-078.

REFERENCES

[1] K. Rajashekara, "Power electronics applications in electric/hybrid vehicles," IECON'03. 29th Annual Conference of the IEEE Industrial Electronics Society (IEEE Cat. No.03CH37468), Roanoke, VA, USA, 2003, pp. 3029-3030 Vol.3.

[2] A. Emadi, Y. J. Lee and K. Rajashekara, "Power Electronics and Motor Drives in Electric, Hybrid Electric, and Plug-In Hybrid Electric Vehicles," in IEEE Transactions on Industrial Electronics, vol. 55, no. 6, pp. 2237-2245, June 2008.

[3] B. Bilgin et al., "Making the Case for Electrified Transportation," in IEEE Transactions on Transportation Electrification, vol. 1, no. 1, pp. 4-17, June 2015.

[4] N. Keshmiri, D. Wang, B. Agrawal, R. Hou and A. Emadi, "Current Status and Future Trends of GaN HEMTs in Electrified Transportation," in IEEE Access, vol. 8, pp. 70553-70571, 2020.

[5] D. M. Bellur and M. K. Kazimierczuk, "DC-DC converters for electric vehicle applications," 2007 Electrical Insulation Conference and Electrical Manufacturing Expo, Nashville, TN, 2007, pp. 286-293, doi: 10.1109/EEIC.2007.4562633.

[6] Sakka, M. A.; Van Mierlo, J. and Gualous, H. DC/DC Converters for Electric Vehicles Electric Vehicles - Modelling and Simulations, 2011

[7] J. Millán, P. Godignon, X. Perpiñà, A. Pérez-Tomás and J. Rebollo, "A Survey of Wide Bandgap Power Semiconductor Devices," in IEEE Transactions on Power Electronics, vol. 29, no. 5, pp. 2155-2163, May 2014.

[8] M. Kanechika, T. Uesugi and T. Kachi, "Advanced SiC and GaN power electronics for automotive systems," 2010 International Electron Devices Meeting, San Francisco, CA, 2010, pp. 13.5.1-13.5.4.

[9] P. Friedrichs, J. Millan, T. Harder, N. Kaminski, A. Lindemann, L. Lorenz, L.Schindele, and P. Ward. ECPE position paper on next generation power electronics based on wide bandgap devices. ECPE Position, 2016.

[10] J. Millán, P. Godignon and A. Pérez-Tomás, "Wide Band Gap Semiconductor Devices for Power Electronics", Automatika, vol.53, no. 2, pp. 107-116, 2012. [Online]. https://doi.org/10.7305/automatika.53-2.177

[11] T. Kachi, D. Kikuta and T. Uesugi, "GaN power device and reliability for automotive applications," 2012 IEEE International Reliability Physics Symposium (IRPS), Anaheim, CA, 2012, pp. 3D.1.1-3D.1.4.

[12] S. Das, L. D. Marlino, and K. O. Armstrong, "Wide bandgap semiconductor opportunities in power electronics," Oak Ridge National Lab., Oak Ridge, TN, USA, Tech. Rep. ORNL/TM-2017/702, 2018.

[13] W. Zhang et al., "Wide bandgap power devices based high efficiency power converters for data center application," 2014 IEEE Workshop on Wide Bandgap Power Devices and Applications, Knoxville, TN, 2014, pp. 121-126.

[14] U. K. Mishra, L. Shen, T. E. Kazior and Y. Wu, "GaN-Based RF Power Devices and Amplifiers," in Proceedings of the IEEE, vol. 96, no. 2, pp. 287-305, Feb. 2008, doi: 10.1109/JPROC.2007.911060.

[15] A. Lidow, J. Strydom, M. de Rooij, and D. Reusch. GaN Transistors for Effcient Power Conversion. Wiley, 2014.

[16] R. Hou, J. Lu and D. Chen, "Parasitic capacitance Eqoss loss mechanism, calculation, and measurement in hard-switching for GaN HEMTs," 2018 IEEE Applied Power Electronics Conference and Exposition (APEC), San Antonio, TX, 2018, pp. 919-924.

[17] Bahat-Treidel, Eldad. GaN Based HEMTs for High Voltage Operation. Design, Technology and Characterization. 2012 10.14279/depositonce-3203.

[18] Rophina Chi-Wai Li. Driving techniques for GaN power hemts. Master's project, University of Toronto, 2016.

[19] U. K. Mishra, L. Shen, T. E. Kazior and Y. Wu, "GaN-Based RF Power Devices and Amplifiers," in Proceedings of the IEEE, vol. 96, no. 2, pp. 287-305, Feb. 2008.

[20] J. Lautner and B. Piepenbreier, "Analysis of GaN HEMT switching behavior," 2015 9th International Conference on Power Electronics and ECCE Asia (ICPE-ECCE Asia), Seoul, 2015, pp. 567-574, doi: 10.1109/ICPE.2015.7167840.

[21] B. Sun, Z. Zhang and M. A. E. Andersen, "Switching transient analysis and characterization of GaN HEMT," 2018 3rd International Conference on Intelligent Green Building and Smart Grid (IGBSG), Yi-Lan, 2018, pp. 1-4, doi: 10.1109/IGBSG.2018.8393542.

[22] B. Sun, Z. Zhang and M. A. E. Andersen, "Switching transient analysis and characterization of GaN HEMT," 2018 3rd International Conference on Intelligent Green Building and Smart Grid (IGBSG), Yi-Lan, 2018, pp. 1-4.

[23] GaN Systems. GS66508T-EVBDB2/ GS66516T-EVBDB2, GaN E-HEMT Daughter Board, and GS665MB-EVB Evaluation Platform User's Guide, 2018

[24] Galanos, Nicolas. "Investigation of the inductor's parasitic capacitance in the high frequency switching of the high voltage cascode GaN HEMT." 2015.

[25] GaN Systems. GSP65RxxHB-EVB 650V High Power IMS Evaluation Platform User's Guide, 2017.

[26] GaN Systems. GN006 Application Note: SPICE model for GaN HEMT usage guidelines and example., August 2016.