Discrete-time modeling of pulse-width modulated DC-DC converters in sub-sampling conditions

Pablo F. Miaja, Marlon Alberto Granda, Cristina Fernandez, Maria R. Rogina, Pablo Zumel

Part of this paper was presented at COMPEL 2018 held in Padova, Italy, in June 2018

Abstract

This paper presents an extension of a small-signal discrete time modeling procedure for DC-DC converters. It takes into account the fact that the time between samples can be an integer multiple of the switching period of the converter, thus in under-sampling or sub-sampling conditions. The objective of this paper is to obtain a small-signal discrete model so the degradation in the dynamic performance of the DC-DC converter introduced by the sub-sampling conditions can be assessed and a proper controller designed.

Index Terms

small-signal discrete time model DC/DC converters

I. Introduction

Digital control of DC-DC converters has been a well established discipline since the early 2000's. At the cornerstone of the digital control design process is the discrete small-signal

model of the DC-DC switching converter to be regulated. Although discretization of the classical averaged small-signal models [1] is possible and often used, discrete-time modeling techniques are recognized as being more accurate for the task and a wide number of references can be found in the literature [2]–[5]. Small-signal discrete-time models take into account aliasing effects that the averaged models do not consider [4]. In almost all the examples found in the literature the discretization is done at the switching period of the converter so a sample of the variable to control (i.e. the output voltage v_o) is always present for setting the duty cycle for the next switching period.

In order to improve the dynamic response of DC-DC converters, over-sampling, or getting more samples per switching period, has been proposed [6]–[8]. However, to the best knowledge of the authors, no explicit model for the opposite situation, sub-sampling, has been published. In this context, sub-sampling means that the variables used to calculate the control actions are taken at such a rate that more than one switching cycle take place between samples. This implies that the same control action is applied to several switching cycles. Therefore, the dynamic properties of the converter degrade. However, in certain cases, when the hardware available is not powerful enough to perform the control actions at the switching rate, it may be the only solution possible and it has been used where restrictions (such as cost, space, hardware availability, power consumption, etc.) in the control platform prevent the use of more powerful hardware capable of dealing with the control at the switching rate. In [9] an example of a Power Factor Corrector at MHz switching frequency is carried out using a microcontroller. The control shown is complex and it is carried out at least each 4 switching cycles. This is an example on how thanks to the use of wide-bandgap semiconductors and optimized designs in terms of efficiency and power density switching frequencies are increasing and the control platforms may not be able to work at the same rate. In some cases, the control does not require a sampling frequency as high as switching frequency. Sub-sampling is then useful to save resources in the digital controller. For example, in [10], sub-sampling is used in steady-state conditions to reduce the power consumption of the control chip, whilst control at the switching frequency is used during transients in order to improve the dynamic response. Another example of these kind of limitations can be seen in space applications. Although the digital control is very interesting for the reasons well known in terrestrial applications, (adaptability, integration with advanced diagnostics, digital management and communication buses,...) the radiation tolerant, space grade, hardware available is usually

less powerful than their terrestrial counterparts.

An accurate dynamic model of the converter under sub-sampled conditions can be used in the design process to asses the degradation of the dynamic behavior in order to determine the minimum digital resources to achieve a specified dynamic performance. The calculation of the regulator needs an accurate small signal model to achieve in the practice the dynamic specification, typically in terms of cross over frequency and phase margin. Other functionalities, such as health monitoring [11] [12], are based on the accurate knowledge of the converter model and the capability to measure the value of different components through parametric identification techniques [13].

In order to provide an accurate knowledge of the dynamic behavior of the converter in sub-sampling conditions a discrete model including this effect is presented in this paper. It is based on the same techniques presented in [3], [4]. A state-space representation and a numerical evaluation of the propagation of such states is used to determine the small-signal model, in fact, it can be seen as an extension of the procedures described in [3], [4].

The paper is organized as follows: Section II shows the process to derive the model and a theoretical example using a buck converter, section III shows the experimental results using a buck and a boost converters. Finally, conclusions are addressed in section IV.

II. GENERALIZATION OF THE SMALL-SIGNAL DISCRETE-TIME MODEL

As aforementioned, the approach followed in this paper builds on the methodology presented in [3], [4], which is based on the perturbation and linearisation of the sampled converter state vector in the vicinity of the converter operating point, thus obtaining the small-signal state-space description of the sampled dynamics.

$$\hat{\mathbf{x}}[k + 1] = \mathbf{\Phi}\hat{\mathbf{x}}[k] + \gamma\hat{u}[k]$$

$$\hat{\mathbf{y}}[k] = \delta\hat{\mathbf{x}}[k]$$

(1)

With this representation the value of the sampled state vector $\hat{\mathbf{x}}[k + 1]$ at instant $k + 1$ is obtained based on the state vector sampled at instant k, $\hat{\mathbf{x}}[k]$, the small-signal state matrix $\mathbf{\Phi}$ and the small-signal control-to-state matrix γ. The converter output matrix δ will be the converter

output matrix in the topological state of the converter at the sample instant.

Let us suppose, without the loss of generality, that the converter has two topological states S_0 and S_1 selected by the state of the switches of the converter, and that between sample k and sample $k + 1$ there are n_{sub} switching periods, each one of duration T_s. Please note that if $n_{sub} = 1$, then a sample is taken at each switching cycle and the situation is the same as the one explained in [3], [4]. Let us assume too that we are using a trailing edge pulse width modulator and that the amplitude of the PWM ramp is $N_r = 1$. Therefore, a small change in the duty cycle $\hat{d}[k]$, will translate into a control variation $\hat{u}[k] = \hat{d}[k]T_s$. The samples are taken whilst the converter is in the topological state S_0, between a sample of $\hat{\mathbf{x}}[\mathbf{k}]$ is taken and $\hat{d}[k]$ takes place, the delay time t_d is elapsed. Under trailing-edge pulse width modulation t_d accounts for the computation time to calculate the new duty cycle, t_{ctrl} and the time spent on the state S_1, DT_s, which is determined by the converter steady state duty cycle D. Therefore

$$t_d = t_{ctrl} + DT_s \tag{2}$$

In this paper we will denote the complementary duty cycle as $D' = 1 - D$. This is the situation depicted in Fig. 1.

In order to calculate the evolution of the small-signal state vector it is necessary to propagate $\hat{\mathbf{x}}[k]$ until the time at which sample $\hat{\mathbf{x}}[k + 1]$ is taken, whilst assuming that $\hat{u}[k] = 0$. This propagation takes into account the different topological states S_0 and S_1. Propagation is carried
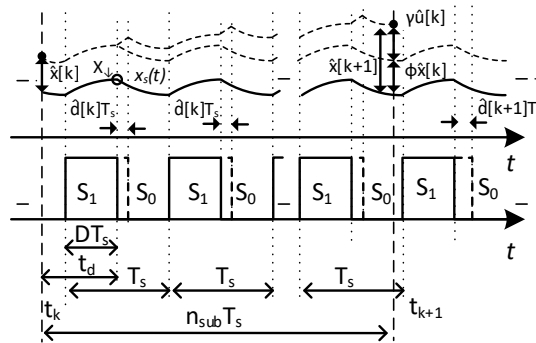

Fig. 1: State propagation

out through the application of the operator $e^{A_c t}$, being A_c the state matrix correspondent to either states S_0 or S_1. Therefore, in the situation depicted in Fig. 1, $\hat{\mathbf{x}}[k]$ is propagated in state S_0 during $(t_d - DT_s)$. At this instant the converter changes to state S_1, so the propagation is done in this state S_1 during DT_s. At this instant, the state of the converter changes to S_0 during $D'Ts$ and then again S_1 during DT_s. The propagation through S_0 during $D'T_s$ and S_1 during DT_s repeats for $(n_{sub} - 1)$ times. Finally, it propagates through S_0 during $T_s - t_d$ to get the sample $k + 1$. Therefore:

$$
\begin{aligned}
\hat{\mathbf{x}}[k + 1] =& e^{\mathbf{A_0}(T_s - t_d)} \cdot e^{\mathbf{A_1} DT_s} \cdot e^{\mathbf{A_0} D' T_s} \\
& \ldots \cdot e^{\mathbf{A_1} DT_s} \cdot e^{\mathbf{A_0}(t_d - DT_s)} \cdot \hat{\mathbf{x}}[k] = \\
& e^{\mathbf{A_0}(T_s - t_d)} \cdot \left(e^{\mathbf{A_1} DT_s} \cdot e^{\mathbf{A_0} D' T_s} \right)^{(n_{sub} - 1)} \\
& \cdot e^{\mathbf{A_1} DT_s} \cdot e^{\mathbf{A_0}(t_d - DT_s)} \cdot \hat{\mathbf{x}}[k]
\end{aligned}
\tag{3}
$$

Then matrix $\mathbf{\Phi}$ is:

$$
\begin{aligned}
\mathbf{\Phi} =& e^{\mathbf{A_0}(T_s - t_d)} \cdot \left(e^{\mathbf{A_1} DT_s} \cdot e^{\mathbf{A_0} D' T_s} \right)^{(n_{sub} - 1)} \\
& \cdot e^{\mathbf{A_1} DT_s} \cdot e^{\mathbf{A_0}(t_d - DT_s)}
\end{aligned}
\tag{4}
$$

Matrix γ represents the action of the duty cycle variation $\hat{d}[k]$. It should be noted that, in the under-sampled conditions addressed in this paper, the perturbation $\hat{d}[k]$ will be applied at the end of every transition between S_1 and S_0 between the samples k and $k + 1$. Therefore it will be applied n_{sub} times, each one with the appropriate propagation through the states of the converter. This situation is also depicted in Fig. 1. Therefore, assuming that $\hat{x}[k] = 0$, then:

$$\hat{\mathbf{x}}[k+1] = \gamma \hat{u}[k] =$$

$$e^{\mathbf{A_0}(T_s - t_d)} \cdot$$

$$[(\mathbf{A_1 X_\downarrow} + \mathbf{B_1 V}) - (\mathbf{A_0 X_\downarrow} + \mathbf{B_0 V})] \frac{\hat{u}[k]}{N_r} T_s +$$

$$e^{\mathbf{A_0} D' T_s} e^{\mathbf{A_1} D T_s} e^{\mathbf{A_0}(T_s - t_d)} \cdot$$

$$[(\mathbf{A_1 X_\downarrow} + \mathbf{B_1 V}) - (\mathbf{A_0 X_\downarrow} + \mathbf{B_0 V})] \frac{\hat{u}[k]}{N_r} T_s \tag{5}$$

$$\vdots$$

$$\left(e^{\mathbf{A_0} D' T_s} e^{\mathbf{A_1} D T_s} \right)^{n_{sub}-1} e^{\mathbf{A_0}(T_s - t_d)}$$

$$\cdot [(\mathbf{A_1 X_\downarrow} + \mathbf{B_1 V}) - (\mathbf{A_0 X_\downarrow} + \mathbf{B_0 V})] \frac{\hat{u}[k]}{N_r} T_s$$

where $\mathbf{X_\downarrow}$ is the state vector at the transition between states S_0 and S_1. It only depends on the steady state values [4] and equals

$$\mathbf{X_\downarrow} = \left(\mathbf{I} - e^{\mathbf{A_1} D T_s} \cdot e^{\mathbf{A_0} D' T_s} \right)^{-1}$$

$$\cdot \left[-e^{\mathbf{A_1} D T_s} \cdot \mathbf{A_0}^{-1} \cdot \left(\mathbf{I} - e^{\mathbf{A_0} D' T_s} \right) \cdot \mathbf{B_0} \right. \tag{6}$$

$$\left. -\mathbf{A_1}^{-1} \cdot \left(\mathbf{I} - e^{\mathbf{A_1} D T_s} \right) \cdot \mathbf{B_1} \right] \cdot \mathbf{V}$$

The expression $[(\mathbf{A_1 X_\downarrow} + \mathbf{B_1 V}) - (\mathbf{A_0 X_\downarrow} + \mathbf{B_0 V})]$ is the linear approximation of the change between states S_0 and S_1. As it only depends on steady-state quantities it will be the same over all the cycles between samples.

The first summand on (5) represents the effect of the perturbation in the last S_1 to S_0 transition before sample $k+1$, the second summand the effect of the perturbation over the transition before the last one, finally, the last summand represent the effect of the perturbation in the first transition from S_1 to S_0 after sample k. Rearranging terms in (5), γ becomes

$$\gamma = \sum_{i=0}^{n_{sub}-1} \left[\left(e^{\mathbf{A_0} D' T_s} \cdot e^{\mathbf{A_1} D T_s} \right)^i \cdot e^{\mathbf{A_0}(T_s - t_d)} \right.$$

$$\left. \cdot [(\mathbf{A_1 X_\downarrow} + \mathbf{B_1 V}) - (\mathbf{A_0 X_\downarrow} + \mathbf{B_0 V})] \cdot \frac{T_s}{N_r} \right] \tag{7}$$

Finally, as in the conventional trailing-edge PWM case the samples are taken during the topological state S_0 the converter output matrix

$$\delta = \mathbf{C_0} \tag{8}$$

Please note that both in (4) and (7) making $n_{sub} = 1$ lead to the expressions presented in [4] for the one sample per switching cycle case. With this two expressions and the one in (8) the system in (1) can be calculated and all the discrete transfer functions, such as the output voltage to control $G_{vd}[z]$ and inductor current to control $G_{id}[z]$, obtained.

A. Generalization to leading edge and symmetrical pulsewidth modulations

The aforementioned result was carried out for the case of trailing edge pulsewidth modulation. However they can be extended to the leading edge and symmetrical pulsewidth modulation by reworking the calculation of matrix $\boldsymbol{\Phi}$, explained in (4), and the process for γ explained in (7).

1) Leading Edge Modulation: The state propagation for the leading edge modulation is depicted in Fig. 2. The sample is taken again in the topological state S_1. The delay time t_d will take into account the time elapsed since the sample is taken and when the control action takes place, at the following rising edge. Therefore,

$$t_d = t_{ctrl} + D'T_s \tag{9}$$

please note how the delay time depends on D' and not in D as it was the case for the trailing edge (2).
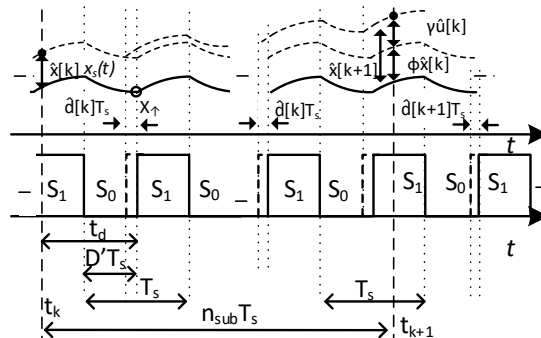

Fig. 2: State propagation for leading edge modulation

Following the same procedure described in (5) matrix $\mathbf{\Phi}$ is determined. It has to be taken into account that first the states should be propagated through $\mathbf{A_1}$ during $(t_d - D'T_s)$, then through $\mathbf{A_0}$ during $D'T_s$ and through $\mathbf{A_1}$ during DT_s. This latter process is repeated for all the complete periods between samples. Finally when we reach to the last period we will propagate again through $\mathbf{A_0}$ during $D'T_s$ and through $\mathbf{A_1}$ during $T_s - t_d$. Therefore,

$$\mathbf{\Phi} = e^{\mathbf{A_1}(T_s - t_d)} \cdot \left(e^{\mathbf{A_0} D'T_s} \cdot e^{\mathbf{A_1} DT_s} \right)^{(n_{sub}-1)} \cdot e^{\mathbf{A_0} D'T_s} \cdot e^{\mathbf{A_1}(t_d - D'T_s)} \tag{10}$$

Again if we make $n_{sub} = 1$ we will be taking one sample per switching period and the expression is compatible with what appears in [4].

At the core of the operation to derive γ we will need to derive a linear approximation to the effect of the change between state S_0 to S_1. For this we will need to derive $\mathbf{X_\uparrow}$, the state vector at the transition from S_0 to S_1. This is taken from $\mathbf{X_\downarrow}$ (6). As $\mathbf{X_\uparrow}$ is determined from the steady state values it will be the same for all the cycles. This work is carried out in [4] and reproduced here for the ease of the reader.

$$\mathbf{X_\uparrow} = \mathbf{X_\downarrow} \cdot \left[e^{\mathbf{A_0} D'T_s} - \mathbf{A_0}^{-1} \left(\mathbf{I} - e^{\mathbf{A_0} D'T_s} \right) \mathbf{B_0} \right] \mathbf{V} \tag{11}$$

Matrix γ will represent the translation of the duty cycle perturbation at the beginning of each switching cycle through the topological states. So it will be propagated through $\mathbf{A_1}$ from the change from S_0 to S_1 to the instant of the sampling, this time is $(T_s - t_d)$. This will model the influence of the last transition. Then through a succession of S_0 states during $D' \cdot T_s$ and S_1 during $D \cdot S_1$. The total response will be the superposition of the individual perturbations correctly propagated, much in the sense of (7). The complete expression is

$$\gamma = \sum_{i=0}^{n_{sub}-1} \left[e^{\mathbf{A_1}(T_s - t_d)} \cdot \left(e^{\mathbf{A_0} D'T_s} \cdot e^{\mathbf{A_1} DT_s} \right)^i \cdot \left[(\mathbf{A_1}\mathbf{X_\uparrow} + \mathbf{B_1}\mathbf{V}) - (\mathbf{A_0}\mathbf{X_\uparrow} + \mathbf{B_0}\mathbf{V}) \right] \cdot \frac{T_s}{N_r} \right] \tag{12}$$

Again if $n_{sub} = 1$ subsampling is not used and the expressions are the same as in [4]. Finally as the samples are taken during the topological state S_1 the converter output matrix

$$\delta = \mathbf{C_1} \tag{13}$$

2) Dual Edge or Symmetrical Modulation: One of the most common PWM techniques is to compare the duty cycle command with an up and down ramp elapsing the switching period T_s. Therefore the ramp will go up for $T_s/2$ and down for $T_s/2$. The converter will be in topological state S_1 whenever the duty cycle command is below the ramp and in S_0 otherwise. Therefore, a small change in the duty cycle $\hat{d}[k]$, will translate into two control variations $\hat{u}[k] = \hat{d}[k]Ts/2$ one at the leading edge of the transition and the other at the trailing edge. So up to some point it can be said that it is the superposition of the trailing edge and the leading edge modulations. Furthermore, often the sampling is performed at the peak of the ramp. This fixes the delay time to $t_d = T_s/2$ and has the benefit to reduce the aliasing effect. For example, the inductor current sample will be taken at the time in which the current value coincides with its average value. In this case, the sample will be taken in the topological state S_0. The state propagation can be seen in Fig. 3. In order to calculate $\boldsymbol{\Phi}$ it can be seen how the sampled states are propagated through S_0 for $T_s/2$, then through a S_1 for DT_s, through S_0 for $D'Ts$, these will be the complete switching periods between samples, and finally through S_1 for DT_s and through S_0 for $D'Ts/2$. The expression for $\boldsymbol{\Phi}$ will be

$$\boldsymbol{\Phi} = e^{\mathbf{A_0}\left(D'\frac{T_s}{2}\right)} \cdot \left(e^{\mathbf{A_1}DT_s} \cdot e^{\mathbf{A_0}D'T_s}\right)^{(n_{sub}-1)} \cdot e^{(\mathbf{A_1}DT_s)} \cdot e^{\left(\mathbf{A_0}D'\frac{T_s}{2}\right)} \tag{14}$$

$$\gamma = \sum_{i=0}^{n_{sub}-1} \left\{ e^{\mathbf{A_0}(D'T_s/2)} \cdot \left[\left(e^{\mathbf{A_1}DT_s} \cdot e^{\mathbf{A_0}D'T_s}\right)^i \cdot F_\downarrow + \left(e^{\mathbf{A_1}DT_s} \cdot e^{\mathbf{A_0}D'T_s}\right)^i \cdot e^{(\mathbf{A_1}DT_s)} \cdot F_\uparrow \cdot \frac{T_s}{N_r} \right] \right\} \tag{15}$$

where $F_\uparrow$ is

$$F_\uparrow = [(\mathbf{A_1X_\uparrow} + \mathbf{B_1V}) - (\mathbf{A_0X_\uparrow} + \mathbf{B_0V})] \tag{16}$$

and $F_\downarrow$ is

$$F_\downarrow = [(\mathbf{A_1X_\downarrow} + \mathbf{B_1V}) - (\mathbf{A_0X_\downarrow} + \mathbf{B_0V})] \tag{17}$$

The expressions for $\mathbf{X_\downarrow}$ and $\mathbf{X_\uparrow}$ were defined previously in (6) and in (11) respectively.

Finally as the samples are taken during the topological state S_0 the converter output matrix is then

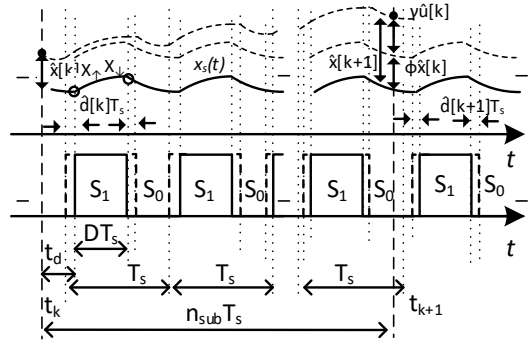$$\delta = \mathbf{C_0} \tag{18}$$

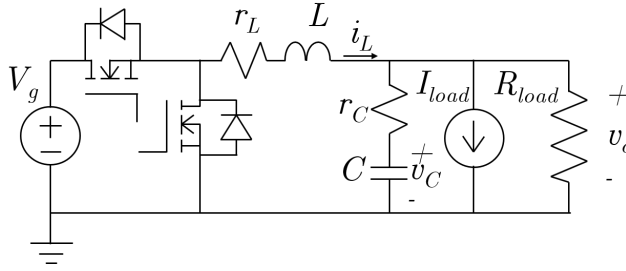Fig. 3: State propagation for symmetrical modulation

Fig. 4: Buck converter used as validation example

As in all the previous cases making $n_{sub} = 1$ in (14) and in (15) renders the expression without subsampling shown in [4].

B. Example: buck converter

In order to validate the approach presented in section II an example based on a buck converter (Fig. 4) has been developed. A buck converter in Continuous Conduction Mode with a trailing-edge PWM was chosen because the state matrix does not change between the topological states S_0 and S_1, and therefore, the small signal discrete model can be obtained via a impulse invariant discretization [4], which will be used to validate the approach presented in section II. The different matrix values can be found in [4] and are reproduced here in (19) and 20) for easing the reader's task.

$$r_{par} = \frac{r_c}{1 + r_c/R_{Load}}$$

$$\mathbf{A_1} = \mathbf{A_0} = \begin{bmatrix} -\dfrac{1}{L} \cdot (r_{par} + r_L) & -\dfrac{1}{L} \cdot \dfrac{1}{1 + r_C/R_{Load}} \\[2ex] \dfrac{1}{C} \cdot \dfrac{1}{1 + r_C/R_{Load}} & -\dfrac{1}{C} \cdot \dfrac{1}{r_C + R_{Load}} \end{bmatrix}$$

$$\mathbf{B_0} = \begin{bmatrix} 0 & \dfrac{r_{par}}{L} & -\dfrac{1}{L} \cdot \dfrac{1}{1 + r_C/R_{Load}} \\[2ex] 0 & -\dfrac{1}{C} \cdot \dfrac{1}{1 + r_C/R_{Load}} & \dfrac{1}{C} \cdot \dfrac{1}{r_C + R_{Load}} \end{bmatrix} \tag{19}$$

$$\mathbf{B_1} = \begin{bmatrix} \dfrac{1}{L} & \dfrac{r_{par}}{L} & -\dfrac{1}{L} \cdot \dfrac{1}{1 + r_C/R_{Load}} \\[2ex] 0 & -\dfrac{1}{C} \cdot \dfrac{1}{1 + r_C/R_{Load}} & \dfrac{1}{C} \cdot \dfrac{1}{r_C + R_{Load}} \end{bmatrix}$$

$$\mathbf{C_1} = \mathbf{C_0} = \begin{bmatrix} 1 & 0 \\[1ex] r_{par} & \dfrac{1}{1 + r_C/R_{Load}} \end{bmatrix}$$

$$\hat{\mathbf{x}} = \begin{bmatrix} \hat{i}_L \\ \hat{v}_C \end{bmatrix} \quad \hat{\mathbf{y}} = \begin{bmatrix} \hat{i}_L \\ \hat{v}_o \end{bmatrix} \quad \mathbf{V} = \begin{bmatrix} V_g \\ I_{Load} \\ V_o \end{bmatrix} \tag{20}$$

The values of the constructive elements of the buck converter (Fig. 4) are the following: $L = 65 \ \mu H$, $C = 104 \ \mu F$, $r_L = 128 \ m\Omega$ and $r_C = 110 \ m\Omega$. Switching frequency is $100 \ kHz$. The output voltage is $V_o = 4 \ V$ and the load is considered a current source with a value of $I_{Load} = 1.9A$, $R_{load} = \infty$. For this example the input voltage is $V_g = 8 \ V$, thus the steady state duty cycle is $D = 0.5$. It will be assumed that the sampling occurs at the beginning of the switching cycle, so $t_d = D \cdot T_s = 5 \ \mu s$.

The discrete model has been calculated with a sample per switching cycle so $n_{sub} = 1$, then the sampling frequency $f_{samp} = 100 \ kHz$, and therefore the correspondent Nyquist frequency is $f_{Nyq} = 50 \ kHz$. Cases studied are two switching cycles between samples, $n_{sub} = 2$, then $f_{samp} = 50 \ kHz$ and $f_{Nyq} = 25 \ kHz$, and 4 switching cycles between samples $n_{sub} = 4$, thus $f_{samp} = 25 \ kHz$ and $f_{Nyq} = 12.5 \ kHz$.

Results can be seen in Fig. 5 where the Bode plots at different sub-sampling rates for both the transfer function $G_{vd} = v_o/d$ and $G_{id} = i_L/d$ are represented up to their Nyquist frequency (indicated by a black vertical line), which is the range of the validity of the model. The continuous model is also represented for comparison purposes. In order to do a first verification of the proposed discrete model the discretization of the continuous model is carried out at a sample frequency $f_{samp} = 25\ kHz$ using the impulse-invariant discretization at $f_{samp} = 100\ kHz$ followed by a down-sampling of the discrete model using a Zero Order hold method. This allows to have a model valid up to $f_{Nyq} = 12.5\ kHz$. This procedure is based on the derivation of the equivalence between the discrete-time modeling and the impulse-invariant discretization in [4], where it is assumed that the control action is a series of Dirac pulses, each one per switching and sampling period. However, in our case we have a series of n_{sub} Dirac pulses, one per switching cycle, in a sampling period. As shown in Fig 5, traces labeled as Discretized are coincident with the results issued from the proposed model for $n_{sub} = 4$.

In order to asses the performance degradation of sub-sampling, Fig 6 shows the difference between the frequency response of the models taking as reference the case of $n_{sub} = 1$. The main effects of sub-sampling are an additional phase loss (or drop) and obviously the shift of the effects around the Nyquist rate. The higher the sub-sampling rate (or the number of periods between samples) the higher the phase loss. This can be specially relevant for the tuning of
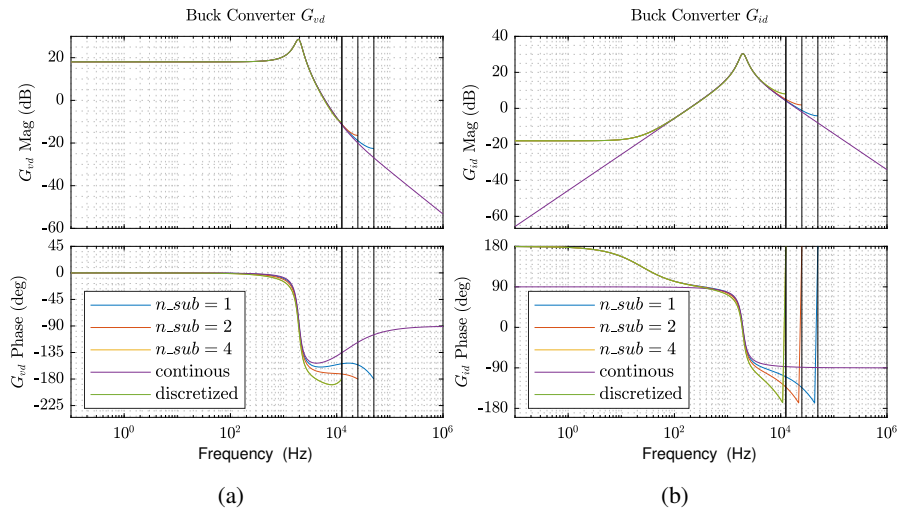

(a)   (b)

Fig. 5: Comparison of the discrete models of a buck converter with different n_{sub}: (a) Transfer function G_{vd} , (b) Transfer function G_{id}
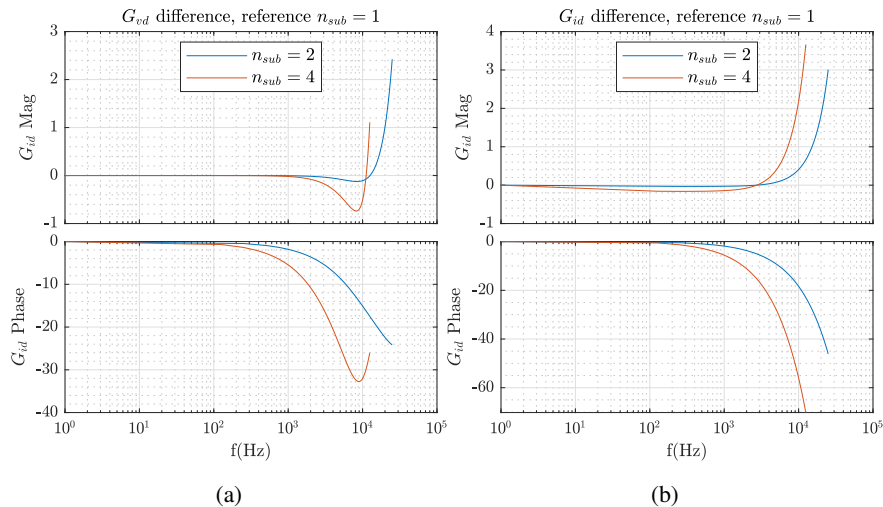
Fig. 6: Performance degradation for buck converter with different n_{sub}: (a) Difference in transfer function G_{vd} taking as reference $n_{sub} = 1$, (b) Difference in transfer function G_{id} taking as reference $n_{sub} = 1$

compensator in closed loop operation when a tight phase margin is specified. So, a regulator will have to either provide a bigger phase boost at the desired cut-off frequency, or, if it is above the phase boosting capabilities of the regulator, the cut-off frequency shall be lower in order to have the same phase margin.

Finally, PSIM simulations were compared to the models to verify the proposed sub-sampling models. The converter used as example has been simulated in buck and boost mode, i.e., reversing the power flow. Thus, models corresponding to buck and boost converter have been verified. The Bode plots on Fig. 7 shows both simulated and model responses. It can be seen how there is a strong match between the model and the simulation, being the biggest discrepancies placed near the Nyquist frequency. Differences in magnitude and phase plotted in Fig. 8 are very small and mainly due to the simulation accuracy, verifying the proposed approach to calculate the discrete time models under sub-sampling conditions.

III. EXPERIMENTAL RESULTS

In order to further verify the model, a synchronous bidirectional buck converter was used along an Systems on Chip (SoC) based identification method to obtain the converter frequency response. The power converter was used in both directions, allowing for checking buck and
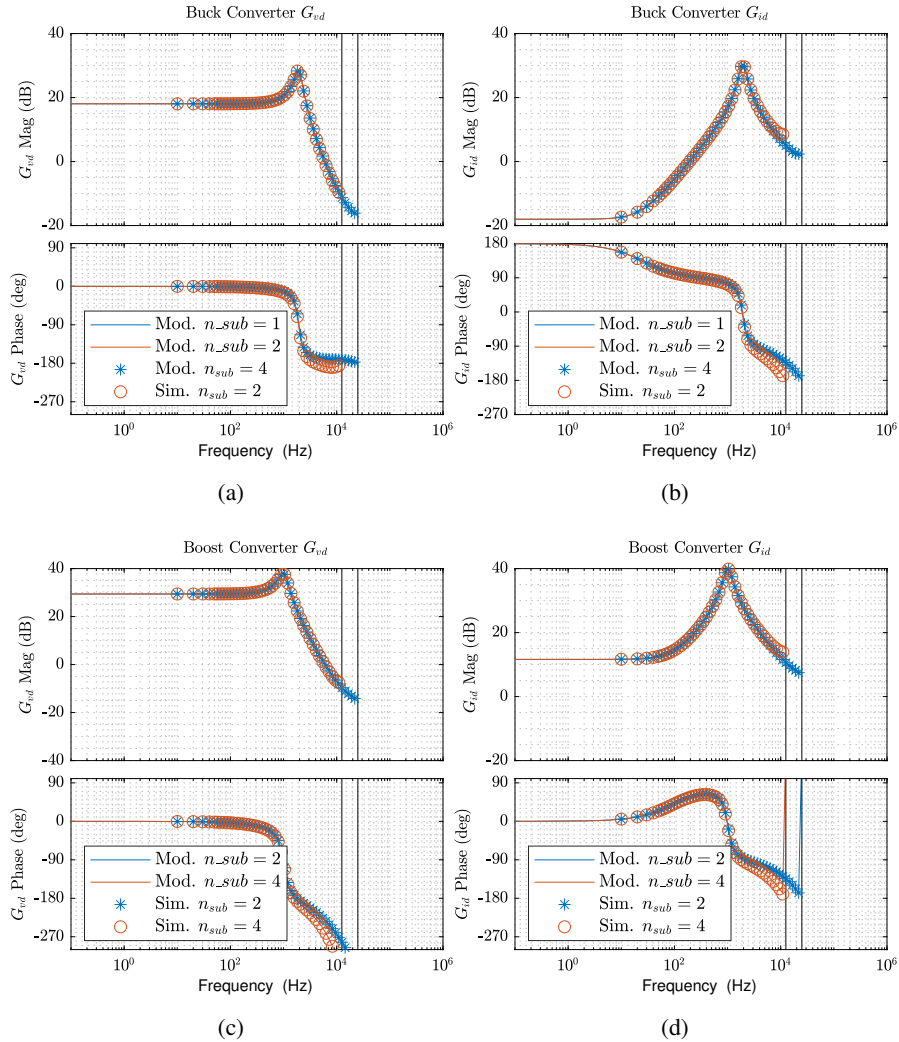
Fig. 7: Validation of the discrete models with simulations for different n_{sub}: (a) Transfer function G_{vd} buck converter, (b) Transfer function G_{id} buck converter, (c) Transfer function G_{vd} boost converter, (d) Transfer function G_{id} boost converter.

boost converter behavior. The experimental set-up can be seen in Fig. 9. The SoC generates the PWM signals of the converter. The duty cycle signal has a DC value plus an AC perturbation based on an pseudorandom binary sequence (PRBS) [14]. The output voltage is digitized via an analog to digital converter (ADC) and stored in the microprocessor part of the SoC. Fast Foutier Trasnform (FFT) is applied to the input and output signals, and finally fractional smoothing is used to calculate the output voltage transfer function, G_{vd}. Note that this measuring method relates the samples of the control signal (duty cycle) and samples of the output voltage.
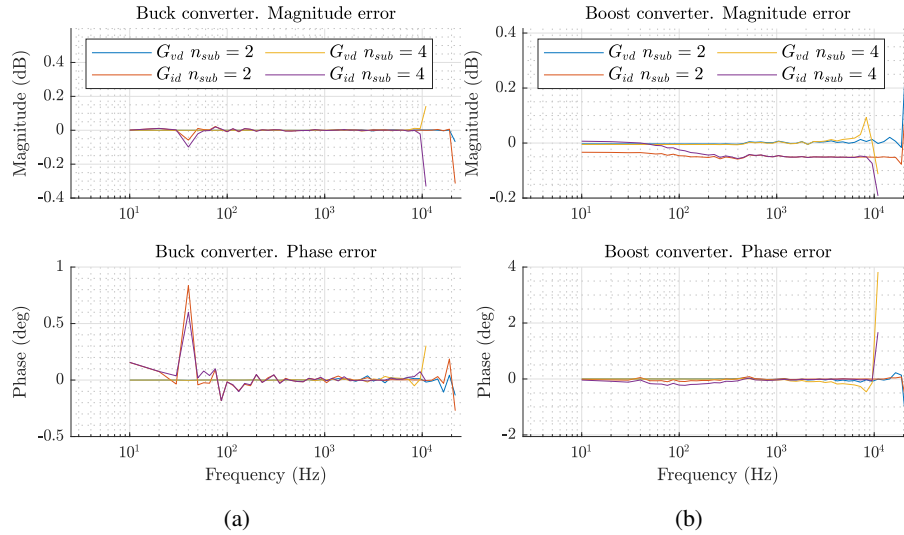
Fig. 8: Error between proposed model and simulations: (a) buck converter,(b) boost converter

The elements of the power converter are $L = 64.6 \ \mu H$ with a parasitic resistance of $r_l = 127 \ m\Omega$. The output capacitor acting as a buck converter is $C_1 = 104 \ \mu F$ with a parasitic resistance $r_{c1} = 110 \ m\Omega$ while in the boost converter operation is $C_2 = 95 \ \mu F$ with a resistance $r_{c1} = 56 \ m\Omega$. The matrices $\mathbf{A_1}, \mathbf{A_0}, \mathbf{B_0}, \mathbf{B_1}, \mathbf{C_0}$, and $\mathbf{C_1}$ were selected accordingly to the
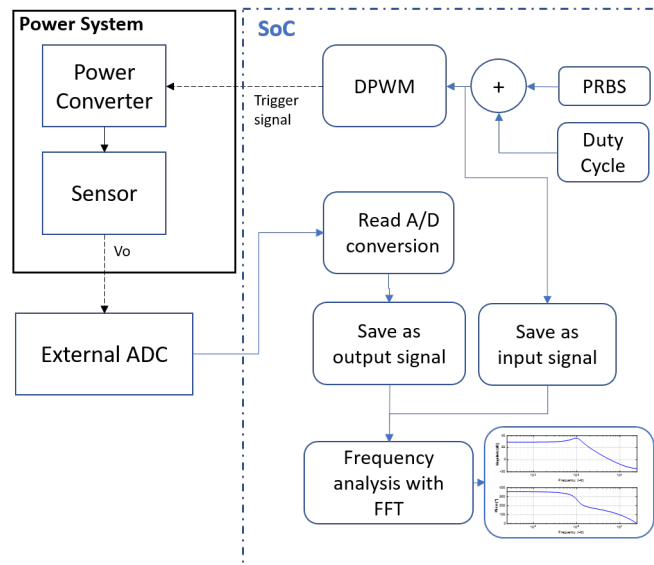

Fig. 9: Experimental set-up

operation mode, buck or boot. Switching frequency was set to $f_s = 100 \ kHz$. The input voltage $V_g = 8 \ V$ and the load was set to $R_{load} = 2.1 \ \Omega$ for the buck converter and $R_{load} = 14.6 \ \Omega$ for the boost converter. The duty cycle was in both cases $D = 0.5$.

(a) buck converter $n_{sub} = 1$

(b) boost converter $n_{sub} = 1$

(c) buck converter $n_{sub} = 2$

(d) boost converter $n_{sub} = 2$

(e) buck converter $n_{sub} = 4$
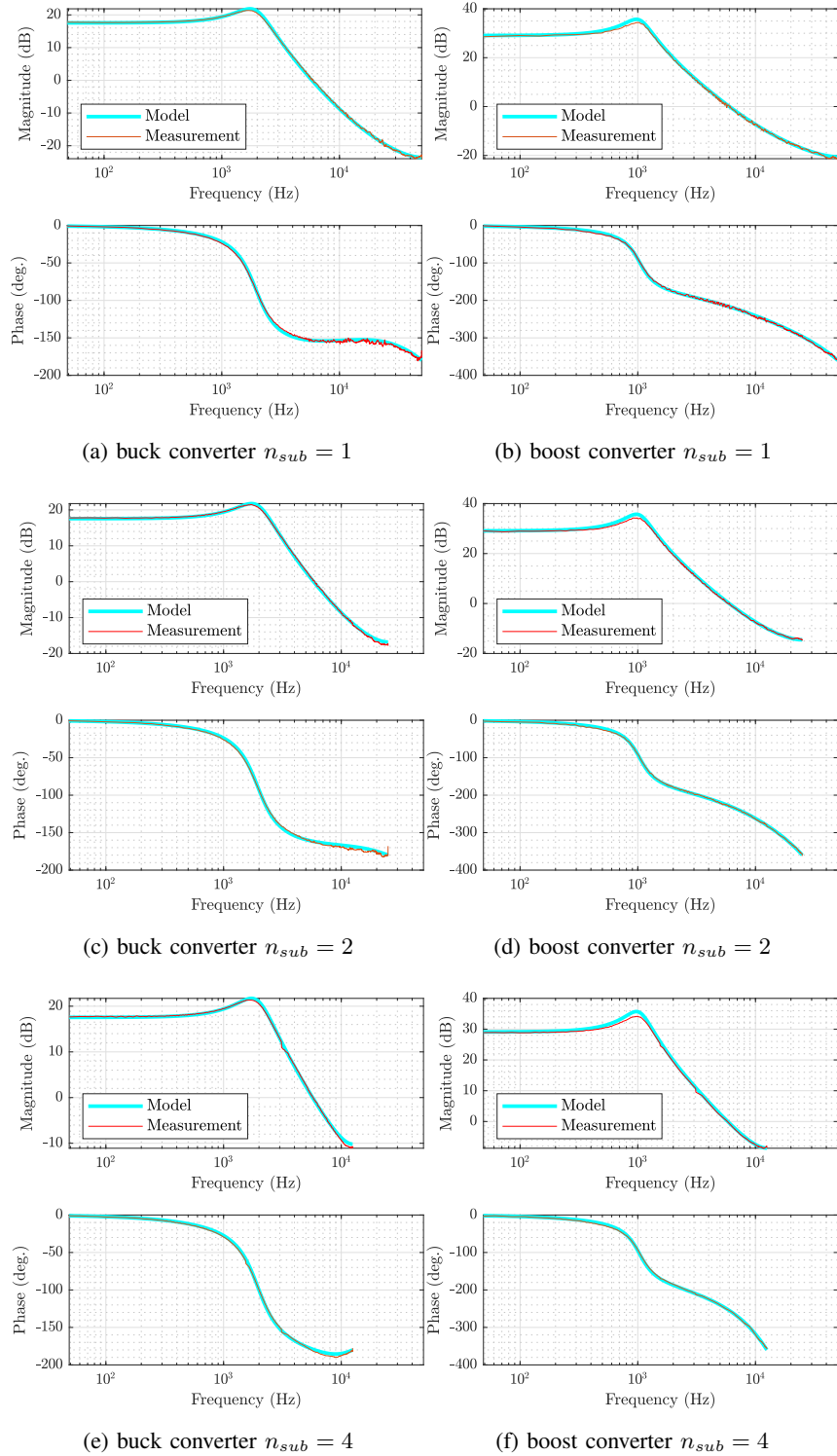
(f) boost converter $n_{sub} = 4$

Fig. 10: Model (blue) and experimental (red) Bode plots. Same power stage, operating as a buck converter (a),(c) and (e), and boost converter (b),(d) and (f).

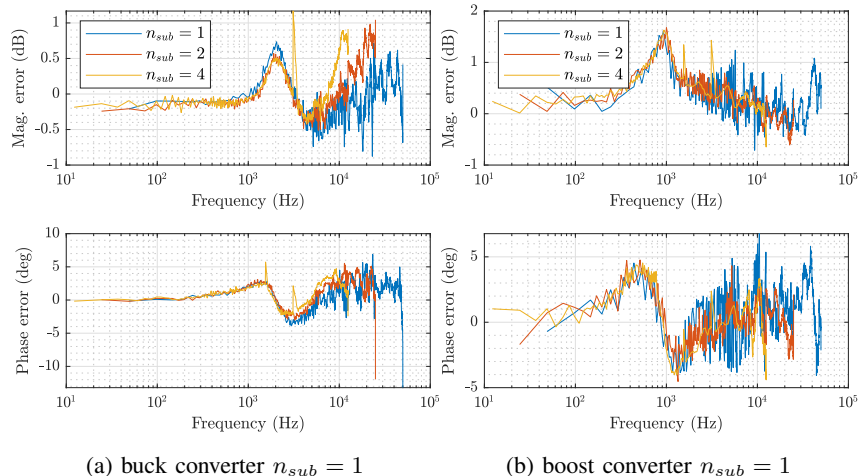(a) buck converter $n_{sub} = 1$ (b) boost converter $n_{sub} = 1$

Fig. 11: Error between model and measurement (a) buck converter and (b) boost converter.

Comparison between the theoretical Bode plot and the measured ones for the prototype with different sub-sampling values and converter topology is provided in Fig. 10 considering the transfer function $G_{vd} = v_o/d$. In the case of $n_{sub} = 1$, the frequency range was set between $f_{min} = 48.82 \ Hz$ and the Nyquist frequency $f_{max} = f_{Nyq}$. Frequency range limits f_{min} and f_{max} are divided by the factor n_{sub} for the other cases. Results are presented for the buck mode for $n_{sub} = 1$ in Fig. 10a, for $n_{sub} = 2$ in Fig. 10c and for for $n_{sub} = 4$ in Fig. 10e. Same cases for the boost mode are shown in Fig. 10b for $n_{sub} = 1$, Fig. 10d for $n_{sub} = 2$ and Fig. 10f for $n_{sub} = 4$. Form the Fig. 10, it can be seen how there is a significant match between the theoretical and the experimental ones. In Fig. 11 the error between model and measurement is plotted for the magnitude and the phase. In terms of magnitude, the error is within the interval $[-1 \ dB, 1 \ dB]$ for the buck converter and $[-1 \ dB, 2 \ dB]$ for the boost converter. In the case of the phase, the differences are within the interval $[-5 \ deg., 5 \ deg.]$ for the buck and boost converter, excluding the point close to the Nyquist frequency. As in case of magnitude, the main differences of phase are in the nearby of natural frequency and at high frequency. It is considered a good agreement between model and measurements. There is no significant differences in the error for the different sub sampling factors.

IV. CONCLUSIONS

This paper develops an extension of the small-signal discrete time model presented in [3], [4] addressing the sub-sampling case, in which several complete switching cycles take place

between the samples used to control the converter. Analytical derivation for the case of a trailing-edge, leading edge and symmetrical pulse width modulators have been presented. The proposed approach can be applied to any type of power converters with fixed switching frequency knowing the corresponding description in the state space.

Extensive verification of the model has been provided both with simulations and experimental measurements using a buck and boost converters. Fairly good agreement between theory and measurements or simulation results have been demonstrated. Lab measurements accounts for differences of $\pm 1\,dB$ in magnitude and $\pm 5\,deg$ for the buck converter and less than $\pm 2\,dB$ and $\pm 5\,deg$ for the boost converter. Simulation results exhibits a closer match.

Although the most common solution is to have no sub-sampling, and from a dynamic point of view this is a better solution, the proposed small-signal analytical model under sub-sampling conditions can be used for tuning a regulator for the converter, assessing the degraded dynamic response or applying parametric identification. As seen in section II-B and III the model reveals an additional phase drop at relatively lower frequencies when using sub-sampling.

The findings provided by the model will be of interest in the application of digital control platforms with low performance such a low-cost micro-controller, low range FPGA or ASICs. Space power converters are an example of potential benefit due to the significant hardware restrictions due to the low availability of radiation tolerant digital hardware compared with its terrestrial counterpart. Low-power application, such as IoT devices, can also benefit from sub-sampled control.

REFERENCES

[1] R. Erickson and D. Maksimovic, *Fundamentals of Power Electronics*. Power electronics, Springer US, 2001.

[2] D. M. V. de Sype, K. D. Gusseme, A. R. V. den Bossche, and J. A. Melkebeek, "Small-signal z-domain analysis of digitally controlled converters," in *2004 IEEE 35th Annual Power Electronics Specialists Conference (IEEE Cat. No.04CH37551)*, vol. 6, pp. 4299–4305 Vol.6, June 2004.

[3] D. Maksimovic and R. Zane, "Small-signal discrete-time modeling of digitally controlled pwm converters," *Power Electronics, IEEE Transactions on*, vol. 22, no. 6, pp. 2552–2556, 2007.

[4] L. Corradini, D. Maksimović, P. Mattavelli, and R. Zane, *Digital Control of High-Frequency Switched-Mode Power Converters*. IEEE Press Series on Power Engineering, Wiley, 2015.

[5] L. Scandola, L. Corradini, and G. Spiazzi, "Small-signal modeling of uniformly sampled phase-shift modulators," *IEEE Transactions on Power Electronics*, vol. 30, pp. 5870–5880, Oct 2015.

[6] L. Corradini and P. Mattavelli, "Modeling of multisampled pulse width modulators for digitally controlled dc-dc converters," *IEEE Transactions on Power Electronics*, vol. 23, pp. 1839–1847, July 2008.

[7] Z. Lukić, A. Radić, A. Prodić, and S. Effler, "Oversampled digital controller ic based on successive load-change estimation for dc-dc converters," in *2010 Twenty-Fifth Annual IEEE Applied Power Electronics Conference and Exposition (APEC)*, pp. 315–320, Feb 2010.

[8] S. Effler, Z. Lukic, and A. Prodic, "Oversampled digital power controller with bumpless transition between sampling frequencies," in *2009 IEEE Energy Conversion Congress and Exposition*, pp. 3306–3311, Sept 2009.

[9] Z. Liu, Z. Huang, F. C. Lee, and Q. Li, "Digital-based interleaving control for gan-based mhz crm totem-pole pfc," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 4, pp. 808–814, Sept 2016.

[10] Z. Lukic, N. Rahman, and A. Prodic, "Multibit $\Sigma\Delta$ pwm digital controller ic for dc-dc converters operating at switching frequencies beyond 10 mhz," *IEEE Transactions on Power Electronics*, vol. 22, pp. 1693–1707, Sept 2007.

[11] J. Morroni, A. Dolgov, M. Shirazi, R. Zane, and D. Maksimovic, "Online health monitoring in digitally controlled power converters," in *2007 IEEE Power Electronics Specialists Conference*, pp. 112–118, 2007.

[12] M. Al-Greer, M. Armstrong, M. Ahmeid, and D. Giaouris, "Advances on system identification techniques for dc–dc switch mode power converter applications," *IEEE Transactions on Power Electronics*, vol. 34, no. 7, pp. 6973–6990, 2019.

[13] G. M. Buiatti, J. A. Martín-Ramos, C. H. Rojas Garcia, A. M. R. Amaral, and A. J. Marques Cardoso, "An online and noninvasive technique for the condition monitoring of capacitors in boost converters," *IEEE Transactions on Instrumentation and Measurement*, vol. 59, no. 8, pp. 2134–2143, 2010.

[14] M. Shirazi, J. Morroni, A. Dolgov, R. Zane, and D. Maksimovic, "Integration of frequency response measurement capabilities in digital controllers for dc-dc converters," *IEEE Transactions on Power Electronics*, vol. 23, pp. 2524–2535, Sept 2008.