Analysis and design of a latching current limiter based on a SiC N-MOSFET

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***Abstract*: Latching current limiters (LCLs) are circuits used for electrical load control on spacecrafts. They provide enhanced current protection, improving reliability. Traditional implementations often used P-MOSFETs as the main current limiter device. However, new wide bandgap materials (WGB) offer the possibility to operate at higher voltages and, allegedly, temperatures. This work presents a complete architecture for a LCL based on a SiC N-MOSFET. The main parts of the architecture with the basic design guidelines are shown. Finally, experimental results for a class 10 LCL, using the proposed architecture is displayed, for bus voltages of 100 V.**

***Keywords*: LCL, SiC, Wide bandgap devices.**

I. Introduction

Solid-state current limiters are commonly used in satellites to manage electrical loads in a reliable way. In European spacecrafts, these switches are usually known as Latching Current Limiters (LCLs). LCLs task is twofold. First, they allow the connection and disconnection of the loads by telecommand. Second, they protect the power bus against over-currents from the said loads. Inside the satellite regulated power bus scheme, LCLs are in the distribution system, just between the main power bus and the secondary power bus (Fig. 1).

LCLs can be seen as intelligent switches. In normal operation, the LCL allows the current demanded by a load to flow if it is below a pre-established limit. If the current is higher than this limit, the LCL will regulate it to this said limit value, during a specific time. This regulation is achieved by having a transistor (or transistors) working in linear mode regulating the current and withstanding a significant voltage (i.e. bus voltage). Thus, the transistor will be dissipating a lot of power which rapidly increases its temperature. If the current does not naturally go below the limit in this predefined time, the LCL will isolate this load disconnecting it form the satellite power bus.

Traditional LCL architectures are based on the use of P-MOSFETs, dud to the easiness to control them. Basically, the source terminal is connected directly to the bus voltage, and it is only necessary to put a lower voltage level on its gate terminal. High power buses on satellites run at 100 V – 120 V. However, P-MOSFETs usually present a worse channel resistance (R_{dson}) than N-MOSFETs for the same voltage and current ratings. As the power demanded by load increases, the conduction losses on P-MOSFETs increase as well. Then, in order to increase the efficiency of the system, it would be interesting to replace them by N-MOSFETs, which in general, present lower R_{dson} values.

In an LCL based on N-MOSFETs, the drain would be connected to the bus and the source will be connected to the load side.

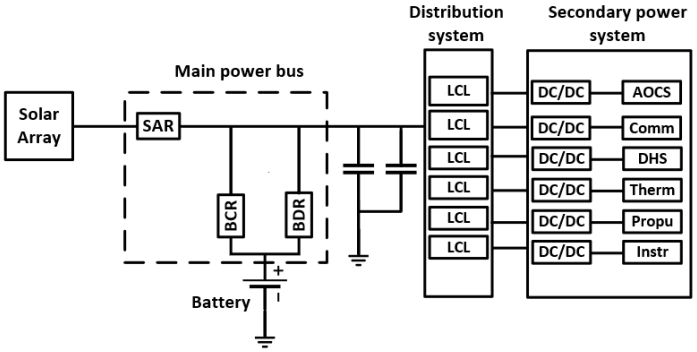


Fig. 1. Regulated power bus in a satellite

The main problem with these transistors is related to the control, as it is necessary to have a gate voltage higher than the source voltage. Therefore, it is mandatory to have a stage capable of transferring the control signal referred to the source of the device. With the advent of power semiconductor technologies based on wide bandgap materials (WBG), especially Silicon Carbide (SiC) and Gallium Nitride (GaN), it is possible to use transistors based on these materials, acting as current limiter devices. The WBG materials also provide the possibility to work at higher voltages and, allegedly, higher temperatures thus reducing the risk of failure due to high junction temperature. In literature, some works [1],[2] regarding LCL topologies based on SiC N-MOSFETs, have been proposed studying some interesting aspects related to the driving circuit, semiconductor selection, and auxiliary power supply.

Going on with this line, the aim of this work is to present the architecture of an LCL based on a SiC N-MOSFET. The design includes an auxiliary power supply, the current control loop implementation, a stage called “analog isolator (DCX)”, which is in charge of providing the gate-source isolated control signal of the N-MOSFET, the timer that will hold the LCL in current limitation for a predefined time, and an undervoltage lockout section (UVLO) to prevent the LCL activation on low bus voltage level.

This article is organized as follows. Section II describes the SiC semiconductor selection process. Section III presents the SiC based LCL architecture, describing the main stages. Experimental results for the designed SiC based LCL prototypes are displayed in Section IV. Finally, the main conclusions to this work are shown in Section V.

II. SEMICONDUCTOR SELECTION

The aim of this section is to select a SiC transistor, either MOSFET of JFET, capable of performing the tasks of the switch of an LCL under the space requirements recorded in [3] and [4]. A set of SiC devices have been preselected and evaluated using theoretical models. The analysis performed in this section aims to verify that the temperature reached by the junction of the devices, working under LCL operation, remains within the device limits with the security margins presented in [4]. These tests are performed under the different LCL classes defined in [3]. LCLs are normally divided in classes according to their maximum operational (normal) current.

This way, a class 10 LCL can drive 10 A as nominal current. The limitation current is stablished for each LCL between 10% and 40% more than the nominal current [5]. Fig. 2 shows the LCL current profile used for calculating the power dissipation under an overload event. Initially, the LCL carries the class current (nominal current), under a short-circuit there is an overshoot which is assumed to be 50 A [3] regardless of the class. This peak is held for the maximum overshoot recovery time of 300 µs [3]. Finally, the maximum limitation current will be held for the maximum trip-off time. This trip-off time depends on the LCL class, being 20 ms for a class 1 LCL and 3 ms for a class 10 LCL. The selection of the transistors has been made considering the availability of the devices and the power dissipation. Despite being intended for space applications, no radiation hardening considerations have been made. The most common SiC transistor has a breakdown voltage of 1200 V and current of several tens of amps, which is much bigger than the spacecraft applications. It is necessary to remind that in LCL applications, the limiting device must withstand power in linear mode for several milliseconds. Therefore, the semiconductors that allow the highest power dissipation in linear mode have been pre-selected. Considering the brief times (i.e. trip-off time) in which the device is limiting the current, the use of thermal heat sinks has not been considered, since the thermal behaviour will be dictated by the transient thermal impedance between the junction and case. The use of radiators will improve the thermal impedance between the case and the exterior but not the one between the junction and the case.

Attending to the maximum junction temperature, most of the devices are rated for a temperature of 150ºC, but there are some exceptions which are rated for 175ºC and 200ºC. Regarding JFETs, they would be, in principle, better suited for working as a current limiter than MOSFETs [6], especially due to its better capability to operate in linear mode. However, they are normally-ON devices. This aspect about JFETs may compromise the capability of the LCL to act as a switch. Without power at the gate, the load will be connected to the power bus, so during the turn ON process, all the loads protected by LCLs will be demanding power to the main bus. This may comprise the correct start-up and the failure recovery. To select among the different transistors two different criteria have been considered. First, the maximum junction temperature will be analysed in order to select the devices that can withstand the power dissipation requirements for LCL applications. The second criterion is based on the dissipation under nominal operation (i.e. without limiting the current). Therefore, the best device will be the one that under current limitation it does not exceeds its junction temperature limit and at the same time it presents the lowest losses under nominal operation. These temperature limits must comply with the requirements in [4]. The worst dissipation case happens when a short-circuit is applied at the output of the LCL, making the current limiter device withstands the full voltage of the power bus.

Power dissipation and junction temperature test:

The test is derived from the current transient response specified in [3]. The analysis is performed using the current profile shown in Fig. 2 (which is not represented to scale). With this test it is possible to assess the temperature reached by the junction of the selected semiconductors:

1. Prior to the short-circuit and the current overload, the FET is in ohmic mode conducing the class current (i.e. nominal current). In this step, the transistor is dissipating the power determined by (1), where R_{ON} is the ON state resistance of the SiC transistor, defined in the datasheet, and I is the class current. This dissipation, together with the thermal impedance of the device, will be used to determines the initial temperature of the junction T_{j_start}.
$$P_{dis\_nom} = R_{ON} \cdot I_N^2 \quad (1)$$
2. During the maximum overshoot recovery time, the switch will be carrying 50 A [3] and it will be assumed that the device is in ohmic mode; therefore, the dissipated power will be determined by (2).
$$P_{dis\_overshoot} = R_{ON} \cdot 50^2 \quad (2)$$
3. During the rest of the maximum trip-off time the FET will be in active mode withstanding the full bus voltage. Then, the dissipated power follows the equation (3), where I_{lim} Is the maximum limitation current.
$$P_{dis\_linear} = V_{bus} \cdot I_{lim} \quad (3)$$
4. At this point, it is possible to determine the temperature rise T_{j_rise}, using the transient thermal impedance of the device and the power profile represented in Fig. 3 with the values of (2) and (3). With T_{j_start} and T_{j_rise} it is possible to obtain the value of the maximum junction temperature (T_{j_max}) according to (4):
$$T_{j\_max} = T_{j\_start} + T_{j\_rise} \quad (4)$$

According to the LCL classes defined in [3], the worst cases will be LCL classes 10 and 8, because they are the ones with the higher-class currents (8 A and 10 A respectively) and the higher maximum limitation currents (11.2 A and 14 A, respectively). With this analysis and the LCL current profile shown in Fig. 2, it is possible to establish the power dissipation profile shown in Fig. 3. The maximum temperature allowed for a transistor in space applications is defined in [4]. It is stated that the maximum junction temperature is 110ºC, or the maximum temperature specified on the semiconductor device minus 40ºC, whichever is lower. However, it is assumed that an LCL will only trip-off once in its lifetime and then the device limit temperature can be reached. This also helps to exploit the advantages of higher temperature devices such as the 200ºC and 175ºC selected MOSFETs. Hence, for this study the maximum temperature allowed will be the one of the devices minus 40ºC, to have a safety margin. To assess which would be the best device, the constant dissipation under nominal current operation has been analysed for the selected semiconductors. This analysis shows that the devices with lower power dissipation under nominal conditions are the SCT3022AL, the SCTW90N65G2V, the C2M0040120D and C2M0045170P. These devices dissipate 2.2 W, 2.4 W, 4 W and 4.5 W respectively, carrying 10 A. For the stress defined by a class 10 LCL and 100 V bus voltage, the transient thermal response of the devices with 150 ºC limit are presented in Fig. 4 a), the ones with 175ºC are presented in Fig. 4 b), and finally Fig. 4 c) represents the ones with 200ºC limit.

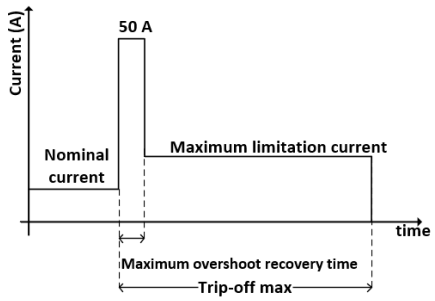


Fig. 2. Current profile for thermal simulation

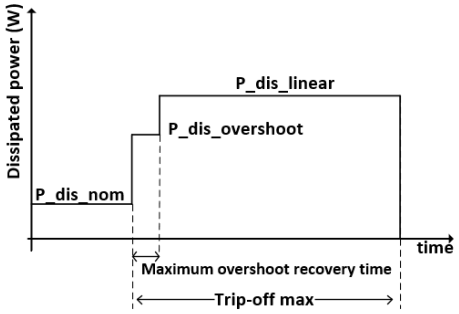
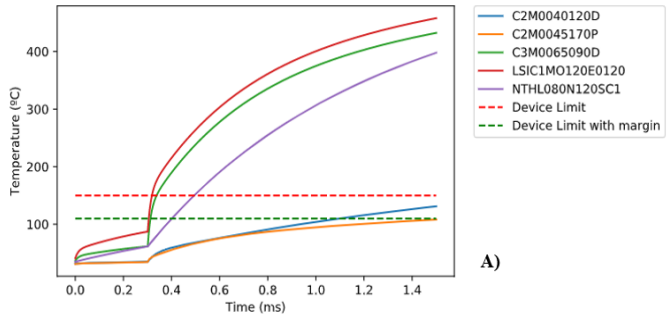
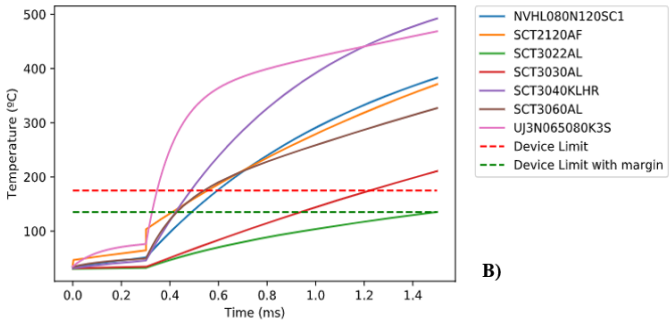


Fig. 3.Power dissipation under short-circuit

The safety temperature limit (device - 40ºC) is also represented for all cases. Regarding this analysis, it is important to remark that the temperature limit must not be exceeded in the trip-off time specified for each class. For a class 10 LCL the minimum trip-off time is 1.5 ms and the maximum is 3 ms. Only the SCTW90N65G2V [7] complies with the safety limit in 3 ms. However, the SCT3022AL [8] complies with the safety limit for the trip-off minimum time, and it is the one that presents the lowest dissipation losses (i.e. 2.2 W). Therefore, two LCL prototypes, with the same architecture, have been built using these two SiC N-MOSFETS. Experimental results, regarding this junction temperature analysis, are very difficult to get for such short times in the milliseconds range. There are some specific techniques [9], [10] that require decapsulating the MOSFET which are not feasible in this work.





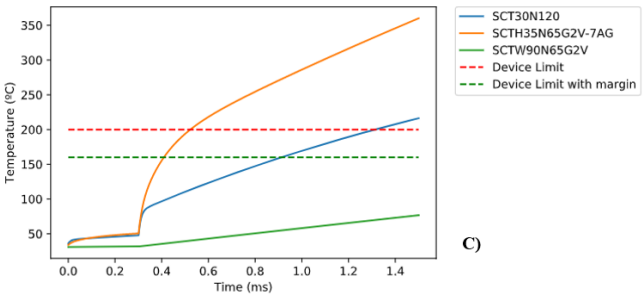


Fig. 4. Thermal response a) 150ºC, b)175ºC and c) 200ºC

III. LCL ARCHITECTURE

The complete LCL architecture proposed in this work is shown in Fig. 5. Being a space application, all these stages are implemented in an analog way using discrete components with rad-hard equivalents. All the circuitry needed by the LCL (the auxiliary power supply, the current sensor, the current control loop, the analog isolator, the flip-flop that controls the LCL state, the timer section and the undervoltage lockout) is supplied between the bus voltage and an additional voltage level which will act as the reference for the control circuitry. The voltage between the bus and this additional level will be V_{supply}. This is done to comply with the requirements of the current sensor [11] for the maximum allowed voltage between power and sensing terminals, regardless the bus voltage. This way, the design has been tailored to 100 V – 150 V. This design is based on [2] and [12]. The main drawback is that the reference voltage for all the circuitry is not the satellite power bus, but the source terminal of the P-MOSFET in the auxiliary power supply (control reference). In this regard, special care has to be taken with the elements that interact directly with the power bus, such as the UVLO and the timer sections, which are referenced to the main power bus reference.

A. *Auxiliary power supply*

The power to all the circuitry in charge of driving the N-MOSFET is supplied through a linear power supply formed by a P-MOSFET, a TL431 circuit and a resistor. The voltage of this supply (i.e. V_{supply}) is selected by the TL431 circuit which fixes the gate-source voltage of the P-MOSFET. This MOSFET drives all the current demanded by the control circuitry of the LCL and withstands the difference between the bus voltage (V_{bus}) and V_{supply}. The source terminal of this P-MOSFET generates the aforementioned voltage level. Special care must be taken with the P-MOSFET selection, since as V_{bus} increases, the power dissipation over this MOSFET increases as well. In this case, for a V_{bus} of 100 V and 15 V of V_{supply}, the P-MOSFET is withstanding 85 V and the dissipated power for this transistor is about 0.5 W.

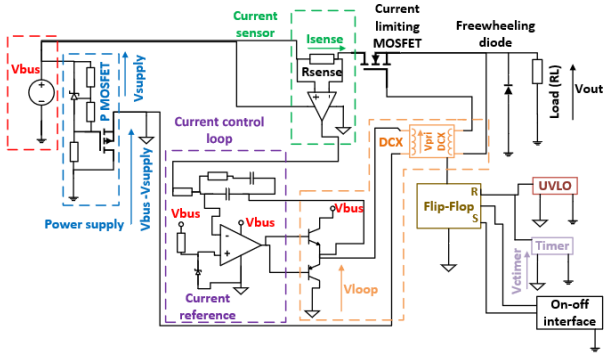


Fig. 5. LCL architecture

B. *Analog isolator (DCX)*

As it was mentioned in Section I, the DCX is the stage that translates the control signal from the current control loop to the N-MOSFET gate-source voltage, controlling this way, the LCL activation. In this way, the limiter MOSFET operates in ohmic zone when the measured current is lower than the preestablished limit, and in active zone when it is necessary to regulate the current at the current limit. This analog isolator will be based on a DC/DC isolated converter working in open loop. This DC/DC converter is designed so its dynamic response does not interfere excessively with the dynamic of the current control loop. For this reason, it operates at a switching frequency of 4 MHz. The control of the DCX output voltage is carried out through the variation of its input voltage performed by the current control loop. The implementation of the DCX stage has been carried out using two topologies, one based on the use of a class DE converter and other one based on a half bridge LLC. A detailed description of the analysis and implementation of the DCX stage using these two topologies is presented in [13]. For the experimental results of the LCL presented in this work, only the LLC-DCX topology was used. A brief design process will be shown here for the ease of the reader. Fig. 6 shows the LLC-DCX topology formed by a half-bridge inverter and a full wave rectifier. It is a resonant topology where it is possible to achieve magnetic integration, thus using the leakage inductances of the magnetic transformer (L_{lk}) as the resonant inductances in the converter. The DCX is integrated in the current control loop, making necessary a precise gain control between the input and the output voltage. DCX designs have been adjusted to get a static gain with a predefined value, so when the control loop output voltage is at its maximum value the gate-source voltage to the current limiting MOSFET is also at its safe maximum. Thus, lowering its R_{ON}. The design of the DCX stages have been made using the First Harmonic Approximation (FHA).

The FHA analyses the resonant network behavior assuming that the circuit is selective enough to make that only the first harmonic can pass through it [14]. In the DCX topologies presented in this work, the half bridge output voltage (V_{bridge}) presents a square form with a duty cycle D, close to 0.5, a low level of 0 V and a high level of V_{in}. This way, the Fourier expression for V_{bridge} is the one shown in (5).

$$V_{BRIDGE} = V_{in} \cdot D + \sum_{k=1}^{\infty} \frac{2}{k \cdot \pi} \cdot V_{in} \cdot sin(k\pi D) \cdot cos(kD\omega_s t) \quad (5)$$

Therefore, the first harmonic amplitude (A_{FH}) will be the one described in (6), being maximum for a D of 0.5 (7):

$$A_{FH} = \frac{2}{\pi} V_{in} \cdot sin(\pi D) \quad (6)$$

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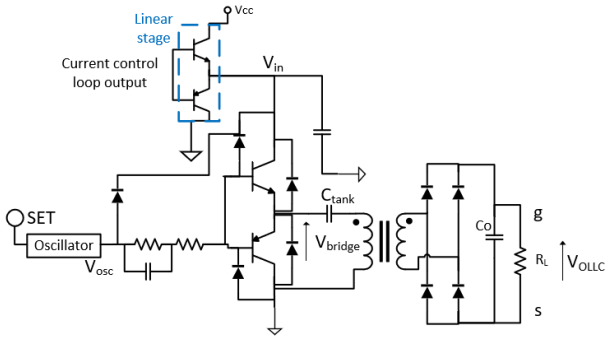

Fig. 6. LLC – DCX circuit diagram

Fig. 7 shows the circuit diagram of the LLC-DCX converter under the FHA in order to analyze the resonant network behavior (Z_{tank}) when a sinusoidal input is used. R_{p1} and R_{p2} are used to model the loses resistor in both transformer windings. Furthermore, as it is possible to achieve magnetic integration, the resonant inductance for the class D inverter will be the leakage inductance, L_{lk1}. The design process is based on choosing the resonant frequency of the network formed by C_{tank} and L_{lk1}. Expression (8) shows the equivalent impedance (Z_{tank}) of the resonant network.

$$Z_{tank} = j \cdot \left(\omega_S \cdot Llk_1 - \frac{1}{\omega_S \cdot C_{tank}}\right) \quad (8)$$

Where $\omega_s = 2\pi \cdot F_{sw}$ is the angular frequency for the switching frequency (F_{SW}). Regarding the full wave rectifier, the input equivalent impedance is described in [15], and its use appeared in the LLC design process manuals [16]. Having an output capacitor (C_o) bigger enough to eliminate the ripple at the switching frequency, this full wave rectifier behaves as a resistor (R_{iLLC}) described in (9).

$$R_{iLLC} = \frac{8}{\pi^2} \cdot R_L \quad (9)$$

Where R_L is the load resistor in the LLC-DCX topology. It is a rectifier topology without voltage gain. Therefore, the voltage gain for this analog isolator topology will be based on the resonant network voltage gain ($G_{tankLLC}$). This R_{iLLC} can be used to choose the quality factor (Q_{tank}) of the resonant network at the resonant frequency (10).

$$Q_{tank} = \frac{\left(\frac{F_R}{F_{SW}}\right) \cdot \omega_s \cdot Llk_1}{R_e} \quad (10)$$

$$R_e = R_{iLLC} + Rp_2 + Rp_1$$

Where F_R/F_{SW} is the ratio between the resonant frequency from C_{tank} and L_{lk1}, and the switching frequency. The $G_{tankLLC}$ value can be obtained using the expressions (11)-(13).

$$Z_1 = R_{iLLC} + Rp_2 + (j \cdot \omega_s \cdot Llk_2) \quad (11)$$

$$Z_{eq} = \frac{j \cdot \omega_s \cdot Lm \cdot Z_1}{j \cdot \omega_s \cdot Lm + Z_1} \quad (12)$$

$$Gtank_{LLC} = \frac{V_{iLLC}}{V_{FA}} = \left| \frac{Z_{eq}}{Rp_1 + Z_{tank} + Z_{eq}} \cdot \frac{R_{iLLC}}{Z_1} \right| \quad (13)$$

Therefore, knowing the $G_{tankLLC}$ value, it is possible to achieve the final expression for the LLC-DCX gain (14) depending on the $G_{tankLLC}$ and the first harmonic amplitude (A_{FH}). The LLC-DCX gain has been selected near to 1, making easier the current control loop design process.

$$G_{aisolatorLLC} = \frac{V_o}{V_{in}} = \frac{2}{\pi} \cdot sin(\pi \cdot D) \cdot Gtank_{LLC} \quad (14)$$

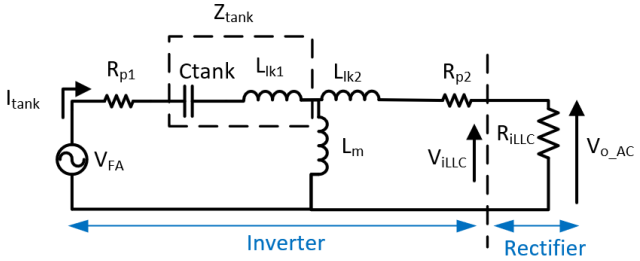

Fig. 7. Equivalent circuit for the LLC-DCX using the FHA

C. Current control loop

This section introduces the control loop design that will regulate the current when the LCL is in limitation mode. The current control loop is based on a Type II regulator. Thanks to its integrator, when the current through the LCL is lower than the limiting value (i.e. the reference of the loop), the loop will saturate to positive putting the maximum gate-source voltage on the limiter N-MOSFET, and thus having the lowest R_{dson} value. If the current measured by the sensor is above the limit, the control loop will reduce its value and thus the gate-source voltage of the MOSFET. This forces the N-MOSFET to operate in linear mode regulating the current. The current control loop will then work so the current sensed is the same as the reference current. For the correct tunning of the regulator, the dynamic of the current sensor, the current source made by the current limiting N-MOSFET and the DCX voltage variations between the input and the output voltage (i.e. audio-susceptibility) must be considered.

The current sensor used in this work was the LT6105 [11] from Linear technologies. Its dynamic behavior has been obtained using, from the vendor provided SPICE simulation model, an AC analysis for frequencies until 1 MHz. After that, a mathematical approximation of the data has been made. This way it is possible to approach the current sensor dynamic behavior using a transfer function (G_{sensor}) composed of 3 poles and 2 zeros. The audio-susceptibility (G_{vo_vg}) has been obtained by measurements of DCX prototypes using a frequency response analyzer [17]. Straightaway, a mathematical approximation of the results has been made for an input voltage of 10 V. Fig. 8 shows the approximation of the experimental data for frequencies until 100 kHz, having a 3dB bandwidth of 20 kHz.

Finally, the current source behavior of the N-MOSFET limiting the current and the impedances seen by the LCL must be considered to model the transfer function (G_{i_uc}) between the DCX output voltage (u_c) and the sensed current (i). Fig. 9 shows the equivalent circuit diagram for the LCL small signal model, and Fig. 10 shows the small signal model between the DCX output and the N-MOSFET of Fig. 9. The limiting transistor is modelled by its parasitic capacitances, its transconductance value (g_m), and the drain-source voltage (u_{ds}) influence in the current sensed. Therefore, the current sensed (i) can be expressed as (15). The value for the transconductance was taken from SPICE simulations with the MOSFET carrying in linear mode the limiting current., since this value was difficult to be extracted from the datasheets. The parasitic capacitances were taken from the curves shown in the device datasheet.

$$\hat{\imath} = g_m \cdot \widehat{ugs} + \widehat{uds} \cdot (1/R_{ds} + s \cdot C_{ds}) \tag{15}$$

As the V_{bus} in the small signal model can be considered as a short-circuit, the u_{ds} voltage can be expressed as (16).

$$\widehat{uds} = -\hat{\imath} \cdot (R_{sense} + Z_{load}) \tag{16}$$

Where Z_{load} models the impedance that the LCL sees as a load. Different load impedances have been tested to define which is going to be the worst case. In case of a short-circuit, the Z_{load} parameter will be zero. The gate source voltage of the N-MOSFET (u_{gs}) can be expressed as (17), where $C_{in} = C_{dg} + C_{gs}$.

$$\widehat{ugs} = \widehat{uc} \cdot \left[\frac{1}{(Zo_{DCX} + R_{gate}) \cdot C_{in} \cdot s + 1}\right] + \widehat{uds} \cdot \left(\frac{Zo_{DCX} \cdot C_{dg} \cdot s}{Zo_{DCX} \cdot C_{dg} \cdot s + 1}\right) \tag{17}$$

Combining (15), (16), (17) and dividing by u_c it is possible to get the expression for the G_{i_uc} (18) transfer function, which relates the DCX output voltage with the current sensed.

$$G_{i\_uc} = \frac{g_m}{(Zo_{DCX} + R_{gate}) \cdot C_{in} \cdot s + 1} + \frac{1}{\frac{1}{(R_{sense} + Z_{load})} \cdot \frac{gm \cdot Zo_{DCX} \cdot C_{dg} \cdot s}{Zo_{DCX} \cdot C_{dg} \cdot s + 1} + \frac{R_{ds} \cdot C_{gd} \cdot s + 1}{R_{ds}}} \tag{18}$$

This way, with G_{sensor}, the DCX audio-susceptibility (G_{vo_vg}) and the dynamic of the N-MOSFET current source (G_{i_uc}), is possible to control the current control loop regulator of the LCL. The current control loop plant to control will be the one described in expression (19).

$$G_{LCL} = G_{sensor} \cdot G_{vo\_vg} \cdot G_{i\_uc} \tag{19}$$

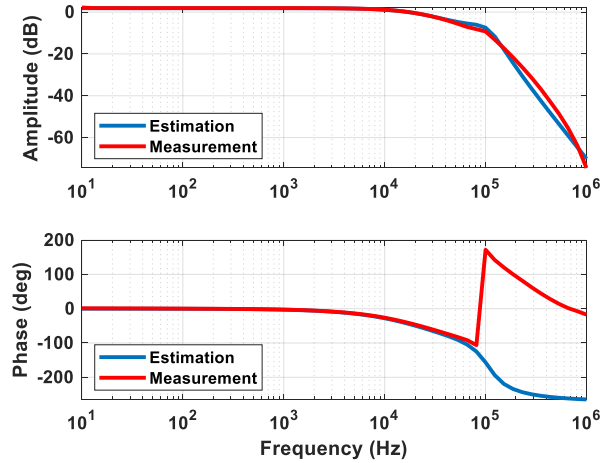

Fig. 8. LLC-DCX audio-susceptibility for an input voltage of 10 V

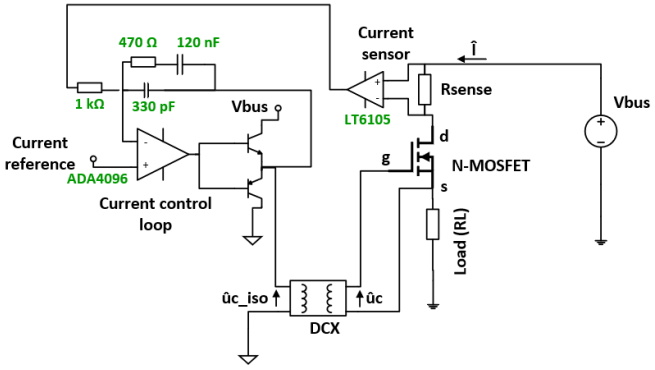

Fig. 9. LLC equivalent circuit for the small signal model

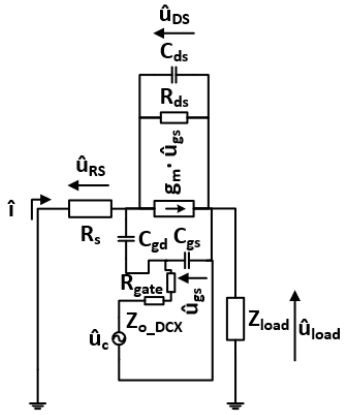

Fig. 10. Small signal model between the DCX output and the N-MOSFET

As it was mentioned, the G_{i_uc} transfer function depends on the load impedance (i.e. Z_{load}). Furthermore, according to the analysis of the G_{i_uc} transfer function, a high Z_{load} is detrimental for the dynamic response. Different Z_{load} representative of realistic situations were introduced in the model to define the worst case. In this work different cases were studied: a pure short-circuit at the output of LCL, a resistor so at the bus voltage carries I_{lim}, a pure inductance, the same inductance in series with the aforementioned resistor, a damped LC filter with a short-circuit at its output, and the same damped LC filter loaded with the aforementioned resistor. The damped LC filter represents the input filter of a DC-DC converter. The filter design process has been adapted from [18], and uses the topology is depicted in Fig. 11 with an L_f = 150 µH, C_f = 150 µF, C_b = 300 µF and R_f = 1.2 Ω. The Bode plot for the G_{i_uc} transfer function is shown in Fig. 12. It can be seen how the worst case happens in the Filter + Resistor case, mainly because is the one the presents the maximum load impedance at the end of the LCL. Fig. 13 shows the bode plot for the current control loop (G_{LCL}) plant defined in (19).

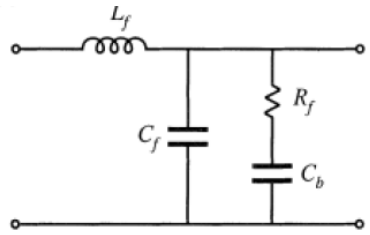

Fig. 11. LC filter design

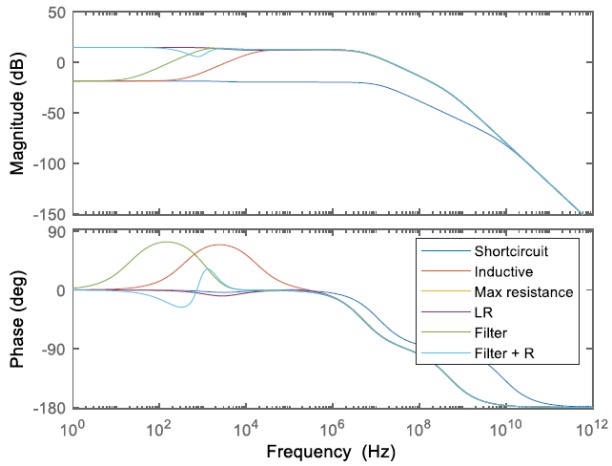

Fig. 12. Bode diagram of the G_{i_uc} transfer function for different Z_{load}

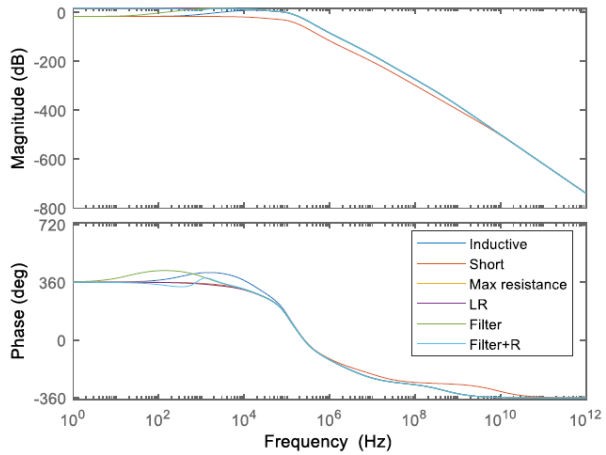

Fig. 13. Bode diagram of the G_{LCL} transfer function for different Z_{load}

D. *Undervoltage Lockout Section (UVLO)*

The undervoltage section prevents the LCL activation in case of a low bus voltage. Furthermore, in case of bus voltage drop it will automatically disconnect the load. Following the specifications in [3] a hysteresis system has been implemented. The main problem that lies with this protection is that the measurement has to be taken directly from the bus voltage, and then the information has to be passed referenced to the control reference. The solution implemented is shown in Fig. 14. It is based on a current mirror. The PNP I transistor is connected between V_{bus} and the bus reference through the R_{mirror_UVLO} resistor, generating the $I_{ref\_mirror\_UVLO}$ current. This current, which is proportional to the V_{bus}, will be mirrored to PNP II collector current, generating the $I_{\_UVLO}$ current. Both, the UVLO and timer sections are connected to a RS flip-flop. Therefore, depending on the NPN_{ref} transistor state, the $I_{\_UVLO}$ current will flow through the R_1 resistor or through the parallel connection between R_1 and R_2 resistors. This resistor is connected to the reference input of the TL431 [19] working as a comparator. This implementation allows the hysteresis in the UVLO section. When the TL431 input voltage is higher than its reference voltage (i.e. 2.5 V), its output voltage saturates to low turning off the NPN_{set} bipolar transistor, connected to the SET terminal of the RS flip-flop. However, if the input voltage level drops below 2.5 V, the NPN_{set} is activated connecting the SET terminal to the control reference. This SET signal is the one that activates the DCX oscillator and hence it controls the LCL activation. This way, when this SET signal is in the low level, the DCX will be turn off, the same as the limiter N-MOSFET.

E. *Timer section*

When the LCL changes from ohmic mode to the active mode to limit the current, a temporization must start. This way when the trip-off time is elapsed the LCL must turn off. This trip-off time guarantees that the semiconductor device has not reached its maximum junction temperature. Traditional LCL architectures have fixed times independent of the limiter device drain-to-source voltage (V_{diff}). In this work, the timer implementation is going to be dependent of the V_{diff} voltage. Fig. 15 shows the circuit diagram for the implemented timer section. It is based on a current mirror. The PNP_{tempI} transistor is connected between the bus voltage, through the R_{g1} resistor, and the N-MOSFET source terminal, through the R_{mirror} resistor. When the V_{diff} voltage is higher than the base-emitter drop voltage, the PNP_{tempI} transistor is in on-state conducing the I_{ref_mirror} current, which will be proportional to the V_{diff} voltage.

This current will be mirrored to the PNP_{tempII} collector current generating the I_{timer} current. This current will be integrated through the RC network formed by the C_{timer} and the resistive divider composed by R_1 and R_2 resistors. This resistive divider is connected to the reference input of a TL431 configured as a comparator. Once this resistor divider reaches its reference voltage (i.e. 2.5 V) it saturates to low level activating the PNP_{set} transistor, connecting the SET terminal to the control reference. When this happens, the DCX stage will be turned off and therefore, the LCL will be in off-state. While the LCL is in off-state, the V_{diff} voltage will be equal to the V_{bus}. Thus, the I_{timer} tends to charge the C_{timer} capacitor. To avoid this and force the C_{timer} voltage to zero, a NPN_{reset} transistor is connected in parallel with C_{timer}.

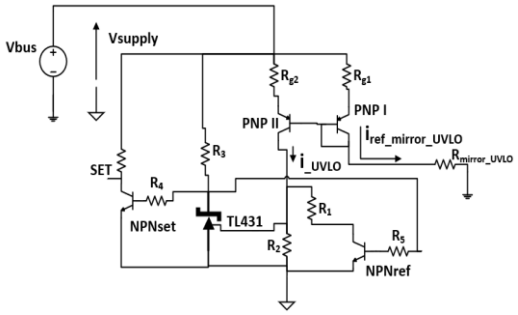

Fig. 14. Undervoltage section circuit diagram

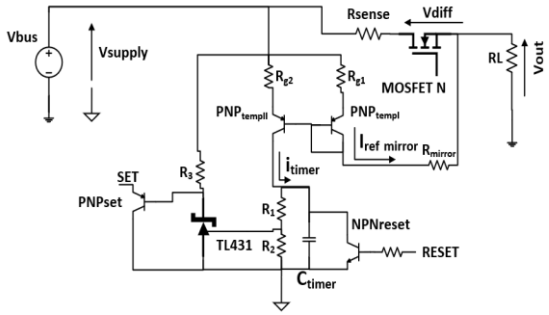

Fig. 15. Timer section circuit diagram

This NPN_{reset} transistor short-circuits the C_{timer} capacitor until the LCL is in on-state. As I_{ref_mirror} current is proportional to the V_{diff} voltage level, the C_{timer} charging time (i.e. trip-off time) will be proportional to the N-MOSFET drain-source voltage level (i.e. V_{diff}). The worst case will be the one in which a short-circuit is connected at the output of the LCL, meaning that V_{diff} will be equal to V_{bus}. The C_{timer} capacitor is sized to make that the LCL turns off in the time range specified in [3], which guarantees that the device temperature never reaches its maximum junction temperature.

IV. EXPERIMENTAL RESULTS

Two different prototypes have been designed following the architecture described in Section III, one using the SCT3022AL (ROHM) N-MOSFET and the other one for the SCTW90N65G2V (ST) N-MOSFET. Everything is the same, but the passive elements that perform the control loop response are tuned to the different small signal response of the two said transistors. Fig. 16 shows the main waveforms for a class 10 LCL limiting the current, under an overload event for a V_{bus} of 100 V. It can be seen how the LCL carries the class current of 10 A (I_N). While this happens, the control loop voltage (V_{loop}) is saturated to positive. The DCX translates this voltage to the N-MOSFET gate-source voltage (V_{gs}). The voltage at the output of the half bridge is represented in V_{bridge}. It can be seen how it follows the loop voltage. Upon an overload, there is an initial overshoot of 37 A and then the LCL reacts limiting the current (I_{lim}) to the maximum limitation value (i.e. 12 A). This is achieved by the control loop adjusting its voltage value, so the current is regulated. It can be seen how the V_{bridge} voltage, and thus the V_{gs} MOSFET follows it. Right after the short-circuit, the timer section starts to work (V_{Ctimer}), shutting down the LCL after a trip-off time of 1.5 ms. This is achieved by the timer turning off the DCX through the SET terminal of the RS flip-flop. It can be seen how V_{bridge} and then V_{gs} goes to zero, turning off the MOSFET. Consequently, the I_{sense} current goes to zero and the control loop saturates to positive. The second test is based on the LCL behaviour in a more stressful point of work. Fig. 17 shows the class 10 LCL prototype activation directly to a short-circuit. It can be seen how after the overcurrent, the DCX stage starts working, and how the current control loop regulates its value making the V_{loop} voltage smaller, in the same way as the N-MOSFET V_{gs} value. Therefore, the I_{sense} current value is regulated to the I_{lim} value of 12 A. After that, the timer section starts working, turning off the LCL after the trip-off time (i.e. 1.5 ms). As it was mentioned in Section III, a high impedance at the end of the LCL could be detrimental for its dynamic behaviour, mainly because the G_{i_uc} dependence on the Z_{load} parameter. Fig. 18 shows the LCL behaviour after a short-circuit when the LC filter described in Section III is connected between the LCL and the load. This case was the one that presents the highest impedance at the end of the LCL and was used for the control loop tuning. In this test, the ROHM N-MOSFET has been used for a bus voltage of 100 V and for a nominal current of 2.3 A, keeping the maximum limitation current in 12 A. As seen in Fig. 18, the LCL carries the nominal current and after the short-circuit the LCL reacts limiting the current with a good performance, in spite of the presence of a small oscillation, which is properly clamped as the LCL regulates the current to the maximum limitation value. In this way it is possible to check the LCL behaviour for the worst Z_{load} case. The same test was carried out using the ST N-MOSFET with very similar results.

The last test presented in this work is based on the connection of a capacitor between the LCL and the load (R_L). The objective is to verify the capacitor charging process through the LCL current. This emulates the turn on process of an equipment powered by the LCL. Fig. 19 shows the charging process (V_C) for a capacitor of 470 µF, using a R_L of 44 Ω, simulating the power demand, and for a bus voltage of 100 V. The charging time for both prototypes is about 5 ms, well above the trip-off time. The R_{sense} value for the all the tests performed with the designed prototypes is 0.02 Ω.

Power losses and dissipation is a key factor in space applications. Fig. 20 shows a loss breakdown analysis for the proposed N-MOSFET architecture in comparison with the traditional P-MOSFET ones. These losses have been measured for a class 10 LCL with a V_{bus} of 100 V. According to Fig. 20, the overall losses for the N-MOSFET architecture, considering the auxiliary power supply, the DCX stage and the current sensed stage, are about 5 W. In a traditional LCL architecture, only the dissipation using a Hi-Rel, space qualified P-MOSFET (i.e. IRHNA5S97260) [20] is about 10 W. For the same bus voltage, a classical LCL based on a P-MOSFET will have the same circuitry except for the DCX which will not be necessary. Therefore, the power consumption of this circuitry would be approximately the same.

Fig. 16. Class 10 LCL operation under a short-circuit for a V_{bus} of 100V, using the ROHM N-MOSFET

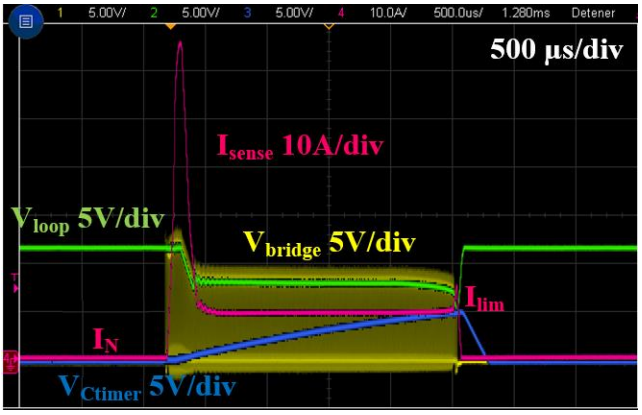

Fig. 17. LCL activation directly from a short-circuit for a V_{bus} of 100V, using the ROHM N-MOSFET

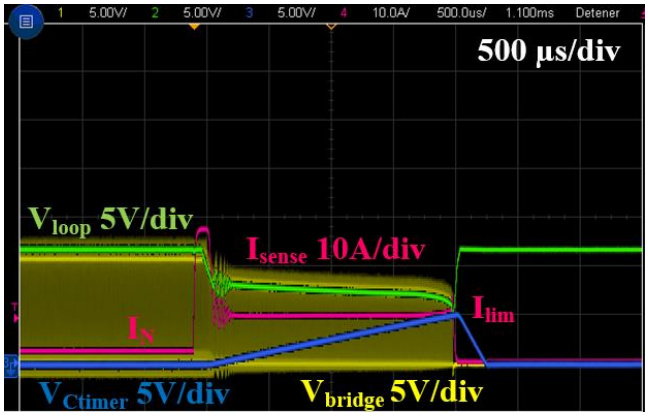

Fig. 18. LCL operation under a short-circuit using an LC filter between the LCL and the load. For a V_{bus} of 100 V, using the ROHM N-MOSFET

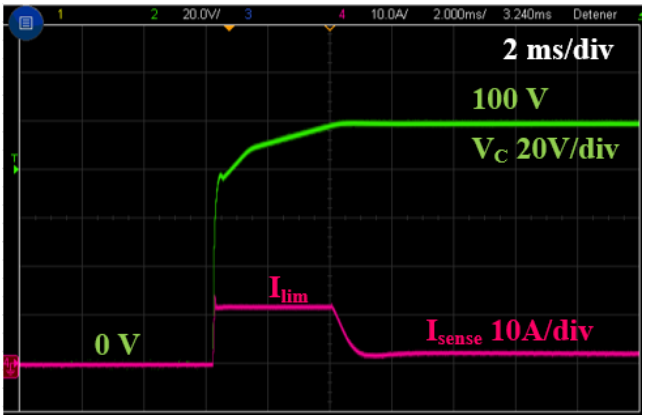

Fig. 19. Charging process of a capacitor connected between the LCL and the load, using the ROHM N-MOSFET. Current sensed (I_{sense}) and capacitor charging voltage (V_C)

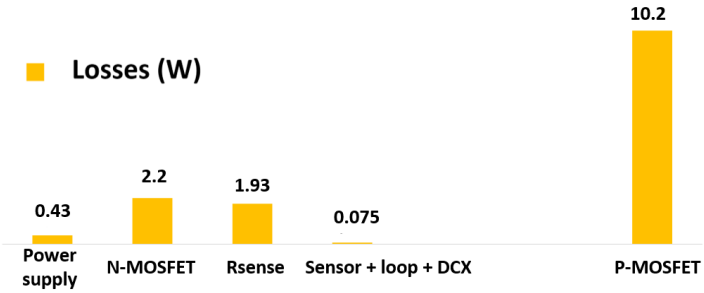

Fig. 20. Losses breakdown for the proposed N-MOSFET architecture and power losses in a Hi-Rel P-MOSFET for a class 10 LCL

V. CONCLUSIONS

This work presents an architecture of a LCL based on a SiC N-MOSFET working as a limiter device. The design process and the working behaviour have been verified through simulation and with experimental results. A class 10 LCL prototype has been designed following the proposed architecture for a bus voltage of 100 V. The proposed LCL reacts limiting the current in case of an overload event in the trip-off time, established for the timer section. This design is flexible enough to be adapted for higher bus voltages such as 120 V or 150 V. The control loop also offers a methodology for tuning the LCL dynamic response behaviour. Thanks to the lower Rdson a much lower dissipation is achieved using this LCL architecture, than with the traditional topologies based on P-MOSFETs. Satellites usually have around 100 LCLs therefore, the savings in power dissipation in the whole distribution system can be very significant.

ACKNOWLEDGEMENTS

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