An Overall Analysis of the Static Characteristics of the Single Active Bridge Converter

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Abstract: The dual active bridge (DAB) converter has been extensively analyzed and used in recent years for applications where bidirectional power flow is required. The unidirectional version of the DAB, which replaces the active output bridge with a diode bridge, has been called the single active bridge (SAB). The static behavior of the SAB differs markedly from similar DC/DC converters and can provide interesting advantages in certain applications. This paper presents a thorough study of the static behavior of the single active bridge (SAB) converter in different conduction modes. This study focuses on the description of the conduction modes, marking the main differences compared to similar DC/DC converters. Moreover, the SAB can be designed to operate in conduction mode for a given power level with different performance. A design guide is proposed, and the performance of different designs are compared, quantifying current stresses in the semiconductors. Finally, the main contribution of this paper is the identification of the similarities and differences between the SAB and the buck, forward, and phase-shifted full-bridge converters. It should be noted that the position of the inductor, either before or after the output rectifier bridge, modifies the voltage withstood by the output diodes and depends on the conduction mode, the voltage conversion ratio of the converter, and consequently, its main operation and performance. Moreover, the operation of the SAB is similar to a current source in all conduction modes, and it is not usual in similar converters. This peculiar behavior can be useful in certain applications. The theoretical study, the different designs, and the predicted operation of the SAB in different conduction modes have been validated using simulation and experimental results.

Keywords: isolated DC/DC converters; dual active bridge converter; single active bridge converter

1. Introduction

The dual active bridge converter (DAB) has garnered great interest over the last 15 years [1–4]. Its input-output symmetry makes it especially interesting for applications where bidirectional power flow between the input and output ports is required. In applications where one of the ports will always act as the input and the other as the output, it is possible to replace the entire active output bridge with a diode bridge, lowering the cost of the converter. The converter thus obtained has been called the single active bridge (SAB). The general scheme of the SAB converter is shown in Figure 1. Few studies have examined the basics of this converter [5–7]; thus, a full study is warranted.

In recent years, different circuit topologies have been proposed for unidirectional isolated DC/DC converters, such as battery chargers. Multiple SAB converters are connected in the input-parallel and output-parallel (IPOP) configuration to achieve higher

power in [8]. In addition, an isolated three-port DC/DC converter based on SAB converters is proposed in [9] to offer an efficient solution for meeting the increasing demand of integrating energy delivery elements, such as renewable energy sources, energy storage devices, and mains.
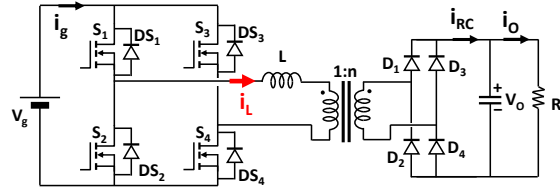

Figure 1. Single active bridge (SAB) converter.

A different unidirectional topology, also based on the DAB converter in which two switches in the secondary H-bridge converter are replaced with diodes, is proposed in [10] for fuel cell electric vehicles. Other topologies based on the SAB are analyzed in [11], where the SAB with a voltage doubler and with a full-bridge rectifier are compared, and [12] in which suitable modulation and controller schemes are proposed for improving the converter dynamics.

To improve the efficiency and power density of the SAB converter, soft-switching capabilities of this converter in its different conduction modes are analyzed in [6,13], and techniques to reduce switching and conduction losses are proposed in [14–16].

This article describes an extensive study of the static characteristics of this converter, including its conduction modes and the boundary between them, the value of its voltage conversion ratio in each conduction mode, the determination of the electrical requirements of its semiconductors, a guide to its design, and a comparison with other similar topologies. This study was validated using simulation and experimental results.

2. Static Analysis of SAB Converter in Continuous Conduction Mode (CCM)

Figure 2 shows the six equivalent circuits that characterize the operation of the converter in the operation mode in which the current by the inductor does not remain at zero. This operation mode is called continuous conduction mode (CCM). The value of the current passing through the inductor (i_L), shown in Figure 3a, can be calculated in all cases applying Faraday's law. The results are as follows:

- Interval (t_0, t_1): Corresponds to Figure 2a, where the semiconductors conducting the current are DS_1, DS_4, D_2, and D_3. The value of i_L is:

$$i_L = \frac{1}{L}\left(V_g + \frac{V_O}{n}\right)(t - t_0) + i_{L0},\tag{1}$$

where i_{L0} is the inductor current value at the beginning of this interval. This interval ends when i_L reaches zero at t_1, the value of which is:

$$t_1 = t_0 - \frac{Li_{L0}}{V_g + \frac{V_O}{n}}.\tag{2}$$

- Interval (t_1, t_2): Corresponds to Figure 2b, where the semiconductor conducting the current are S_1, S_4, D_1, and D_4. The value of i_L is:

$$i_L = \frac{1}{L}\left(V_g - \frac{V_O}{n}\right)(t - t_1).\tag{3}$$

At the end of this interval, the inductor current reaches the value i_{L2} at instant t_2, the value of which is:

$$t_2 = t_1 + \frac{Li_{L2}}{V_g - \frac{V_O}{n}}.\tag{4}$$

- Interval (t_2, t_3): Corresponds to Figure 2c, where the semiconductors conducting the current are DS_2, S_4, D_1, and D_4. The value of i_L is:

$$i_L = -\frac{1}{L}\left(\frac{V_O}{n}\right)(t - t_2) + i_{L2}. \tag{5}$$

At the end of this interval, the inductor current reaches the value $i_{L3} = -i_{L0}$ at instant t_3, the value of which is:

$$t_3 = t_2 + \frac{L(i_{L3} - i_{L2})}{-\frac{V_O}{n}}. \tag{6}$$

- Interval (t_3, t_4): Corresponds to Figure 2d, where the semiconductors conducting the current are DS_2, DS_3, D_1, and D_4. The value of i_L is:

$$i_L = -\frac{1}{L}\left(V_g + \frac{V_O}{n}\right)(t - t_3) + i_{L3}. \tag{7}$$

This interval ends when i_L reaches zero at instant t_4, the value of which is:

$$t_4 = t_3 + \frac{Li_{L3}}{V_g + \frac{V_O}{n}}. \tag{8}$$

- Interval (t_4, t_5): Corresponds to Figure 2e, where the semiconductors conducting the current are S_2, S_3, D_2, and D_3. The value of i_L is:

$$i_L = \frac{1}{L}\left(-V_g + \frac{V_O}{n}\right)(t - t_4). \tag{9}$$

At the end of this interval, the inductor current reaches the value, $i_{L5} = -i_{L2}$, at instant t_5, the value of which is:

$$t_5 = t_4 + \frac{Li_{L5}}{-V_g + \frac{V_O}{n}}. \tag{10}$$

- Interval (t_5, t_6): Corresponds to Figure 2f, where the semiconductors conducting the current are DS_1, S_3, D_2, and D_3. The value of i_L is:

$$i_L = \frac{1}{L}\left(\frac{V_O}{n}\right)(t - t_5) + i_{L5}. \tag{11}$$

At the end of this interval, the inductor current reaches the value, $i_{L6} = -i_{L3}$, at instant t_6, the value of which is:

$$t_6 = t_5 + \frac{L(i_{L6} - i_{L5})}{\frac{V_O}{n}}. \tag{12}$$

Finally, the switching period can be obtained as a result of the duration of these intervals using:

$$T_S = t_6 - t_0. \tag{13}$$

Given the operation symmetry of the converter in periods, (t_0, t_3) and (t_3, t_6), the following equation is satisfied:

$$t_3 - t_0 = t_6 - t_3 = \frac{T_S}{2}. \tag{14}$$

One of the possible control techniques for this converter is to keep the frequency constant and to regulate the duration of the time corresponding to intervals, (t_0, t_1) and (t_1, t_2). For this reason, it is useful to define:

$$t_c = t_2 - t_0, \tag{15}$$

$$d = \frac{t_c}{T_S}. \tag{16}$$

The voltage conversion ratio of this converter in this conduction mode can be calculated using the previous equations, determining the average current injected into the output RC network, i_{RC_avg}, during a switching half period, which for convenience can be measured between t_1 and t_4. Note that during this entire time interval, D_1 and D_4 diodes are conducting; thus, the i_L/n current is injected into the aforementioned RC network. Since the i_L waveform is composed of linear sections, this calculation is quite simple, but laborious. The result of the calculation is:

$$i_{RC\_avg} = \frac{1}{2nLT_S} \left[V_g t_c (T_S - t_c) - \frac{T_S^2 \left(\frac{V_O}{n} \right)^2}{4V_g} \right]. \tag{17}$$

This current determines the output voltage value, given by the following equation:

$$V_O = i_{RC\_avg} R_L. \tag{18}$$

Using Equations (16)–(18), the normalized voltage conversion ratio is easily obtained using:

$$N = \frac{V_O}{nV_g} = \frac{4(1-d)d}{k + \sqrt{k^2 + 4(1-d)d}}, \tag{19}$$

where N is the voltage conversion ratio normalized at the transformer ratio (n) and parameter k is defined as:

$$k = \frac{2Ln^2}{R_L \frac{T_S}{2}}. \tag{20}$$

Equations (19) and (20) show that the SAB converter has high output impedance operating in CCM, as its voltage conversion ratio depends on the load resistance, R_L, through the parameter k. This situation (a behavior similar to a current source) is the opposite of most DC/DC converters operating in CCM. This is because the inductor is placed on the AC side of the converter and not at the output of the rectifier, as in other bridge converters. The operation of the SAB converter in CCM only implies that the current does not remain at zero when it reaches this value.
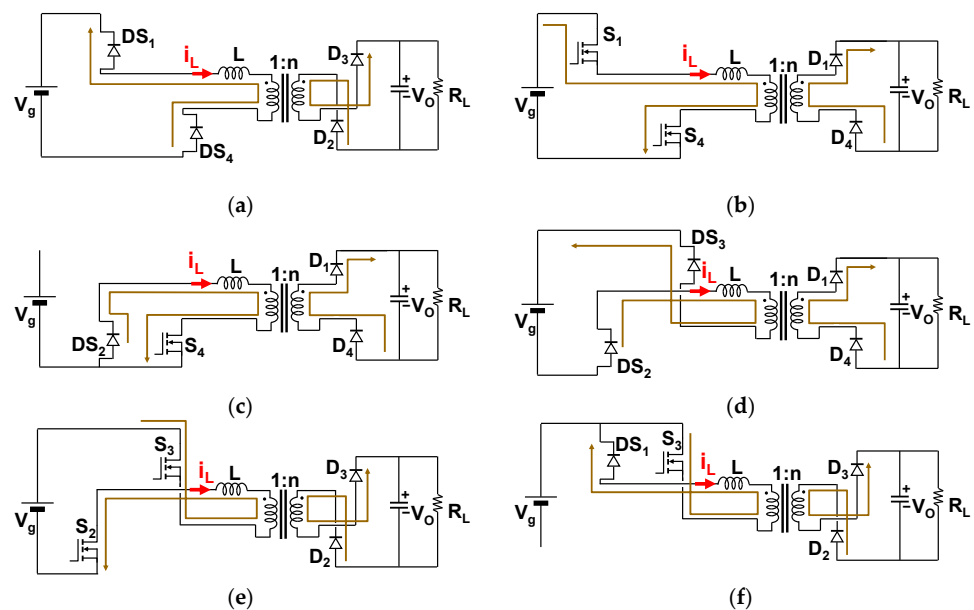

Figure 2. Lineal subcircuits of operation of SAB converter in CCM. (**a**) Interval (t_0, t_1), (**b**) interval (t_1, t_2), (**c**) interval (t_2, t_3), (**d**) interval (t_3, t_4), (**e**) interval (t_4, t_5) and (**f**) interval (t_5, t_6).

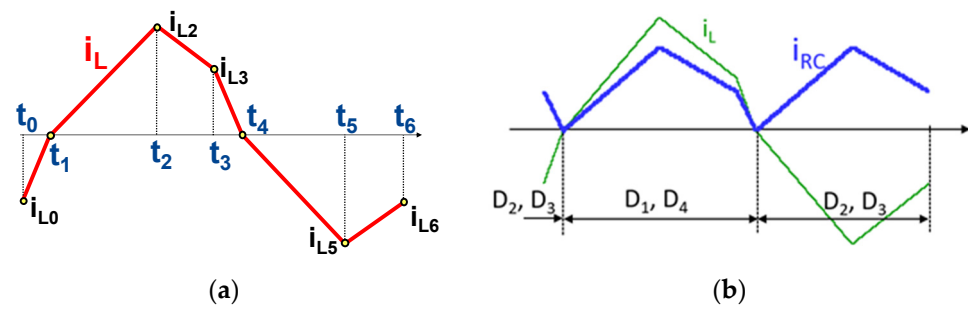**Figure 3.** (**a**) Inductor current in CCM. (**b**) Inductor current and current injected into the output RC network through the corresponding output bridge diodes in CCM.

3. Static Analysis of SAB Converter in Discontinuous Conduction Mode (DCM)

The operation mode in which the current passing through the inductor reaches zero in the intervals, (t_2, t_3) and (t_5, t_6), is called discontinuous continuous mode (DCM). If this occurs, the current remains zero until the end of these intervals. In this case, some of the equations for CCM must be modified. Thus, Equations (1) and (7) for CCM become, in both cases:

$$i_L = 0. \tag{21}$$

The value of i_L given by the previous equations in the other intervals remains valid. The duration of the different intervals, given by (2) and (8) are not valid, while Equations (4) and (10) remain unchanged, and Equations (6) and (12) must be modified by replacing the values of i_{L3} and i_{L6} with zero. The linear subcircuits of Figure 2a,d are no longer valid and must be replaced by the one depicted in Figure 4. The i_L waveform in DCM is represented in Figure 5a.
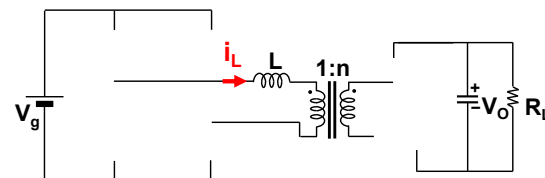

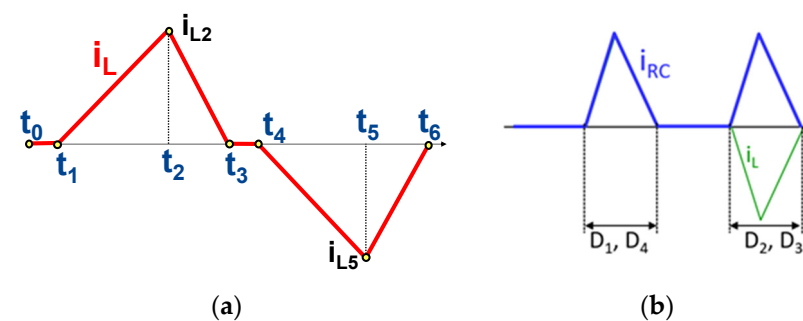**Figure 4.** Lineal subcircuit of operation of SAB converter in DCM.

Figure 5. (**a**) Inductor current in DCM. (**b**) Inductor current and current injected into the output RC network through the corresponding output bridge diodes in DCM.

As in CCM, the voltage conversion ratio is calculated in DCM using the value of i_{RC_avg}. The calculation of i_{RC_avg} is again simple but laborious. The result is as follows:

$$i_{RC\_avg} = \frac{V_g}{V_O L T_S} \left[V_g - \frac{V_O}{n} \right] t_c^2. \tag{22}$$

Using (16), (18), and (22), the normalized voltage conversion ratio in DCM is easily obtained:

$$N = \frac{V_O}{nV_g} = \frac{2d}{d + \sqrt{d^2 + k}}.$$

(23)

4. Boundary between the Two Conduction Modes and Voltage Conversion Ratio

In the operation of the SAB converter working at a constant frequency, the value of the parameter, k, varies only with the load resistance (R_L). The R_L value corresponding to the converter operating on the boundary between the two conduction modes is called R_{L_crit}. k_{crit} can be defined as follows:

$$k_{crit} = \frac{2Ln^2}{R_{L\_crit} \frac{T_S}{2}}.$$

(24)

As Equations (19) and (23) must be simultaneously verified on the boundary between the two conduction modes, and adding the suffix "*crit*" to the corresponding k and d values to operate at this boundary, the following equation is obtained:

$$k = k_{crit} = 1 - 2d_{crit}.$$

(25)

By substituting Equation (25) in (19) or (23), the following equation is obtained:

$$N_{crit} = \left(\frac{V_O}{nV_g} \right)_{crit} = 2d_{crit}.$$

(26)

As in the case of other converters, CCM occurs when $R_L < R_{L\_crit}$. Considering Equation (24), this is equivalent to verifying $k > k_{crit}$ in CCM, while $k < k_{crit}$ in DCM.

Once the boundary between the two conduction modes has been obtained, it is straightforward to determine when (19) (valid only in CCM) and when (23) (valid only in DCM) should be used to calculate the open loop voltage conversion ratio. Setting the value of duty cycle d and letting the output voltage change when changing R_L, the evolution of this normalized voltage conversion ratio is shown in Figure 6a, which shows three different regions: operation in CCM, operation in DCM, and unachievable voltage conversion ratios.
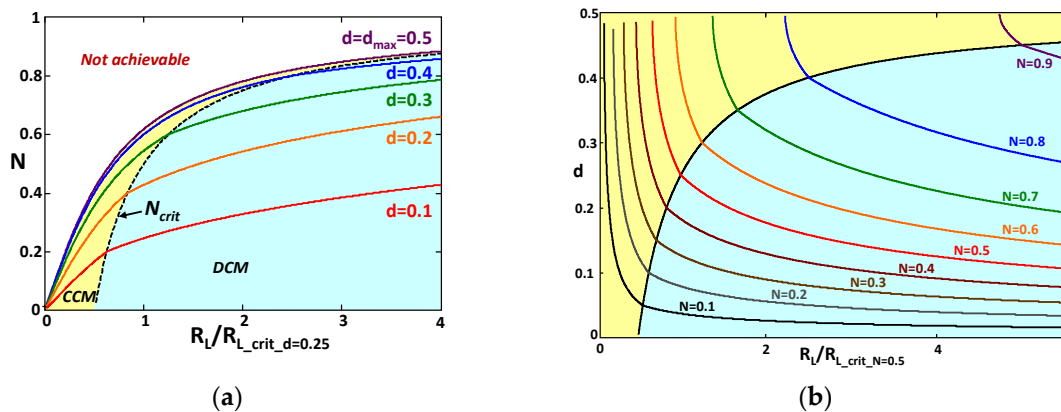

(a)　　　　　　　　　　　　　　　　　　　　　　(b)

Figure 6. (**a**) Variation of the normalized voltage conversion ratio in open loop based on the normalized load resistance. In this normalization, the critical value of R_L when d is 0.25 (half of d_{max}) is used as the base value. (**b**) Variation of the duty cycle of the converter in closed loop, based on the normalized load resistance. In this normalization, the critical value of R_L when N is 0.5 (half of N_{max}) is used as the base value.

Figure 6a shows that this converter has high output impedance, not only in DCM (as other converters) but also in CCM. This peculiar behavior can be interesting for certain applications. The maximum normalized voltage conversion ratio is obtained by unloading

the converter to the limit, which corresponds to calculating the limit of N (calculated in DCM, i.e., by (23)) as k approaches zero:

$$N_{max} = \lim_{k \to 0} N = 1. \tag{27}$$

The information provided by Figure 6a is very important for understanding the operation of the SAB converter, but it is especially useful to have an idea of the closed-loop operation of the converter, that is, when a feedback loop ensures a given voltage conversion ratio at full load and the value of R_L is gradually increased. Under these conditions, the duty cycle of the converter will decrease, which can be seen in Figure 6b. The normalized voltage conversion ratio, N, has been used as a parameter. The duty cycle at the boundary of the two conduction modes, d_{crit}, is the value shown in (26).

The curves shown in Figure 6b are obtained using (19) and (23), clearing the value of d. The value of R_L has been represented as normalized in Figure 6b, using the critical value of R_L when N is 0.5 as the base value for normalization. Remember that the maximum value of N is 1, given by (27).

5. Voltage and Current Stresses of Semiconductors

One of the most interesting properties of this converter is that the maximum voltages in the transistors and diodes in the primary bridge, on the one hand, and in the diodes in the output rectifier bridge, on the other hand, are limited by the values of the input and output voltages, respectively.

In contrast, rms currents passing through the transistors and diodes of the primary bridge (in general, considering the possibility of using IGBTs) strongly depend on the point of operation of the converter and which of the branches is being considered. The latter is closely related to the sequence of control pulses in transistors.

As an example, an operation point has been chosen in CCM. Figure 7a shows the voltages at the midpoints of the two branches of the bridge (v_{S2} and v_{S4}). The phase-shift between them generates the v_B waveform, which is the voltage between those midpoints. Looking at the voltages, v_{S2} and v_{S4}, it is clear that v_{S2} is delayed from v_{S4}; thus, the branch where v_{S2} is measured is called the "lagging branch", and the other branch is called the "leading branch".

From the sequence of intervals shown in Figure 2, the waveforms in Figure 7b are easily inferred. In the lagging branch there is a more equal distribution of the currents driven by the transistor and its diode in anti-parallel, compared to the leading branch. Therefore, conduction losses will be greater in transistors in the leading branch and in anti-parallel diodes of transistors in the lagging branch, than in transistors in the lagging branch and anti-parallel diodes of transistors in the leading branch.
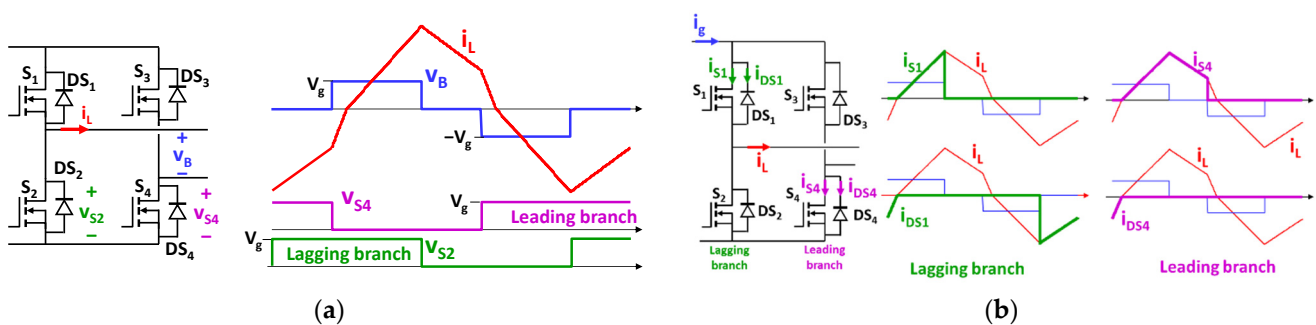

(a)   (b)

Figure 7. (**a**) Voltages at the midpoints of the branches. (**b**) Currents through the semiconductors of the input bridge.

Average and rms currents through the semiconductors of the primary bridge can be calculated using the following equations:

$$i_{S1\_avg} = \frac{1}{T_S}\left[\frac{i_{L2}}{2}(t_2 - t_1)\right], \tag{28}$$

$$i_{DS1\_avg} = \frac{1}{T_S}\left[\frac{i_{L0}}{2}(t_1) + i_{L0}(t_3 - t_2) - \frac{i_{L2} - i_{L3}}{2}(t_3 - t_2)\right], \tag{29}$$

$$i_{S4\_avg} = \frac{1}{T_S}\left[\frac{i_{L2}}{2}(t_2 - t_1) + \frac{i_{L2} - i_{L3}}{2}(t_3 - t_2) + i_{L3}(t_3 - t_2)\right], \tag{30}$$

$$i_{DS4\_avg} = \frac{1}{T_S}\left[\frac{i_{L0}}{2}(t_1)\right], \tag{31}$$

$$i_{S1\_rms} = \frac{1}{\sqrt{3}}\sqrt{\frac{i_{L2}^2(t_2 - t_1)}{T_S}}, \tag{32}$$

$$i_{DS1\_rms} = \frac{1}{\sqrt{3}}\sqrt{\frac{i_{L0}^2 t_1 + (i_{L2}^2 + i_{L3}^2 + i_{L2}i_{L3})(t_3 - t_2)}{T_S}}, \tag{33}$$

$$i_{S4\_rms} = \frac{1}{\sqrt{3}}\sqrt{\frac{i_{L2}^2(t_2 - t_1) + (i_{L2}^2 + i_{L3}^2 + i_{L2}i_{L3})(t_3 - t_2)}{T_S}}, \tag{34}$$

$$i_{DS4\_rms} = \frac{1}{\sqrt{3}}\sqrt{\frac{i_{L0}^2 t_1}{T_S}}. \tag{35}$$

Average and rms currents through the diodes of the secondary bridge can be calculated using the following equations:

$$i_{D1\_avg} = \frac{1}{nT_S}\left[-\frac{i_{L0}}{2}(t_1) + \frac{i_{L2}}{2}(t_2 - t_1) + \frac{i_{L2} - i_{L3}}{2}(t_3 - t_2) + i_{L3}(t_3 - t_2)\right], \tag{36}$$

$$i_{D1\_rms} = \frac{1}{n\sqrt{3}}\sqrt{\frac{i_{L0}^2 t_1 + i_{L2}^2(t_2 - t_1) + (i_{L2}^2 + i_{L3}^2 + i_{L2}i_{L3})(t_3 - t_2)}{T_S}}. \tag{37}$$

Average values of the input and output currents and the rms value of the inductor current can be calculated with the following equations:

$$i_{g\_avg} = \frac{2}{T_S}\left[\frac{i_{L0}}{2}(t_1) + \frac{i_{L2}}{2}(t_2 - t_1)\right], \tag{38}$$

$$i_{RC\_avg} = 2i_{D1\_avg}, \tag{39}$$

$$i_{L\_rms} = \frac{1}{\sqrt{3}}\sqrt{\frac{i_{L0}^2 t_1 + i_{L2}^2(t_2 - t_1) + (i_{L2}^2 + i_{L3}^2 + i_{L2}i_{L3})(t_3 - t_2)}{T_S/2}}. \tag{40}$$

To graphically show the distribution of the currents through the transistor and its anti-parallel diode (Figure 8), an SAB converter is designed, selecting the change between modes at half of the maximum output current for the lower input voltage and the higher output voltage (i.e., the maximum voltage conversion ratio). The semiconductor rms current values are normalized to the average input current, while the output current is normalized to its maximum value.

$$i_{x\_RMS\_norm} = \frac{i_{x\_RMS}}{i_{g\_avg}} \tag{41}$$

$$I_{O\_norm} = \frac{I_O}{I_{O\_crit\_Nmax}} \tag{42}$$

In Figure 8a, normalized rms values of the current through the semiconductors are shown for the maximum voltage conversion ratio ($N = N_{max}$), while in Figure 8b, the voltages are changed to obtain a $N = 0.8 \cdot N_{max}$.

Another important issue to consider is the possibility of operating with zero-voltage-switching (ZVS) on the transistors in the primary bridge. During the interval, (t_0, t_3), this is achieved if the i_L current is positive in t_2 and t_3 since this current is responsible for redistributing the electrical charges associated with the parasitic capacitance of the midpoints of the branches. This current is always positive in t_2 but is only positive in t_3 if the converter operates in CCM. Of course, the same happens in the interval, (t_3, t_6), but in this case with i_L being negative at t_5 and t_6. Therefore, transistors in the leading branch only operate with ZVS in CCM, while transistors in the lagging branch operate with ZVS in both conduction modes.
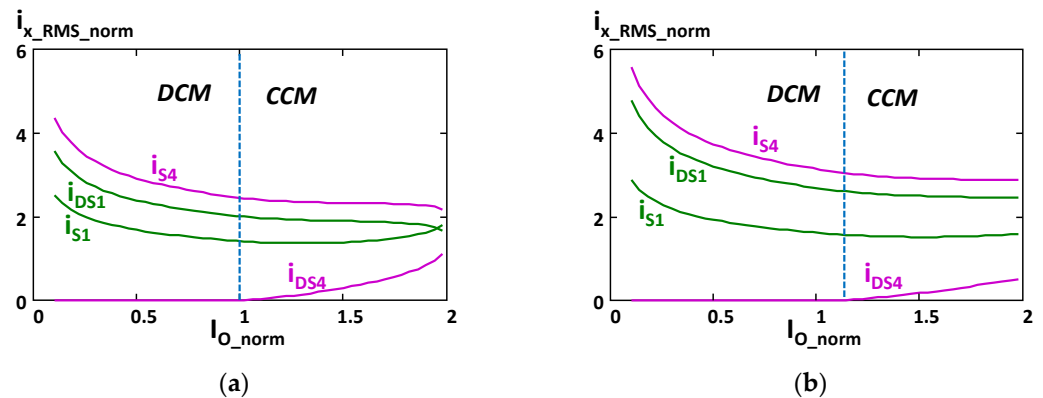

(a)　　　　　　　　　　　　　　　　　　　　　　　(b)

Figure 8. Normalized rms values of the current through the semiconductors of the primary bridge. The converter is designed to enter in DCM at half of the maximum output current at the maximum normalized voltage conversion ratio; $N = N_{max}$. d_{max} is limited at 0.48. (**a**) $N = N_{max}$ and (**b**) $N = 0.8 \cdot N_{max}$.

Consequently, the operation in CCM is desirable to minimize switching losses on the transistors. However, CCM implies that during intervals, (t_0, t_1) and (t_3, t_4), the i_L current is not zero (unlike in DCM) and is circulating in such a way that electrical power is returned to the primary source (V_g). In other words, the converter works with electrical energy recirculated towards its input (reactive energy), which ends up decreasing its efficiency by increasing conduction losses. Therefore, the ideal situation is one in which the converter works in CCM but very close to the boundary between this mode and DCM.

Finally, rectifier diodes of the secondary bridge operate neglecting switching losses in both conduction modes. The current in the turn-off of the rectifier diodes is always zero, and consequently, there are no reverse recovery losses.

6. Comparison with Other Converters

As discussed above, the SAB converter operating in CCM differs markedly from similar DC/DC converters, as V_O varies by changing the R_L value when d and V_g are maintained constant. On the other hand, the operation in DCM is very similar to the other classic converters belonging to the buck family of converters, as will be explained in this section.

Regarding the SAB converter operating in the DCM, (23) can be rewritten as follows:

$$N = \frac{2}{1 + \sqrt{1 + \frac{k}{d^2}}} \tag{43}$$

In the case of the buck converter operating in DCM, it is well known that the voltage conversion ratio in DCM is [17]:

$$N_{Buck} = \frac{V_O}{V_{g\_Buck}} = \frac{2}{1 + \sqrt{1 + \frac{4k_{Buck}}{d_{Buck}^2}}},\tag{44}$$

where the subscript "*Buck*" has been added to the original expression given in [17]. The value of the dimensionless conduction parameter k_{Buck} is defined in [17] as follows:

$$k_{Buck} = \frac{2L_{Buck}}{R_L T_{S\_Buck}}.\tag{45}$$

Comparing (43) with (44) and (20) with (45), it can be concluded that N and N_{Buck} coincide if:

(a) The dimensionless conduction parameters, k and k_{Buck}, also coincide, which means that:

$$L_{Buck} = Ln^2.\tag{46}$$

$$T_{s\_Buck} = \frac{T_S}{2},\tag{47}$$

In other words, k and k_{Buck} coincide if the buck inductor is selected with the same value as the SAB inductor reflected to the transformer secondary side and the buck switching frequency is selected as twice the SAB frequency, which, in fact, coincides with the switching frequency corresponding to its output diodes.

(b) The buck duty cycle d_{Buck} is selected as twice the SAB duty cycle, d:

$$d_{Buck} = 2d_{SAB}.\tag{48}$$

As in the previous case, this is a consequence of the symmetrical operation of the SAB during (t_0, t_3) and (t_4, t_6).

(c) As the buck converter does not have any transformers, n must be selected as equal to 1.

In the case of the forward converter operating in DCM, the normalized voltage conversion ratio can also be easily deduced from [17], taking into account that the LC output filter is excited by the input voltage multiplied by n, and it works at the same converter duty cycle and switching frequency, leading to:

$$N_{FW} = \frac{V_{O\_FW}}{n_{FW}V_{g\_FW}} = \frac{2}{1 + \sqrt{1 + \frac{4k_{FW}}{d_{FW}^2}}},\tag{49}$$

$$k_{FW} = \frac{2L_{FW}}{R_L T_{S\_FW}},\tag{50}$$

where the subscript "*FW*" denotes that the quantities correspond to the forward converter. This case is very similar to the case of the buck converter; the final conclusions being that the operation of the forward and SAB converters in DCM coincide if:

$$L_{FW} = Ln^2,\tag{51}$$

$$T_{S\_FW} = \frac{T_S}{2},\tag{52}$$

$$d_{FW} = 2d,\tag{53}$$

$$n_{FW} = n.\tag{54}$$

Special attention must be paid to the case of the phase shifted full-bridge converter. It should be noted that the LC output filter of this converter is excited by a square voltage waveform whose peak value is the input voltage multiplied by n; its duty cycle and frequency are both twice those of the converter. When this converter is operating in DCM, the normalized voltage conversion ratio can be easily deduced from [17], taking into account the aforementioned differences in comparison to the buck converter, leading to:

$$N_{FB} = \frac{V_{O\_FB}}{n_{FB} V_{g\_FB}} = \frac{2}{1 + \sqrt{1 + \frac{k_{FB}}{d_{FB}^2}}}, \tag{55}$$

$$k_{FB} = \frac{2 L_{FB}}{R_L \frac{T_{S\_FB}}{2}}, \tag{56}$$

where the subscript "*FB*" denotes that the quantities correspond to the full-bridge converter (with phase shifted control). Comparing (43) with (55) and (20) with (56), it can be concluded that N and N_{FB} coincide if:

$$n_{FB} = n \tag{57}$$

$$L_{FB} = L n^2 \tag{58}$$

In other words, the normalized voltage conversion ratio in DCM of the phase shifted full-bridge converter and SAB converter, N_{FB} and N, coincide if both converters have been designed with the same transformer turns ratio, and the full-bridge inductor has been selected with the same value as the SAB inductor reflected to the transformer secondary side.

Therefore, if the power stages shown in Figure 9 are compared, it can be concluded that the normalized voltage conversion ratio of both stages is the same if the stages have been designed to operate in DCM, whereas the normalized voltage conversion ratio of both stages differs completely if the stages start working in CCM. This also means that if the stages have been designed to operate in DCM, then the normalized voltage conversion ratio is independent of the position of the inductor, either before or after the output rectifier bridge. It should be noted that the position of the inductor modifies the maximum voltage withstood by the output diodes.

In Table 1, the voltage conversion ratio in DCM of the previously described converters is shown to summarize the comparison of SAB with similar converters.

Table 1. Summary of the converter comparison.

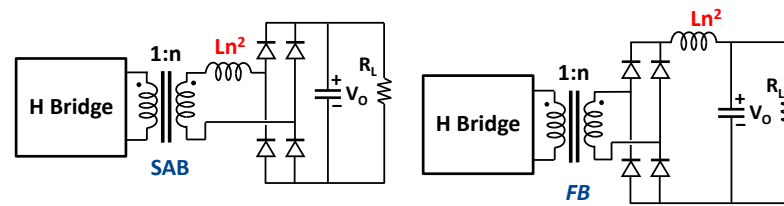| Converter	Voltage Conversion Ratio (N) in DCM
SAB	$N_{SAB} = \dfrac{2}{1 + \sqrt{1 + \frac{k_{SAB}}{d_{SAB}^2}}}$
Buck	$N_{Buck} = \dfrac{2}{1 + \sqrt{1 + \frac{4 k_{Buck}}{d_{Buck}^2}}},$
Forward	$N_{FW} = \dfrac{2}{1 + \sqrt{1 + \frac{4 k_{FW}}{d_{FW}^2}}},$
Phase-shifted full bridge	$N_{FB} = \dfrac{2}{1 + \sqrt{1 + \frac{k_{FB}}{d_{FB}^2}}},$

Figure 9. Comparison of SAB and phase-shifted full-bridge converter.

7. Converter Design Guide

The initial variables for the converter design, which are a function of the specifications of the application, are as follows:

- Maximum input voltage, V_{gmax}.
- Minimum input voltage, V_{gmin}.
- Maximum output voltage, V_{omax}.
- Minimum output voltage, V_{omin}.
- Maximum output current, I_{omax}.
- Minimum output current, I_{omin}.
- Maximum duty cycle, d_{max}, always lower than 0.5.
- Switching frequency, f.

Since the converter has a transformer, a certain voltage conversion ratio V_O/V_g can be given by infinite possible values of N, depending on the choice of n and always taking into account (27). Moreover, N depends on d and the choice of L through k. Therefore, a certain operation point, defined by V_O, V_g, and R_L, can be achieved with infinite sets of values of n, d, and L. That operation point will change during the use of the converter and the new operation point must be reached by changing only the value of d and always complying with the existing restrictions to the possible values of d and N (i.e., $d < d_{max} = 0.5$ and $N < N_{max} = 1$). Despite this, there are infinite combinations of n and L compatible with the new operation point obtained by changing d. In conclusion, there is always a degree of freedom in the choice of n and L. Therefore, one of these values can be defined according to a certain objective. In this paper, an objective is proposed that the converter operates in CCM in a certain operating range. To do this, the value of d_{crit} is set to the minimum input voltage and the maximum output voltage. This value of d_{crit} is called $d_{critmax}$. By setting this value, the value of n is calculated from Equation (26), resulting in:

$$n = \frac{V_{Omax}}{2V_{gmin}d_{critmax}}. \tag{59}$$

Once the value of n is chosen, the value of L must be low enough to allow the converter to process the maximum output current, i.e., at V_{Omax}, V_{gmin}, and R_{Lmin}. Considering that $I_{Omax} = V_{Omax}/R_{Lmin}$ and using (19) and (20), the value of L is obtained with:

$$L = \frac{\left[V_{gmin}d_{max}(1 - d_{max}) - \frac{V_{Omax}^2}{4V_{gmin}n^2}\right]}{2nfI_{Omax}}. \tag{60}$$

Two different design examples are shown here. The following specifications are the same for both designs: V_{gmax} = 850 V; V_{gmin} = 800 V; V_{omax} = 400 V; V_{omin} = 350 V; I_{omax} = 5.5 A; I_{omin} = 0.5 A; d_{max} =0.45; f = 33 kHz. The difference between the two designs is the selection of $d_{critmax}$:

Design 1: $d_{critmax}$ = 0.1 is selected. With the previously described global specifications, n is calculated using (59), obtaining the value of n = 2.5. With the previously calculated value of n and the global specifications, L is calculated using (60), obtaining the value of L = 209 µH.

Design 2: $d_{critmax} = 0.25$ is selected. With the previously described global specifications, n is calculated using (59), obtaining the value of $n = 1$. With the previously calculated value of n and the global specifications, L is calculated using (60), obtaining the value of $L = 408\ \mu H$.

In Figure 10a,b, the evolution of the duty cycle depending on the output current is shown when the converter works in closed loop for both designs. These curves are obtained as in Figure 6b, i.e., from Equations (19) and (23) and by clearing the value of d in them. The difference is that the independent variable is in this case $I_O = V_O/R_L$ instead of R_L. It can be observed that choosing $d_{critmax} = 0.1$ (Design 1), the converter operates in CCM for most of the I_O variation range. This is attractive for reducing switching losses, but it penalizes conduction losses. In Design 2 ($d_{critmax} = 0.25$), since the converter works in DCM for most I_O values, conduction losses are reduced while switching losses are penalized. In Figure 10c,d, the waveforms corresponding to $V_O = 400$ V, $V_g = 800$ V and two output power levels are shown. Comparing the two figures, the current values in the second design are lower than in the first. The same pattern can be seen in more detail in Figure 10e,f, which show the rms values of the current passing through the transistors and anti-parallel diodes of the leading branch (taking as an example S_3 and DS_3) and the lagging branch (taking as an example S_1 and DS_1). Considering the scales of the figures it is clear the conduction losses are lower in the second design.
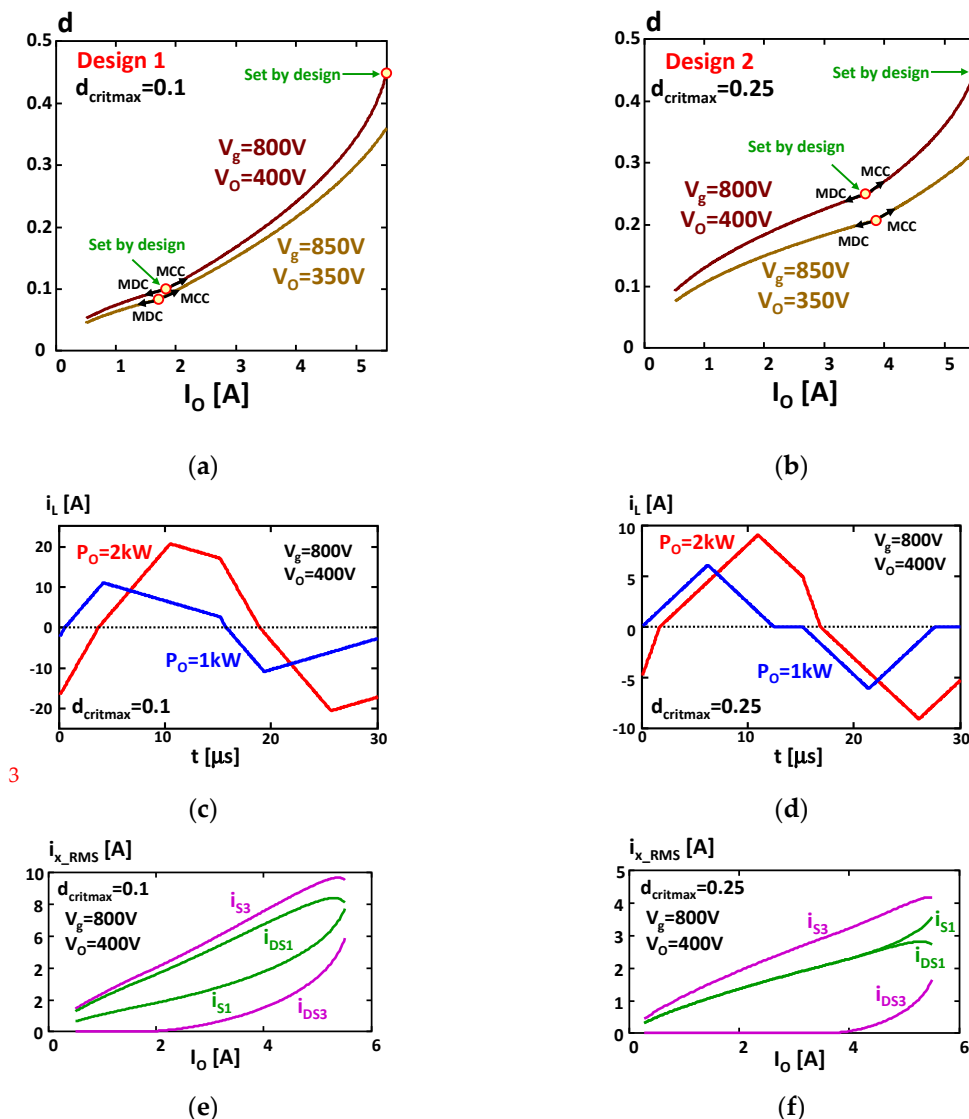

Figure 10. Analytical results using Design 1 ($d_{critmax} = 0.1$, (**a**,**c**,**e**)) and Design 2 ($d_{critmax} = 0.25$, (**b**,**d**,**f**)).

8. Simulation and Experimental Results

The verification of the proposed static analysis of the SAB converter was initially carried out by simulation with PSIM on a converter with ideal components and the same characteristics as those presented in the design examples. The results predicted by the theory perfectly matched the results at various simulated operating points. In addition, the waveforms obtained in the simulation perfectly matched those produced by the theory. Simulation results are not shown because they are the same as the presented analytical results.

A preliminary SAB prototype has been developed and tested to validate the analytical study proposed in this paper. The prototype has the characteristics of Design 2. Experimental (squares and diamonds) and analytical (continuous line) results at various operating points are compared in Figure 11a with good agreement. Moreover, experimental waveforms obtained using the prototype and shown in Figure 11b,c match those obtained from the theory (Figure 10d). As can be seen in Figure 11c, a small resonant period is observed during the intervals where the inductor current should theoretically be zero. This resonant period is caused by the reverse recovery current of the anti-parallel diodes of the main transistors. This phenomenon occurs on many occasions when DC/DC converters work in DCM.
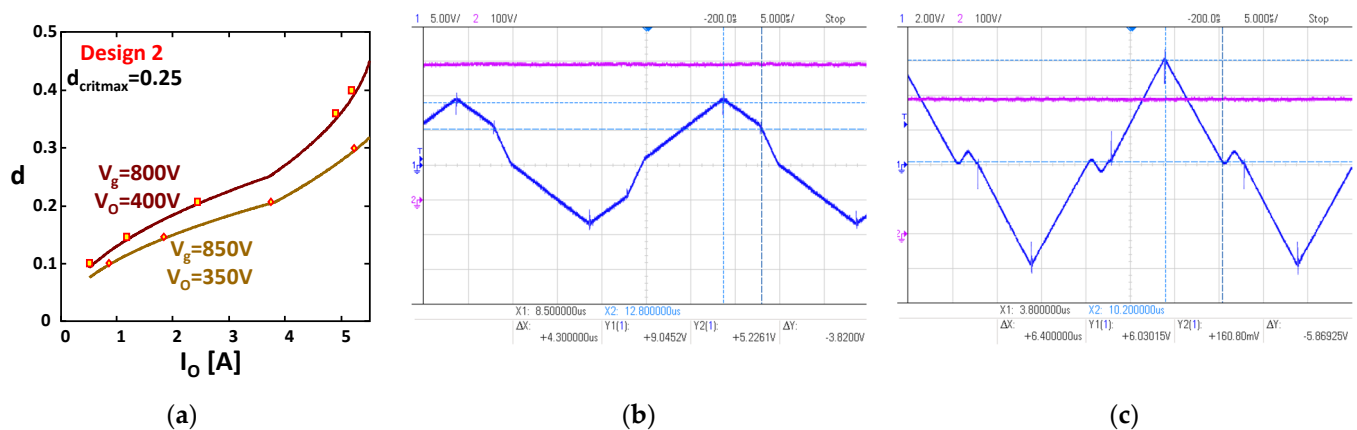

(a)   (b)   (c)

Figure 11. Experimental results using Design 2 ($d_{critmax}$ = 0.25, n = 1, and L= 407 uH), V_g = 800 V and V_O = 400 V. (**a**) Experimentally measured output current for different duty cycles. Inductor current (blue) and output voltage (violet) in (**b**) CCM at 2 kW (d = 0.36) and (**c**) DCM at 1 kW (d = 0.206).

9. Conclusions

In this paper, the static behavior of the SAB converter has been thoroughly studied. The voltage conversion ratio in both CCM and DCM have been found, as well as the conditions for the change of conduction mode. Unlike other converters, operation in CCM does not imply low open loop output impedance, but, as in DCM, this converter has a high output impedance under both conduction modes. This means that when the converter works in a closed loop, its duty cycle changes extensively when changing the load in both conduction modes. It is also appreciated that the design for operation in CCM reduces switching losses, but penalizes conduction losses, just the opposite of operating in DCM. Finally, operation in DCM is identical to that of buck, forward and phase shifted full-bridge converters if appropriate transformations related to the switching frequency, duty cycle, and inductance value are performed.

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