Analysis and design of a resonant DC/DC transformer in modular operation

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Abstract: **Modular connection between DC/DC converters is commonly used for many applications, to adapt voltage and power ranges, and in order to achieve scalability. This work presents a modular connection between DC/DC modules, providing an accurate voltage and power sharing, in a reliable way. This option could be used in the intermediate bus architectures, to adapt voltage and power levels, achieving high efficiency. Another advantage of the modular connection is the possibility of standardization. This way, it is possible to reuse a whole system module, just only adapting its voltage level, using an intermediate stage, based on the connection of several DC/DC blocks. To validate this solution, several DC/DC resonant converts have been designed for an input and output voltage of 56 V and 28 V respectively, for a rated power of 200 W (per module) and for a switching frequency of 400 kHz. Therefore, by combining several of these designed modules, it is possible to work at higher voltages and powers in whole system.**

Keywords: ***Resonant converter, isolated converter, standardization, modular converter, reliability.***

I. Introduction

Modular design of DC/DC converters has been widely used in industrial, military, or medical applications when high efficiency and power sharing are required This solution brings, also, the possibility to have flexible designs, just by combining several DC/DC blocks. In order to generate different voltage levels there are many options. The first one would be a Distributed Power Architecture (DPA), represented in Fig. 1. However, for higher powers, an Intermediate Bus Architecture (IBA) structure, as the one shown in Fig. 1b, has a better performance [2]. A regulated IBA structure (Fig. 1b) is normally composed by two stages. The first one (i.e. bus converter) takes a nominal input voltage (typically 48 V) and step it down to a range of 8V – 12 V [1]. The second stage is a point of load (PoL) converter that adapts the output voltage of the bus converter to the required voltage. This IBA structures have been used in industry, for many years, to distribute power with good performance. Other possibility is the unregulated IBA structure, as the one shown in Fig. 1c. This architecture is based on the use of an unregulated DC/DC transformer (DCX) that adapts the bus voltage level to the desired one. In general, it is more competitive than the regulated one due to its more optimized design of the passive components [2]. Nonetheless, due to its fixed gain, it must be specifically designed for given input and output voltages. IBA power scalability can be achieved by input-parallel, output-parallel connections, while voltage scalability can be achieved by series connections. In both cases, tolerances in components normally force the use of specific power-sharing techniques, being too complex or based on centralized controllers [3],[4].

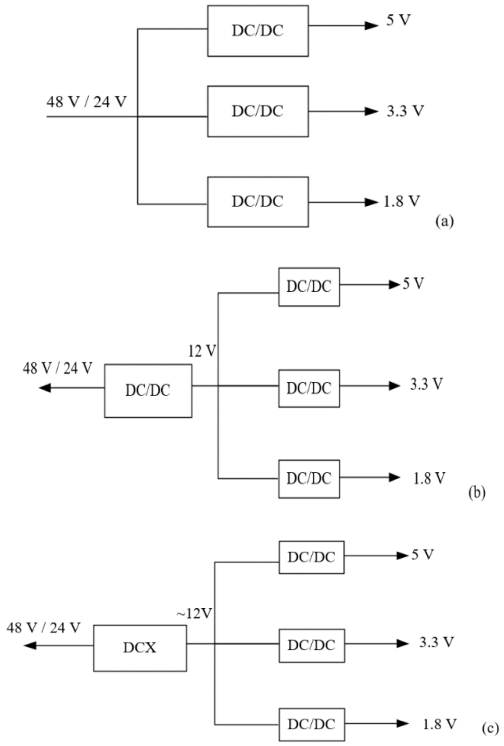


Fig. 1. DPAs for lower power applications. (a) conventional, (b) regulated IBA, (c) unregulated IBA

The aim of this work is analyzing a specific DCX modular topology for an unregulated IBA structure and how can be connected in ISOP (Input Series – Output Parallel) or IPOP (Input Parallel – Output Parallel) configurations for voltage and power scalability. In both cases good power sharing and input voltage sharing are achieved without requiring a complex control stage, being this its main advantage. The control stage only needs a common straight forward synchronization signal, so all the DCX modules will start each switching period at the same time. Thanks to this, the same topology can be easily used for different input voltage ranges by selecting the number of modules in ISOP connection (forming a string), equally sharing the input voltage, instead of redesigning the whole DCX converter. Similarly, power scalability is achieved by IPOP connection of these strings.

Traditional DCX architectures found in literature [5] are many times based on LLC resonant topologies because they can achieve high efficiencies due to their soft switching characteristics and because their high-power density. However, tolerances in their passive components can affect negatively the voltage and power sharing because their static gain is dependent

on these passive component values. This forces the use of complex controls, centralized or master-slave structures, with their associated drawbacks, like being a weak point from the reliability point of view. The DCX topology used in this work presents a tolerance immunity because its static gain is only dependent on the turn ratio of the magnetic transformer.

This article is organized as follows. Section II describes DCX topology selected for this work. Section III describes the operation of different DCX modules connected. Section IV describes the robustness of this topology against tolerances in the resonant circuit. Experimental results are shown in Section V. Finally, the main conclusions to this work are shown in Section VI.

II. THE DC/DC TRANSFORMER TOPOLOGY (DCX)

The DCX topology (Fig. 2.a) has been introduced in [6] and consists in a resonant full bridge converter operating with fixed duty cycle and fixed switching frequency. In the secondary side, a center-tap rectifier is implemented. In each half switching period, the resonance takes place between the leakage inductance of the transformer (L_{lk_i}) and the output capacitor (C_O). If L_{lk_i}, Co and f_{sw} are conveniently selected, current will start and end at zero level at any load condition, leading to the waveforms shown in Fig. 2.b and ensuring ZCS in secondary diodes. If magnetizing current is conveniently adjusted, ZVS is reached on primary MOSFETs even at no load situation. All of this leads to a very high efficiency.

This topology presents a fixed static voltage gain only dependent on the turns ratio 'n' of the magnetic transformer (1):

$$V_o = V_{in} \cdot n \tag{1}$$

This is the main advantage of the topology for this application in comparison to other options, such as DCXs based on the LLC resonant converter [5], whose static gain is dependent not only on the switching frequency, but also on the parameters of its resonant tank. This dependence forces the necessity of specific controls to ensure power and voltage sharing when tolerances are considered [3], [4]. On the other hand, the turns ratio of a transformer is a fixed value independent from tolerances or control signal variability. This makes the equalization of input voltages between series- or parallel-connected modules straightforward (this aspect will be fully analyzed in Section IV). This also makes possible to have a reduced set of predesigned transformers (with different turn ratios) as a straightforward way of changing the static gain of the module during its assembly process, without compromising standardization.

The resonant current and the output voltage can be expressed as:

$$v_o(t) = (V_{in} \cdot n) - I_o \cdot \sqrt{\frac{L_{lk_i}}{C_o}} \cdot sin(\omega_i \cdot t) + (v_O(0) - V_{in} \cdot n) \cdot cos(\omega_i \cdot t) \tag{2}$$

$$i_{lk\_i}(t) = I_o \cdot (1 - cos(\omega_i \cdot t)) + \frac{V_{in} \cdot n - v_o(0)}{\sqrt{\frac{L_{lk_i}}{C_o}}} \cdot sin(\omega_i \cdot t) \tag{3}$$

$$\omega_i = \frac{1}{\sqrt{L_{lk\_i} \cdot C_o}} \tag{4}$$

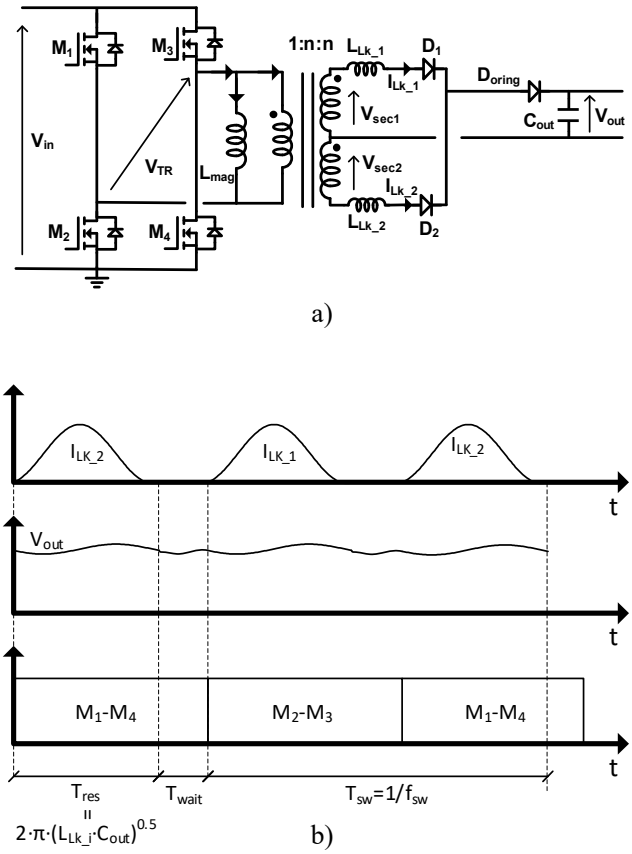


Fig. 2. a) Schematic of the DCX module; b) Main waveforms

where $v_o(t)$ is the output voltage, V_{in} the input voltage, 'n' the turn ratio of the magnetic transformer, I_o is the output current, L_{lki} is the leakage inductance of the winding 'i' (as well as the resonant inductance), C_o is the output capacitance (which is also the resonant capacitance), $v_o(0)$ is the output voltage at the beginning of each resonance, $i_{lk\_i}(t)$ is the resonant current through leakage inductance 'i'. It should be considered that the time 't' restarts in zero for each resonant period (i.e. for each half switching period of the topology). The magnetizing inductance does not play any role in the resonant tank, as in the case of the LLC resonant converter [5]. This alleviates the design constraints of the transformer and makes easier the integration of the resonant inductance and the transformer in a single core. The magnetizing inductance is only tied to the condition of reaching ZVS under any load condition, so its value can be wisely adjusted.

The output capacitor is the resonant capacitor as well. This reduces the number of components, but it may also increase the output voltage ripple. In general, this is a drawback that makes this topology unsuitable for many applications. Nonetheless, in any application in which this converter in not supplying a final load directly, but a second stage converter, the high-frequency ripple of the DCX output capacitor will be filtered by the EMI filter of the second stage. This is the case of the IBA structure mention in Section I or any two-stage topology, in which EMI filters are mandatory. Moreover, the proposed DCX stage will presumably have a higher switching frequency than the second stage, so the filtering effect should be enhanced.

III. MODULAR OPERATION

Thanks to the simple static gain of the topology, which does not depend on the values of the resonant components, several DCX converters [7]-[10] can be connected in ISOP or IPOP reaching automatic input-voltage and power sharing without a complex central control, only sharing a simple clock signal (synchronization signal). The analysis assumes that all the DCX modules have equal values of L_{lk} for both windings (L_{lk}=L_{lk1}=L_{lk2}), and of L_{lk} and C_o for all modules. In Section IV, the effect of the tolerances in these values will be shown.

The key point of the proposed system is that the PoLs of a given IBA structure operate with a common input voltage. Therefore, there is no need to connect the output ports of the DCX modules in series to adapt the overall output voltage. Their outputs can be then designed for that predefined voltage and connected in parallel for power scalability. According to (1), this common output voltage to all the DCX modules leads to an equal input voltage level in all the modules, whether they are connected in series or in parallel. Hence, the input voltage is evenly shared by all the serialized modules without specific control. Once the input voltage range adaptation is achieved by selecting the appropriate number of serialized modules (m_s) and their static gain (G_v) through the implemented transformer, the resulting scheme can be parallelized 'm_p' times to reach power scalability (see Fig. 3).

For the mathematical analysis, the several DCX modules connected ('m_s · m_p' modules) can be represented as in Fig. 4.a), where the square-pulse voltage sources represent the voltage at the secondary side of the magnetic transformers, with a given period with zero voltage applied to the transformer (dead times). Assuming a clock signal synchronizing all the DCX modules, the phase of all the square-pulse voltage sources is the same. As already explained, the input voltage of all the modules is equal, given equation (1) and the parallel connection of all the modules at their output. Consequently, the amplitude of those square-pulse voltage sources is equal as well. Hence, the voltage at the switching nodes (SN_{ij}) is equal for every module in every instant, so they are electrically equivalent, and the system can be represented as in Fig. 4.b), where all the resonant tanks are connected in parallel. Thus, the output voltage of this equivalent circuit is:

$$v_o(t) = (V_{in} \cdot n) - I'_o \cdot \sqrt{\frac{L_{lk}}{C_0 \cdot (m\_s \cdot m\_p)^2}} \cdot sin(\omega' t) + (V_C(0) - V_{in} \cdot n) \cdot cos(\omega' t) \quad (5)$$

being,

$$\omega' = \sqrt{\frac{1}{L_{lk} \cdot C_o}} = \omega \quad (6)$$

$$I'_o = I_o \cdot (m\_s \cdot m\_p) \quad (7)$$

The angular frequency is equal for a single resonant tank and for the equivalent one (see (4) and (6)). Replacing (6) and (7) in (5):

$$v_o(t) = (V_{in} \cdot n) - I_o \cdot \sqrt{\frac{L_{lk}}{C_0}} \cdot sin(\omega \cdot t) + (V_{Co} - V_{in} \cdot n) \cdot cos(\omega \cdot t) \quad (8)$$

The output voltage is the same for one stand-alone module or for several modules connected in any configuration at their input (see (2) and (5)). Therefore, the resonant currents can be calculated as (9):

$$i_{lk\_i}(t) = \frac{1}{L_{lk}} \cdot \int_0^{\frac{2\cdot\pi}{\omega}} [V_{in} \cdot n - v_o(t)] \cdot dt = I_o \cdot (1 - cos(\omega \cdot t)) + \frac{V_{in} \cdot n - v_O(0)}{\sqrt{\frac{L_{lk}}{C_o}}} \cdot sin(\omega \cdot t) \quad (9)$$

As can be seen from (3) and (9), all the resonant currents are equal and are not affected by the number of modules or by the array configuration (bear in mind the assumption of no tolerances in the resonant inductors). This means that, given the common output voltage, accurate power sharing between all the modules can be achieved without any kind of dedicated or complex sharing control, just with a clock signal that synchronizes all the primary full bridges. Delays or problems related to the transmission of this clock signal are minor, and they can be easily overcome.

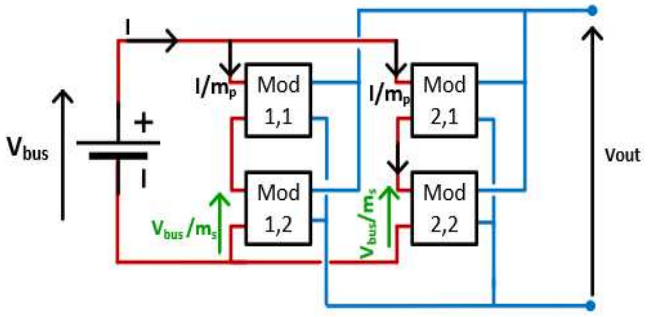


Fig. 3. Modular connection between DCX modules

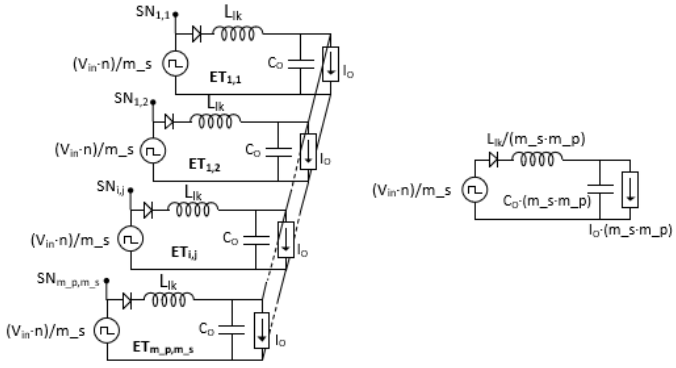


Fig. 4. a) Equivalent circuit for the DCX presented when resonant conditions are observed. b) simplified equivalent circuit derived from a)

IV. TOLERANCE INFLUENCE

Many DC/DC transformers use the LLC resonant topology in order to have high efficiency and power density [5]. Nonetheless, these LLC converters have a static gain dependent not only on the switching frequency but also on the parameters of its resonant tank (i.e. resonant capacitor, leakage inductance and magnetizing inductance). This dependence forces the necessity of specific and complex control stages to ensure power and voltage sharing when tolerances in the resonant elements are considered [3],[4]. On the other hand, the DCX topology used in this work has a fixed static voltage gain only dependent on the turn ratio of the magnetic transformer. This is a main advantage as the turns ratio of a magnetic transformer is a fixed value, robust against tolerances, aging, or control signal variability.

This ageing and tolerance analysis is valid not only for different values of L_{lk} between different modules, but also between leakage inductances of the same module (L_{lk1} and L_{lk2}).

Even when the resonant tanks of different modules are not exactly equal, if they fulfill the imposed conditions of starting and ending each resonant period with zero current, equation (1) is still valid, leading to the same square-pulse waveform in the input of each resonant tank, as previously explained using Fig. **4**. Therefore, it is possible to establish the expressions for the equivalent inductance and capacitance as before, but considering the drift (due to aging and constructions tolerance) affecting each component as well:

$$\frac{1}{L_{eq}} = \frac{1}{L_{lk}} \cdot \sum_{i=0}^{m} \frac{1}{1 + dr_{L\_i}} \cdot \tag{10}$$

$$C_{eq} = C_o \cdot \sum_{i=0}^{m} 1 + dr_{C\_i} \tag{11}$$

where 'm' is the total number of modules, and dr_{L_i} and dr_{C_i} are the relative drift (positive or negative) of the inductor and the capacitor in module 'i'. Therefore:

$$v_o(t) = V_{in} \cdot n - I'_o \cdot \sqrt{\frac{L_{eq}}{C_{eq}}} \cdot sin(\omega' \cdot t) + (v_O(0) - V_{in} \cdot n) \cdot cos(\omega' \cdot t) \tag{12}$$

$$\omega' = \sqrt{\frac{1}{L_{lk} \cdot C_o} \cdot \sum_{i=0}^{m} \frac{1}{1 + dr_{L\_i}} \cdot \frac{1}{\sum_{i=0}^{m} 1 + dr_{C\_i}}} \tag{13}$$

$$I'_o = I_o \cdot m \tag{14}$$

$$m = m\_s \cdot m\_p \tag{15}$$

With (12) it is possible to obtain the current through any resonant tank:

$$i_{lk\_i}(t) = \frac{1}{L_{lk\_i}} \cdot \int_0^{\frac{2 \cdot \pi}{\omega'}} [V_{in} \cdot n - v_o(t)] \cdot dt \tag{16}$$

which yields:

$$i_{lk\_i}(t) = \frac{L_{eq}}{L_{lk\_i}} \cdot I_O \cdot m \cdot (1 - \cos \omega' \cdot t) - \frac{Vc_0 - V_{in} \cdot n}{\omega' \cdot L_{lk_i}} \cdot \sin \omega' \cdot t \tag{17}$$

Considering these equations, it is clear that aging and tolerance does not compromise the operation of the DCX modules, if a common synchronization signal is used. As all the modules share the same input and output voltage levels, the resonant currents through the different inductors start at the same time and reach zero also at the same time (see (17)). This way the initial assumption, regarding current, is then verified and equation (2) is still valid.

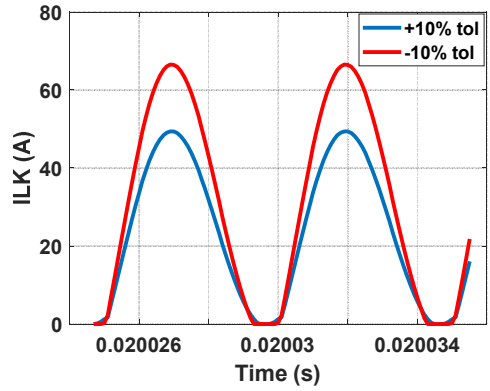
Nonetheless, as can be derived form (17), depending on the module inductance value, its current peak value will change, leading to a power imbalance between modules. This power imbalance represents a drawback of the proposed topology and the prize to pay for the simple synchronization and the straightforward series/parallel connection of the modules at the input port. Nonetheless, as can be derived from (17), the capacitor value drift does not affect the current sharing between modules. Therefore, the power imbalance is considerably lower than in other DCX topologies in which the resonant capacitor is not parallelized between the modules (for instance, the LLC resonant converter [5]). In this example, value drifts of 10%, have been considered.

Fig. 5 shows a simulation of the resonant currents through the rectifier diodes (I_{lk}) for two modules in IPOP connection when LLC topology is used (Fig. 5 b) and when the proposed topology is used (Fig. 5 a). A center-tap rectifier has been used in both topologies. The control in both topologies is the same as well; a simple PWM signal synchronized among all the modules. In this simulation, ±10% tolerances in the resonant components have been considered for all the DCX modules. This way, it is possible to see how when the LLC topology is used without a specific control as in [3], [4], the tolerances lead to I_{lk} currents differing in amplitude and in phase. With the proposed DCX system, there is no phase difference between the resonant currents, (i.e. both starts and ends at the same point), and the amplitude differences are smaller than with the LLC architecture. This better performance of the DCX module proposed in this work is based on the equivalent resonant inductor (L_{lk}) for all the IPOP modules, being the parallel combination of all the L_{lki}, in the same way as happens with the resonant capacitor (C_O) (see Fig. 4 b). In the LLC topologies, only the equivalent magnetizing inductance is the parallel combination of the magnetizing inductance of each module.

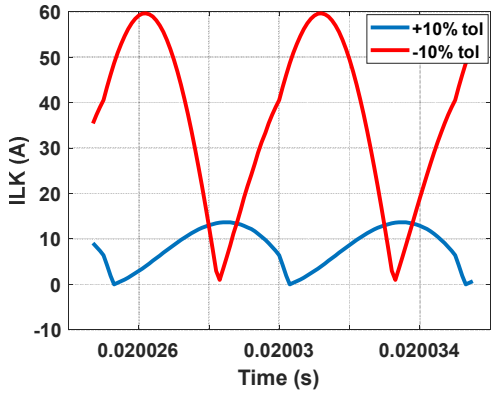
Even when perfect synchronization can be achieved, the change in the common resonant frequency (see (13)) may lead to the loss of ZCS and, consequently, to a reduction in efficiency. Obviously, the switching period must be chosen so that enough time is given to the resonant current to reach zero. Hence, the switching period, and thus the period of the synchronization signal, must be equal to two times the resonant period in the worst case. This worst case is represented by having all the resonant elements of all the DCX modules affected by the maximum positive drift, thus achieving the longest resonant period. From (13):

$$T_{sw} = 2 \cdot \frac{2 \cdot \pi}{\omega'} = \frac{4 \cdot \pi}{\sqrt{\frac{1}{L_{lk} \cdot C_o} \cdot \frac{1}{1 + dr_{L\_i}} \cdot \frac{1}{(1 + dr_{C\_i})}}} \tag{18}$$

In this case, the situation would be the one depicted in Fig. 2.b with T_{wait} equal to zero. This resonant period has to be adjusted at design stage and cannot be changed during operation, or a centralized and more complex control stage would be required.



a)



b)

Fig. 5. Currents through the rectifier diodes in two modules in IPOP connection using a) DCX used; b) LLC topology

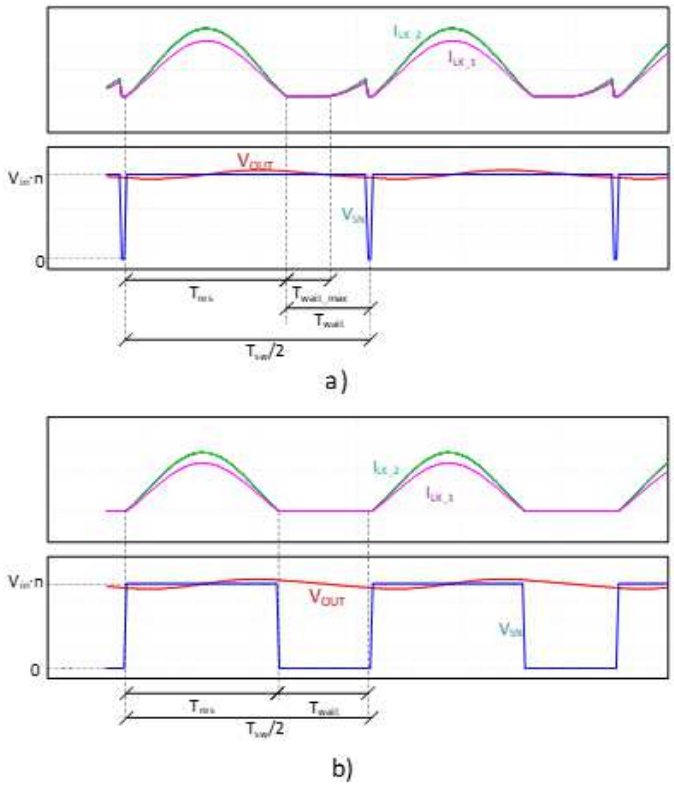


Fig. 6. a) Resonant current when T_{wait} is longer than T_{wait_max}; b) same situation but with the transformer short-circuited when the resonant current reaches zero until new switching period begins

In any other case, the resonant period will be shorter than half the maximum switching period, leading to a situation as the one depicted in Fig. 2.b with T_{wait} different from zero, where ZCS is still achieved but, during some part of the switching period there is no energy transference between primary and secondary of the DCX. During this time with zero resonant current, energy provided to the load comes exclusively from the output capacitor, leading to its voltage reduction. If this period is long enough, the situation will turn into the one shown in Fig. 6.a for two parallel modules. The output voltage V_{out} becomes lower than the voltage in the secondary side of the magnetic transformer (V_{in}·n) during T_{wait}, forward biasing the rectifier diode and leading to a new resonance to take place. This resonance will be cut as soon as $T_{sw}/2$ is reached (a new half switching period started), losing ZCS in the diode. Moreover, the whole performance in the system is affected as the premise of starting and finishing each resonant period at zero current is not fulfilled. It is possible to calculate the output voltage evolution and obtain the maximum value for T_{wait}, denoted as T_{wait_max}, before the resonance is restarted inside the same switching half period (see Fig. 6a):

$$V_O(T_{res}) - \frac{I_o \cdot \mathrm{m} \cdot T_{wait\_max}}{C_o \cdot \sum_{i=0}^{m} 1 + dr_{C_i}} = \mathrm{V}_{in} \cdot \mathrm{n} \tag{19}$$

$$T_{wait\_max} = [V_O(T_{res}) - \mathrm{V}_{in} \cdot \mathrm{n}] \cdot \frac{C_o \cdot \sum_{i=0}^{m} 1 + dr_{C_i}}{I_o \cdot \mathrm{m}} \tag{20}$$

where $V_O(T_{res})$ is the output voltage right when the resonant current reaches zero.

In order to avoid restarting the resonance inside the same half period, the full bridge control scheme can be modified, and the primary side of the transformer can be short-circuited (by turning on MOSFETs M_1-M_3 or M_2-M_4) once the current through the diodes becomes zero. In this way, ZCS is still achieved but it would be impossible to start the unwanted resonance unless the output voltage falls below zero. The short-circuit will be released when the next half period starts according to the synchronization signal. This strategy can be easily implemented with a pair of small-size magnetic cores, a very simple analog circuit and a dc-blocking capacitor in the power stage (if required). With this strategy, the situation depicted in Fig. 6.a becomes the one in Fig. 6.b. As can be seen, as soon as the resonant current becomes zero, the voltage in the secondary side of the transformer is clamped to zero until a new half period needs to be started. This enlarges the value of T_{wait_max} to:

$$T_{wait\_max} = V_O(T_{res}) \cdot \frac{C_o \cdot \sum_{i=0}^{m} 1 + dr_{C_i}}{I_o \cdot \mathrm{m}} \tag{21}$$

This new value of T_{wait_max} ensures that the resonance is not restarted for any reasonable drift value which, as has been said, can be in the 10% range. This control variation is independent from the rest of the modules and does not compromise modularity or simplicity. Conditions for ZVS in the primary switches are dependent on the magnetizing current only (not on load current) and short-circuiting the primary side keeps the magnetizing current at the value it had when the short-circuit was applied. Therefore, ZVS and efficiency are not affected either.

To sum up, although the topology was already proposed in [5], the idea of connecting several of these DCX modules in series or parallel, its tolerance immunity analysis, and the method for not losing ZCS due to tolerances in the resonant tank components are considered as new contributions in this work.

V. EXPERIMENTAL RESULTS

This section presents experimental results using the designed DCX prototypes. On the first part, experimental results for one DCX module is shown. On the second part, several DCX modules are connected in Input-Parallel Output-Parallel (IPOP) and Input-Series Output-Parallel (ISOP) configurations.

A. Experimental results for a single DCX module

Four prototypes of DCX modules have been designed and built according to the schematic in Fig. 2. Its main characteristics are listed in Table I. A photograph of one of the prototypes is shown in Fig. 7, where MOSFETs are highlighted in green and diodes in red. Fig. 8 shows a detail of the V_{DS} and V_{GS} transition of one of the MOSFETs; it can be seen that ZVS is achieved. Fig. 9 shows the drain-source voltage in M_4 primary transistor (V_{DSM4}), the resonant currents through the rectifier diodes (I_{LK}), and the output voltage (V_{OUT}) behavior. It is possible to see that the output voltage ripple is not negligible in the DCX topology, however this ripple can be easily filtered considering the input filter of a DC/DC converter connected downwards. Fig. 10 shows the same waveforms as Fig. 9 but considering the voltage downwards this second-stage input filter. This way, it is possible to see how the voltage ripple is minimized without affecting the resonant current behavior. As can be seen, ZVS can be reached in primary switches and ZCS in secondary ones. Therefore, the efficiency of each module is very high, as shown in Fig. 11, reaching 98% at the rated power and around 97% at half the rated power. Different efficiencies shown in Fig. 11 are due to the two different versions of the prototypes designed.

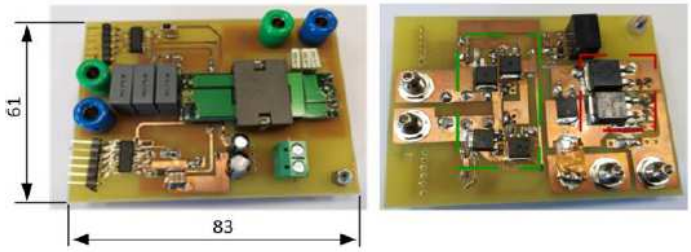


Fig. 7. Photograph of the prototype

Table I. Main specifications of the DCX designed

Input voltage (V_{in})	56 V
Output voltage (V_O)	28 V
Rated power (P_O)	200 W
Switching frequency (F_{SW})	400 kHz
Clock Source	ALTERA MAX 10M50DAF484C7G
Leakage inductance (L_K)	65 nH
Output capacitor (C_O)	0.3 µF
MOSFETs (M_1, M_2, M_3 y M_4)	PSMN063-150D
Rectifier diodes (D_1, D_2)	NRVBB60H100CTT4G
Magnetic core	EIR22/6/16
Magnetic material	N97
Drivers	IR2110 / SI8238BB
Turns	4:2

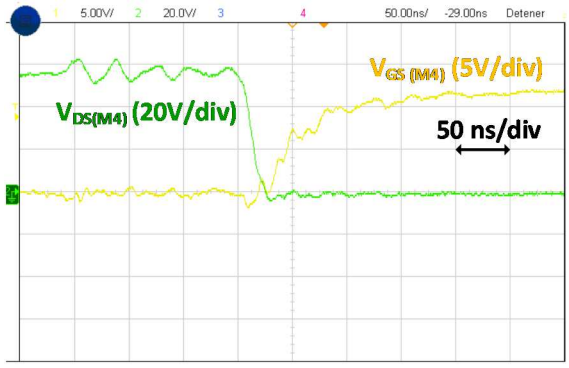


Fig. 8. ZVS achievement on primary switches

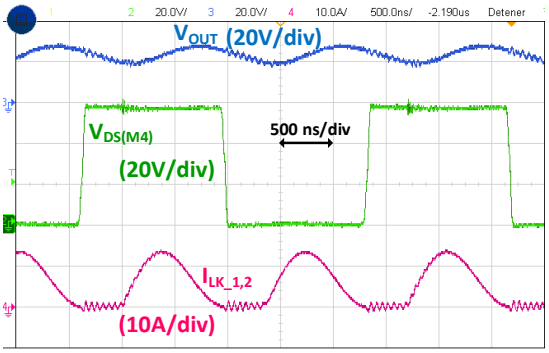


Fig. 9. V_{DS} (M_4), V_{OUT} and $I_{LK\_1,2}$ through the diodes

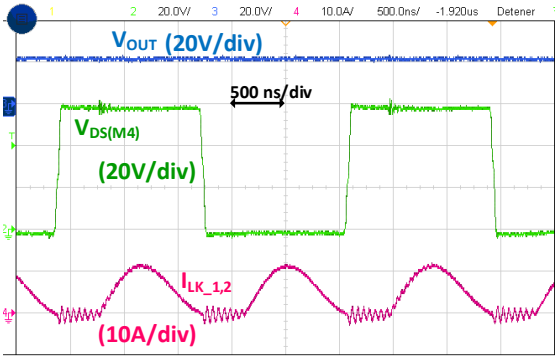


Fig. 10. V_{DS} (M4), V_{OUT} and $I_{LK\_1,2}$ through the diodes, considering the DC/DC converter input filter

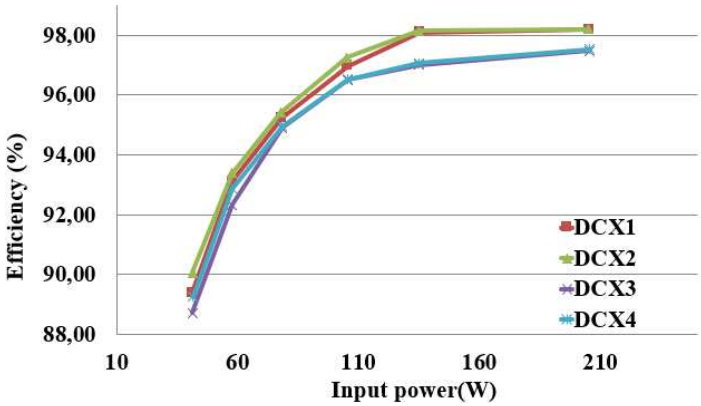


Fig. 11. Efficiency comparison between DCX modules

B. Experimental results for two DCX modules in IPOP configuration

Two DCX modules have been connected in IPOP configuration, increasing the rated power of the full system. Fig. 12 shows the output voltage (V_{OUT}) and the resonant currents through the diodes ($I_{LK\_1,2}$) for both DCX modules. In this case, variations in the leakage inductances have been artificially introduced in each module to increase the effect of the drifts and tolerances in the transformers. As can be seen, this does not affect the resonant behavior of the modules regarding ZCS. Both resonances finish at the same time (i.e. both present the same pulsation), but the amplitude of the resonant currents are different between both modules. As explained before, this is the price to pay for a simple control system based on a single clock signal. Nonetheless, it should be taken into account that this power deviation is relatively small, and it is not influenced by capacitor tolerance or aging. In this test, each DCX module is around the rated power (i.e. 200 W), making that the full power processed by the system will be 400 W (i.e. twice the rated power).

C. Experimental results using four DCX modules

By combining four modules using IPOP and ISOP configurations it is possible to build a system whose nominal input voltage is twice (i.e. 112 V) the rated voltage of one module (i.e. 56 V) while the output voltage is still equal to 28 V. At the same time, the rated power of the whole system (i.e. 800 W) is four times the rated power of a single DCX module (i.e. 200 W). Fig. 13 shows the combination of four modules using IPOP and ISOP configurations. Sub 1 and Sub 2 blocks represent the IPOP combination of a pair of modules, while both blocks are serialized at their inputs. Fig. 14 shows the input voltages in both subsystems (close to 56 V) and the output voltage (V_{OUT}) of the whole system (28 V). As can be seen, the input voltage is perfectly shared among the modules connected in series with the simple control proposed.

Fig. 15 represents the resonant currents through the rectifying diodes in the four modules (I_{DCX1}-I_{DCX4}) and Fig. 16 shows the average value of two of them. In this scenario, the leakage inductances were not artificially modified, as in Fig. 12, but kept the values resulting from the standard fabrication method (i.e. only affected by tolerances, but not aging). As can be seen, the resulting differences in the amplitudes of the resonant currents are small. This is mainly due to the high replicability of planar transformers whose windings are built with PCBs. As they are all connected in parallel at the output, power sharing is as accurate as current sharing.

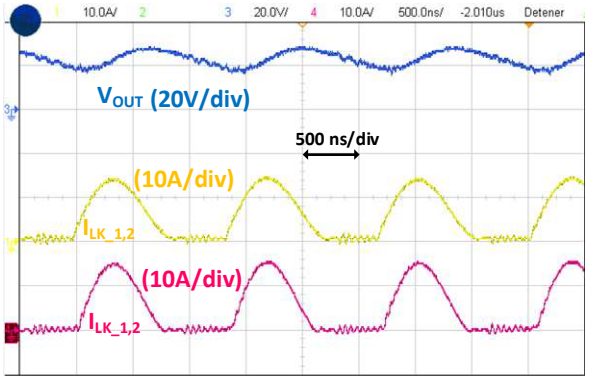


Fig. 12. V_{GS} (M_4) V_{OUT} and $I_{LK\_1,2}$ for two DCX modules in IPOP

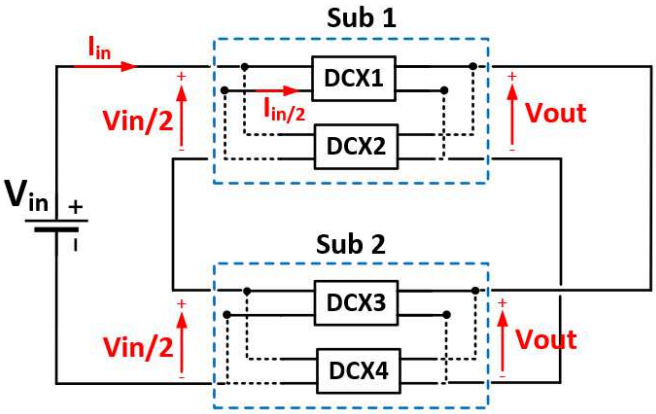


Fig. 13. Connection between four DCX modules

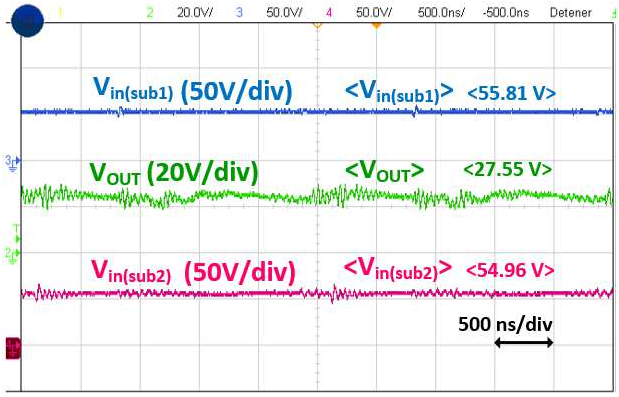


Fig. 14. Input voltages (V_{in}) for sub1 and sub2 with the whole system output voltage (V_{OUT})

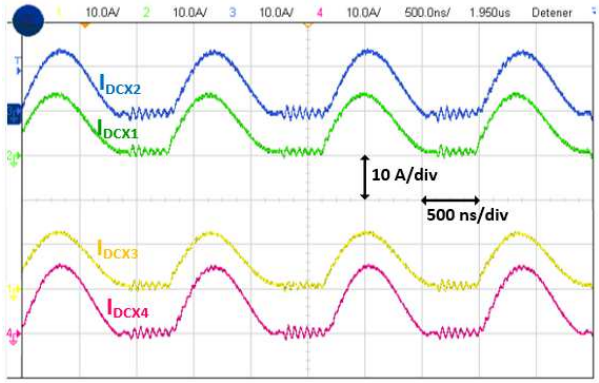


Fig. 15. Currents through the rectifier diodes in the four DCX modules. The shared power per module is nearly 200 W

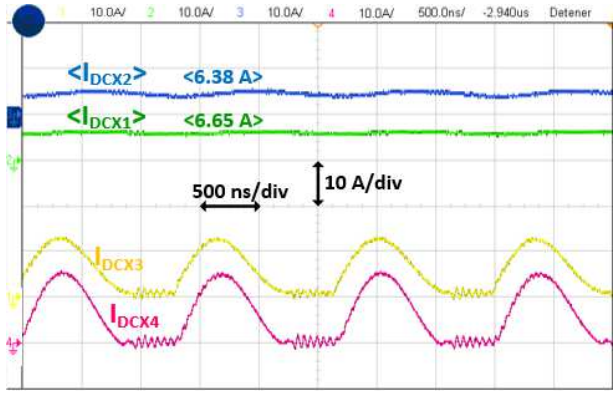


Fig. 16. Average current through DCX_1 and DCX_2 modules and resonant currents through the rectifier diodes in the DCX_3 and DCX_4 modules

VI. CONCLUSIONS

This work analyses the modular operation of a DCX topology used in distributed power architectures. It is based on an unregulated bus architecture, where the DCX adapts the intermediate bus voltage. It is a resonant topology in which high efficiencies can be achieved thanks to ZVS and ZCS at any load. Also, given the application, their outputs will be always connected in parallel, while their inputs can be connected in series or in parallel for both, voltage, and power scalability, respectively.

Its static gain is only dependent on its transformer turns ratio, which is a quite robust parameter against tolerances. Therefore, input voltage sharing is automatically achieved, with the only requirement of a simple synchronization signal. Regarding power sharing, it is low dependent on tolerances, so a good sharing can be achieved without a complex, or centralized control either.

The simplicity of this topology implies that the output capacitor is the resonant capacitor as well. The output voltage ripple is then not negligible. However, this high frequency ripple can be easily filtered without affecting the resonant behaviour and the modular operation of the proposed DCX modules, as shown in the experimental results presented in this work. These experimental results also show the optimum power and voltage sharing between modules, as well as the high efficiency they can achieve. These characteristics, along with a high efficiency and a correct power and voltage sharing between the DCX modules, make this solution especially suitable for intermediate bus architectures.

ACKNOWLEDGEMENTS

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