Adaptation and control of a latching current limiter based on a SiC N-MOSFET

Abraham López[1], Pablo F. Miaja[1], Manuel Arias[1], M. Fernández-Costales[1] and Arturo Fernández[2]
[1]Universidad de Oviedo, Electronic Power Supply Systems Group (e-mail: lopezabraham@uniovi.es)
Campus Universitario de Viesques, 33204 Gijón, Spain
[2]Electrical Power Management Section European Space Agency (ESA), Noordwijk, Netherlands

***Abstract*: Latching current limiters (LCLs) are circuits used for electrical load control on spacecrafts. They provide enhanced over current protection, improving reliability. LCL classic implementations are based on the use P-MOSFETs as the main current limiting device. However, new wide bandgap materials (WBG) offer the possibility to operate at higher voltages and, allegedly higher temperatures. Therefore, it exists the possibility to design an LCL architecture based on a SiC N-MOS device. In order to control the LCL and to adapt its working behaviour to a different N-MOS, the most important stages are the analog isolator (DCX) which is the one that controls the gate-source voltage level of the N-MOS, and the current control loop in charge of react if the sensed current is higher or not regarding the current reference. This way, this work presents a guideline for the design of the DCX and the current control loop stages. Finally, some experimental results for a class 10 LCL, following the proposed designs, for a bus voltage of 100 V will be shown.**

***Keywords*: LCL, SiC N-MOS, wide bandgap devices, current protection.**

I. INTRODUCTION

The solid state current limiting switches are used in satellites to achieve power distribution in a safe way. In the European context these switches are called latching current limiters (LCLs), and its main function is to protect the main power bus against overcurrent on the spacecrafts. Considering a simplified satellite scheme, as the one described on Fig. 1, the LCLs are in the distribution system, just between the main power bus and the secondary power system.

LCLs can be considered as "intelligent fuses" or "intelligent switches". In normal operation, the LCL allows the current demanded by a load to flow if this current is lower than a preestablished limit. If the current demanded is higher than this limit, the LCL regulates the current according to the preestablished limit during a specific time (i.e. trip-off time). If during this time the current does not go below this limit, the LCL will isolate the load. This load could be reconnected in the future by telecommand.

Traditional LCL architectures are based on P-MOSFETs working as the main limiter devices, due to its easiness to control them. If the source terminal is connected to the main bus, it is only necessary to use a lower voltage level on the gate. The voltage ranges for high power busses are about 100 V and 120 V. However, these P-MOS devices present higher values for the channel resistance (R_{ON}). This way, for higher powers demanded by the loads, the conduction losses of these semiconductors increase as well. This way, in order to achieved higher efficiencies it will be necessary to replace the P-MOS devices for N-MOS devices, which in general present lower R_{ON} values.

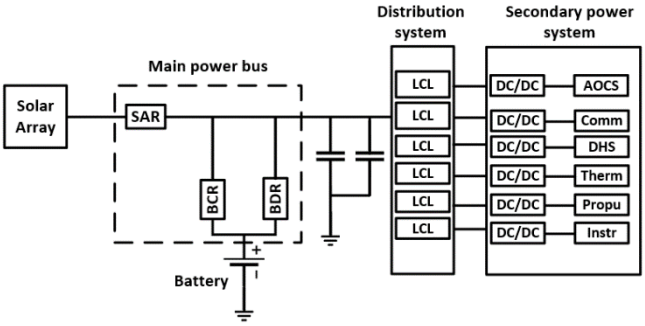

Fig. 1. Regulated power bus system on a satellite

In a N-based LCL architecture, the drain of the N-MOS will be connected to the bus, and the source will be connected to the load side.

The main problem using N-MOS devices is that to control them it is necessary that the gate voltage level has to be higher that the source voltage one. This way, it is necessary to have some stage to transfer this control signal referred to the N-MOS source terminal. With the development of the WBG materials, specially, silicon carbide (SiC) and gallium nitride (GaN), it is possible to have transistors based on these materials working at higher voltages and, allegedly, higher temperatures, reducing this way, the possible failure due to high junction temperature.

In the same way, some works in literature [1] and [2] present SiC N-MOS based LCLs where some design aspects are highlighted. For example, the semiconductors selection, the control stage, the auxiliary power supply, etc. The aim of this work is to present the analysis and results of the analog isolator stage (DCX) capable of controlling the gate of the N-MOS, referring this voltage level to the source terminal of the device. In the same way, this work presents some guidelines for the current control loop design, in terms of the changes that must be considered when a different N-MOS is used. A complete design of the proposed SiC N-MOS based LCL considering the timer and the undervoltage lockout (UVLO) sections is described in [2].

This paper is organized as follows. In Section II, the guidelines for the DCX stage design are shown. Section III describes the process for the current control tunning. Section IV focuses on the experimental results for a class 10 LCL using the proposed architecture. Finally, the main conclusions of this work are shown in Section V.

II. ANALOG ISOLATOR (DCX) DESIGN

Fig. 2 shows the LCL scheme based on a N-MOS. Its working behavior is based on the constant sensing of the current through the MOSFETs. After that, the error between the current sensed and the current reference will be integrated. Therefore, when the current sensed is lower that the device limit, the integrator will be saturated to a positive voltage level. The reference voltage for these types of systems will be the return of the bus voltage (V_{bus}) or an intermediate voltage. Conveniently translated to the gate-source voltage (V_{GS}) of the MOSFET, this positive voltage level will make that the N-MOS will be working in ohmic mode. However, if the current sensed through the MOSFET is higher than the limit, the integrator makes the voltage level lower. At this point, the N-MOS is working in active zone regulating the current to the reference value.

A) Oscillator design:

The DCX design is based on a DC/DC converter working in open loop. To control this converter, an oscillator, generating pulses for a switching frequency of 4 MHz and a duty cycle of 50% is used. The dynamic behavior of the DCX stage must not interfere with the dynamic of the current control loop. That is reason why the DCX stage operates in the 'MHz' range. Traditional strategies are based on pulse width modulation techniques. In this case, it was not possible to find a space qualified PWM modulator capable of working at those frequencies. This way, the DCX design is based on a fixed duty cycle, varying its input voltage. The oscillator to control the DCX has been implemented using the CD4093B integrated circuit [3], composed by four NAND gates with a Schmitt trigger input (see Fig. 3). This circuit implements an oscillator using an RC feedback network. Thanks to the tunning of this RC network is possible to determine the oscillation frequency.

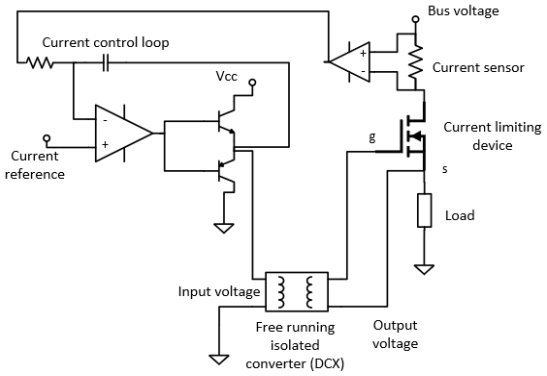

Fig. 2. DCX concept for a N-MOS based LCL

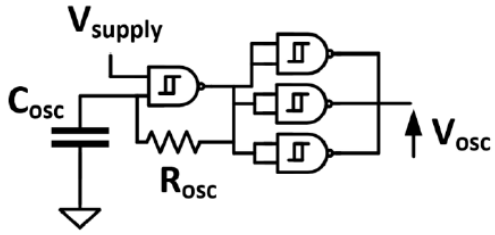

Fig. 3. Oscillator implementation for the DCX stage

B) DCX topology design:

Considering that the DCX stage will be integrated in the current control loop, it is necessary a precise static gain control between its input and output voltages. This way, the DCX stage designs have been adjusted in order to have a know static gain value between input and output voltages. Furthermore, the DCX stage will adapt the output voltages of the current control loop to the proper gate-source voltage values of the N-MOS.

The DCX implementation has been made considering an LLC topology. Fig. 4 shows the entire architecture composed by a half bridge inverter and a full wave rectifier. The detailed design of this topology can be found in [4]. It is a resonant topology where it is possible to achieved magnetic integration, making that the leakage inductance (L_{lk}) of the resonant transformer works as the resonant inductance of the DCX-LLC converter. The DCX design has been made considering the First Harmonic Approximation (FHA) [5]. In the LLC topology, the full bridge output voltage (V_{bridge}) is a square waveform with a duty 'D' close to 50%, a lower value of 0V and a maximum value of V_{in}. Therefore, the Fourier expression of the V_{bridge} is the one shown in (1):

$$V_{bridge} = V_{in} \cdot D + \sum_{k=1}^{\infty} \frac{2}{k \cdot \pi} \cdot V_{in} \cdot sin(k\pi D) \cdot cos(kD\omega_s t) \quad (1)$$

This way, the amplitude of the first harmonic (A_{FH}) will be the one determined for the expression (2), being the peak value the one determined by a 'D' of 0.5 (3).

$$A_{FH} = \frac{2}{\pi} V_{in} \cdot sin(\pi D) \quad (2)$$

$$A_{FH} = \frac{2}{\pi} V_{in} \quad (3)$$

Fig. 5 shows the equivalent circuit for the DCX-LLC topology under the FHA approximation. This way, it is possible to analyze the network resonant behavior (Z_{tank}) under the effect of an input sinusoidal function. R_{p1} and R_{p2} resistors are used to model the losses resistance of the magnetic transformer windings. Considering also, that it is possible to achieve magnetic integration, the resonant inductance of the half bridge inverter will be the L_{lk} value. Therefore, the design process will be based on the selection of the resonant frequency in the network formed by C_{tank} and L_{lk1} (i.e. leakage inductance of the primary side).

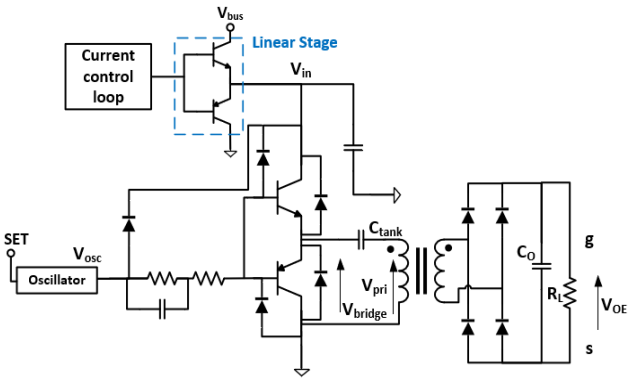

Fig. 4. Schematic of the DCX-LLC topology

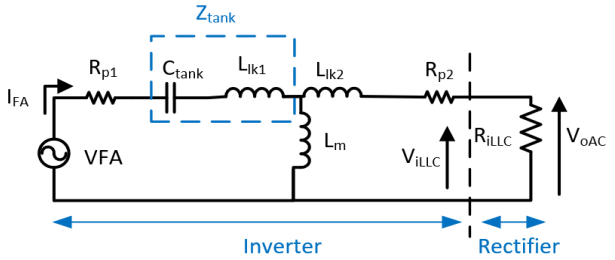

Fig. 5. Equivalent circuit of the DCX-LLC topology under the first harmonic approximation

The value of the equivalent impedance (Z_{tank}) in the resonant network can be determined according to (4):

$$Z_{tank} = j \cdot \left(\omega_S \cdot Llk_1 - \frac{1}{\omega_S \cdot C_{tank}}\right) \tag{4}$$

where $\omega_s = 2\pi \cdot F_{sw}$ is the angular frequency associated to the switching frequency (F_{sw}). Regarding the full wave rectifier, its equivalent input impedance is described in [6]. This way, considering an output capacitor (C_o) bigger enough to eliminate the switching frequency ripple, this rectifier behaviour can be model as a resistor (R_{iLLC}) with the value established on expression (5).

$$R_{iLLC} = \frac{8}{\pi^2} \cdot R_L \tag{5}$$

where R_L is the load resistor of the DCX-LLC topology. The voltage gain will be determined through the resonant network gain ($G_{tankLLC}$). Using R_{iLLC} it is possible to know the quality factor (Q_{tank}) of the resonant network, at the switching frequency, according to expression (6).

$$Q_{tank} = \frac{\left(\frac{F_R}{F_{SW}}\right) \cdot \omega_s \cdot Llk_1}{R_e} \tag{6}$$

$$R_e = R_{iLLC} + Rp_2 + Rp_1 \tag{7}$$

where F_R/F_{sw} is the ratio between the resonant frequency (C_{tank} and L_{lk1}), and the switching frequency**.** The expression of the $G_{tankLLC}$ can be obtained using the equivalent circuit in Fig. 3 with the expressions (8)-(10):

$$Z_1 = R_{iLLC} + Rp_2 + (j \cdot \omega_s \cdot Llk_2) \tag{8}$$

$$Z_{eq} = \frac{j \cdot \omega_s \cdot Lm \cdot Z_1}{j \cdot \omega_s \cdot Lm + Z_1} \tag{9}$$

$$Gtank_{LLC} = \frac{V_{iLLC}}{V_{FA}} = \left| \frac{Z_{eq}}{Rp_1 + Z_{tank} + Z_{eq}} \cdot \frac{R_{iLLC}}{Z_1} \right| \tag{10}$$

This way, with the $G_{tankLLC}$ value, it is possible to get the final expression for the value of the DCX-LLC topology gain (see (11)), which will be in terms of the network circuit gain, and the first harmonic amplitude (A_{FH}).

$$G_{DCX-LLC} = \frac{V_o}{V_{in}} = \frac{2}{\pi} \cdot sin(\pi \cdot D) \cdot Gtank_{LLC} \tag{11}$$

Apart from the amplitude, the bandwidth is another important aspect to consider in the DCX-LLC design process. Considering space applications, the bandwidth must comply with the ECSS [7]-[9] requirements, regarding the control loop speed to regulate the current. The bandwidth achieved here is in the range of the hundreds of 'kHz', offering a voltage gain, wide enough to comply with these requirements. Therefore, it is possible to establish a relationship between the DCX bandwidth, the resonant network Q_{tank} and the F_R/F_{SW} ratio.

This way, having a fixed value for the Q_{tank} and making variations of the F_R/F_{sw} ratio, it is possible to get Bode diagrams relating the input and output voltages of the DCX-LLC stage. The main steps for the analysis are listed here:

1. For a fixed Q_{tank} value it is possible to get a range of values for the resonant inductance (L_{lk1}).
2. For each L_{lk1} value it is possible to get a F_R/F_{sw} ratio using expression (6), according to (12):

$$\frac{F_R}{F_{SW}} = \frac{Q_{tank} \cdot R_e}{\omega_s \cdot L_{lk1}} \tag{12}$$

3. With the L_{lk1} range of values and the F_R/F_{sw} ratios, it is possible to obtain the values for the resonant capacitor (C_{tank}), according to expression (13):

$$C_{tank} = \frac{1}{\left[\left(\frac{F_R}{F_{SW}}\right) \cdot \omega_s\right]^2 \cdot L_{lk1}} \tag{13}$$

This way, for each F_R/F_{sw} ratio it is possible to get the pair of values for the resonant tank (i.e. L_{lk1} and C_{tank}). Considering this information it is possible to get a Bode diagram for each G_{tank}. Fig. 6 shows the Bode diagrams, without the DC gain, for a fixed Q_{tank} value of 0.1818 and for a F_R/F_{SW} ratio variation between 0.63 and 2.53. The discontinuous line in Fig. 6 represents the -3dB gain drop. The highest bandwidth appears when the F_R/F_{SW} ratio tends to 1. However, if the ratio is higher than unit, the bandwidth starts to drop. In this example, the highest bandwidth is 224.57 kHz for a F_R/F_{SW} ratio of 1.27, and the lowest bandwidth is 73.26 kHz for a F_R/F_{SW} ratio of 2.53.

The second analysis consists on having a fixed F_R/F_{SW} ratio modifying the Q_{tank} value. Again, the main idea is trying to analyze the bandwidth, in this case, due to a variation of the Q_{tank}. Fig. 7 shows the different Bode diagrams for a fixed F_R/F_{SW} ratio of 1.27 and for a Q_{tank} variation between 0.0912 and 0.3650. According to these analyses it is possible to make a connection between the F_R/F_{SW} ratio, the Q_{tank} parameter, the G_{tank} and the 3dB bandwidth. Therefore, to have a high bandwidth combined with a high gain it is necessary to design the DCX stage with a F_R/F_{SW} ratio close to 1 and with a low value of the Q_{tank} parameter. In the DCX-LLC implemented in this work, the Q_{tank} parameter is 0.092 and the F_R/F_{SW} ratio is 0.896. This way, it is possible to achieve a G_{tank} of 1.53.

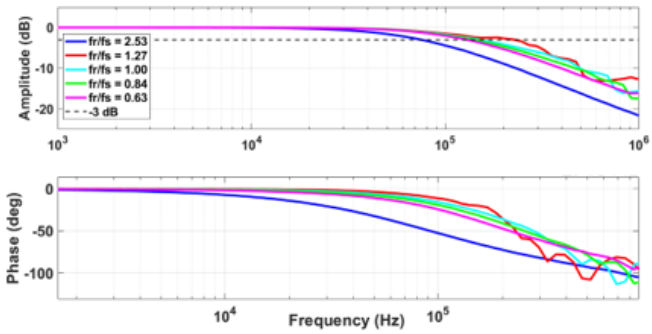

Fig. 6. Bode diagrams for a fixed Q_{tank} of 0.1818 changing the F_R/F_{SW} ratio

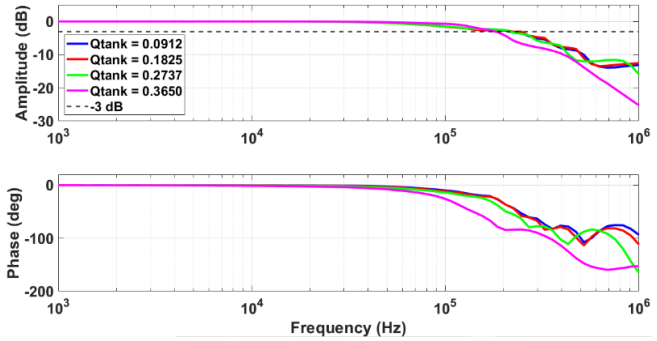

Fig. 7. Bode diagrams for a fixed F_R/F_{SW} ratio of 1.27 changing the Q_{tank}

III. CURRENT CONTROL TUNNING

The current control loop is the one that regulates the current depending on the LCL working behavior point. It is based on a type II regulator (Fig. 8). Thanks to the integrator, when the sensed current is lower than the reference one, it will saturate the control to positive, forcing the maximum voltage level at the end of the DCX stage (i.e. gate-source voltage level). On the other hand, if the sensed current is higher than the reference, the current control loop will reduce its voltage level at the end of the DCX stage making that LCL limit the current level to the reference one. In order to control de dynamic of this current control loop, it is necessary to know the current sensor behavior, the current source behavior of the N-MOS and the variations between the input and output voltage in the DCX stage (i.e. audio-susceptibility). In this case, two different SiC N-MOS have been selected, the SCT3022AL (ROHM)[10] and the SCTW90N65G2V (ST)[11].

This way, the steps to tunned and adapt the current control loop are:

The current sensor used in this work has been the LT6105[12]. Its dynamic behavior has been obtained by simulation using an AC analysis. After that, mathematical approximation has been made getting a transfer function (G_{sensor}) composed by 3 poles and 2 zeros.

The frequency behavior of the DCX (G_{DCX}) stage has been obtained through measurements, using a frequency response analyzer [13] from the prototypes implemented using the DCX-LLC topology.

The N-MOS current source behavior (G_{i_uc}) when the LCL is limiting the current can be obtained by mathematical analysis, considering some parameters in the N-MOS selected devices. In this case, it is assumed a R_{sense} value of 0.02 Ω. In the same way, different loads at the LCL output (Z_{load}) have been tested. This way, from the N-MOS datasheets it is possible to obtain the transconductance value (g_m), the drain-source resistance value (R_{ds}), the drain-source capacity (C_{ds}), the gate-source capacity (C_{gs}) and the drain-gate capacity (C_{dg}). For these analyses the R_{gate} value in both cases will be equal to 1 Ω. These parameters are better illustrated in Fig. 9 showing the small signal model between the DCX output and the N-MOS.

The DCX stage output impedance (Z_o) can be approximated by the parallel connection between the output capacitor (C_o) and the load (R_L) defined in Fig. 4.

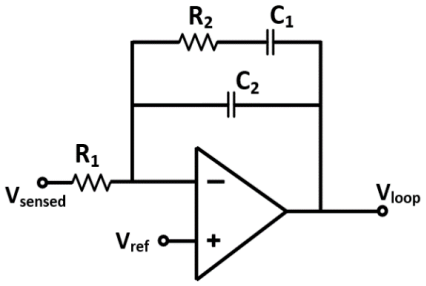

Fig. 8. Implementation of the type II regulator

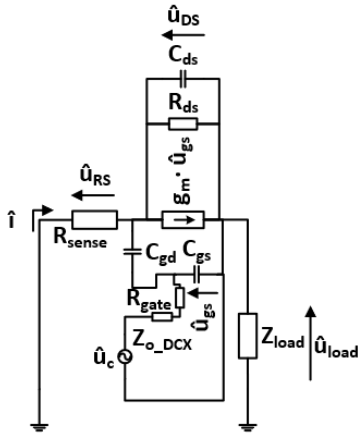

Fig. 9. Small signal model between the DCX output and the current through the N-MOS

At this point, it is possible to achieve an expression for the G_{i_uc} transfer function, adapted to the characteristics of both transistors, according to expression (14), where Z_{load} models the impedance that the LCL sees as a load. Therefore, considering the sensor dynamic behavior (G_{sensor}), the audio-susceptibility (G_{DCX}) and the dynamic of the N-MOSFET current source (G_{i_uc}), is possible to define the current control loop regulator of the LCL (15).

$$G_{i\_uc} = \frac{g_m}{\left(Zo_{DCX} + R_{gate}\right) \cdot C_{in} \cdot s + 1} + \frac{1}{\frac{1}{(R_{sense} + Z_{load})} \cdot \frac{gm \cdot Zo_{DCX} \cdot C_{dg} \cdot s}{Zo_{DCX} \cdot C_{dg} \cdot s + 1} + \frac{R_{ds} \cdot C_{gd} \cdot s + 1}{R_{ds}}} \tag{14}$$

$$G_{LCL} = G_{sensor} \cdot G_{uc\_uciso} \cdot G_{i\_uc} \tag{15}$$

Finally, to achieve of transfer function of the type II regulator, it is necessary to know the G_{LCL} expression and the values for the crossover frequency (F_c) and the phase margin (P_m). Table I shows the parameters obtained for the R_2, C_1 and C_2 values in the regulator (see Fig. 8), if R_1 uses a fixed value of 1 kΩ for both N-MOS. In these tests, the regulator is tuned to maintain a P_m value of 60 º while maximizing the bandwidth.

Considering the parameters shown in Table I, and the closest values, due to the real implementation, it is possible to get the final transfer function and, therefore, the dynamic behavior of the implemented regulator in the current control loop. Finally, Fig. 10 shows the Bode diagram for the complete current control loop plant (G_{LCL}) for different Z_{load} conditions.

Table I. Theoretical parameters for the type II regulator depending on the SiC N-MOS used

SCT3022AL (ROHM)	SCTW90N65G2V (ST)
R_1 = 1 kΩ	R_1 = 1 kΩ
R_2 = 515.72 Ω	R_2 = 144.51 Ω
C_1 = 116 nF	C_1 = 343 nF
C_2 = 328 pF	C_2 = 1.42 nF
g_m = 12.2 $Ω^{-1}$	g_m = 12.5 $Ω^{-1}$
C_{ds} = 400 pF	C_{ds} = 1300 pF
R_{ds} = 2 Ω	R_{ds} = 1.67 Ω
C_{gs} = 2000 pF	C_{gs} = 3800 pF
C_{dg} = 200 pF	C_{dg} = 200 pF

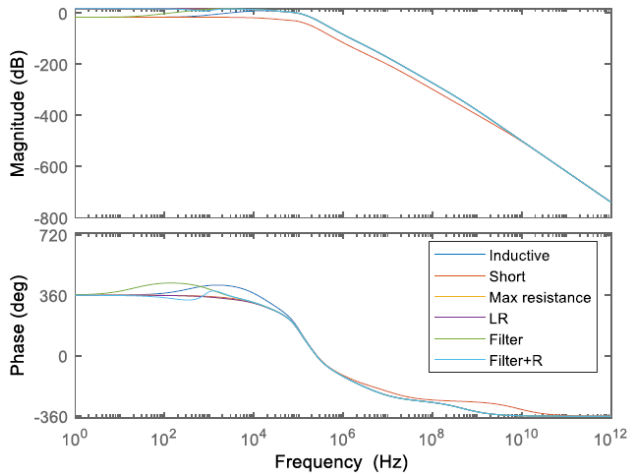

Fig. 10. Bode diagram, using the SCT3022AL SiC N-MOS, for the complete LCL current control loop plant, considering different Z_{load} conditions

According to Fig. 10, different Z_{load} situations have been considered in the G_{i_uc} transfer function to define the worst case for the LCL. The different situations are:

1. A pure short-circuit.
2. A resistor, considering the I_{lim} current level.
3. A pure inductance.
4. An inductance in series with the resistor used in 2).
5. A damped LC filter with a short-circuit at its output.
6. A damped LC filter with the resistor used in 2).

Considering the analysis done, a high Z_{load} value is detrimental for the LCL dynamic response. This way, the worst case in Fig. 10 is the "filter+resistor" one, due to is the one that presents the maximum load impedance at the output of the LCL.

IV. EXPERIMENTAL RESULTS

Experimental results show the behavior of the DCX stage and the current control loop when they are working in a class 10 LCL SiC based N-MOS prototype. In these tests, the bus voltage is about 100 V. Fig. 11 shows an overload test using the SCT3022AL N-MOS working at limiter device. It can be seen how the LCL carries the full current 10 A (I_{sense}). While this happens, the control loop voltage (V_{loop}) is saturated to positive. The DCX translates this voltage to the gate-source terminals of the N-MOS (V_{gs}). The voltage at the output of the half bridge of the DCX is represented as V_{priDCX}. It can be seen how it follows the loop voltage. Upon an overload, there is an initial overshoot of 37 A and then the LCL reacts limiting the current to 12 A.

This is achieved by the control loop adjusting its voltage, so the current is regulated. It can be seen how the half bridge voltage, and thus the V_{gs} level, follows it. Right after the short-circuit, the timer section starts to work (V_{Ctimer}), shutting down the LCL after a trip-off time of 1.5 ms (i.e. trip-off min for a class 10 LCL). This is achieved by the timer turning off the DCX. It can be seen how $V_{priDCX,}$ and then V_{gs}, goes to 0 V, turning off the MOSFET. Consequently, the current goes to 0 A and the control loop saturates to positive. Fig. 12 shows the same waveforms using the SCTW90N65G2V SiC N-MOS device, considering only the spike event when the I_{sense} current turns-off. This way, it is possible so see how a correct tunning of the current control loop makes that different N-MOS semiconductors achieve a good performance working as limiter devices in this LCL topology.

The second test is based on the use of the LCL prototypes considering a short-circuit at the output of the input filter of a converter, designed to provide 80 dB of attenuation at 160 kHz. The filter design was adapted from [14] and it is based on the harmonic content of the input current of a buck converter. The filter topology chosen is shown in Fig. 13 considering L_f = 150 µH, C_f = 150 µF, C_b = 300 µF and R_f = 1.2 Ω. Fig. 14 shows the experimental results for the LC filter test for the SCT3022AL (ROHM) SiC N-MOS. It is possible to see how the LCL carries the class current and after the short circuit the LCL reacts limiting the current with a good performance, is spite of the presence of a small oscillation in the moment that the LCL is going to limit the current. Fig. 15 shows the same overload test for the SCTW90N65G2V (ST), where it is possible to see that here there in no oscillation when the limitation process is going to start.

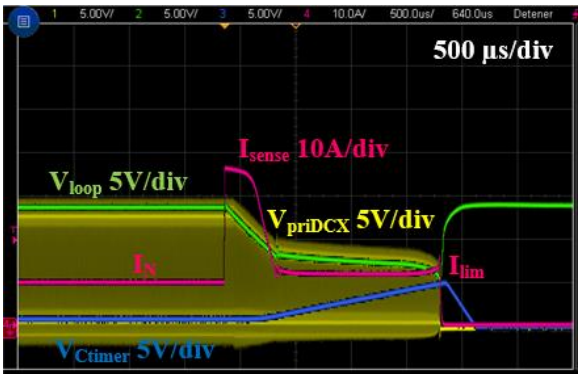

Fig. 11. Class 10 LCL operation waveforms using the SCT3022AL SiC N-MOS

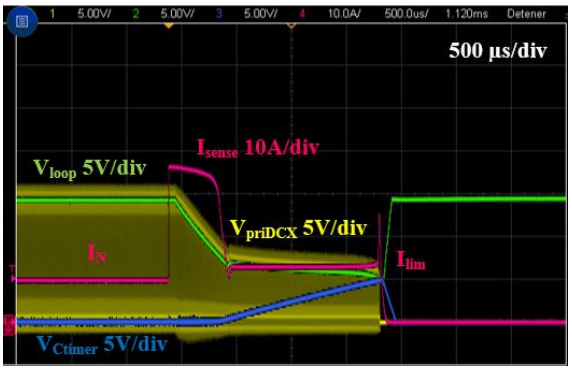

Fig. 12. Class 10 LCL operation waveforms using the SCTW90N65G2V SiC N-MOS

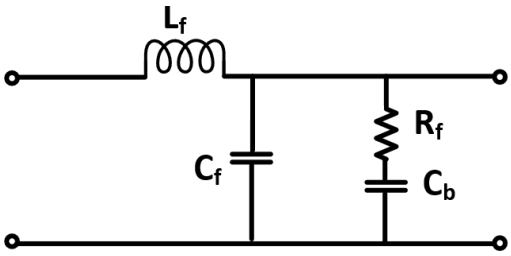

Fig. 13. LC filter implementation

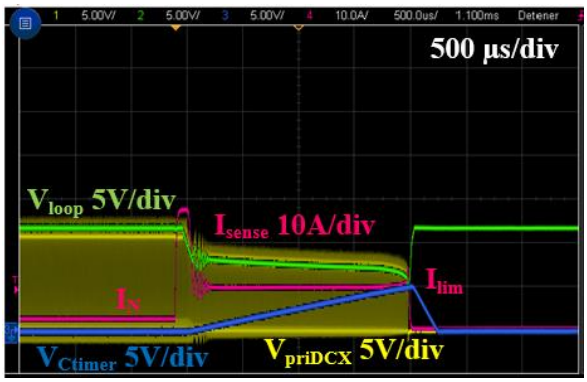

Fig. 14. LCL operation under overload test using and LC filter between the LCL and the load using the SCT3022AL SiC N-MOS

Fig. 15. LCL operation under overload test using and LC filter between the LCL and the load using the SCTW90N65G2V SiC N-MOS

V. CONCLUSIONS

This work remarks some design guidelines of the DCX stage, and the current control loop of a new SiC N-MOS based LCL architecture. Different prototypes of the LCL using two different N-MOS devices have been made, considering a class 10 LCL for a bus voltage of 100 V, and for a maximum limitation current of 12 A. This way, it was verified how the correct tunning of the current control loop, for two different devices, makes that the LCL behavior suits the class specifications. In the same way, a correct design of the DCX stage makes possible the translation of an isolated control signal to control the N-MOS device. The proposed design is flexible enough to be adapted to higher bus voltage levels.

Regarding the DCX-LLC stage is important to remark the relation between the bandwidth, the Q_{tank} factor and the F_R/F_{sw} ratio. This way, it is possible to establish designs for the DCX stage considering high gains and bandwidths for a low Q_{tank} value and for F_R/F_{sw} ratios around the unit. This dependency makes that a higher Q_{tank} involves lower values for the bandwidth.

Regarding the current control loop, a correct tunning of the regulator stage makes possible a correct behavior of the LCL prototypes for different load conditions.

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